The ALICE High Level Trigger

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for the ALICE Collaboration

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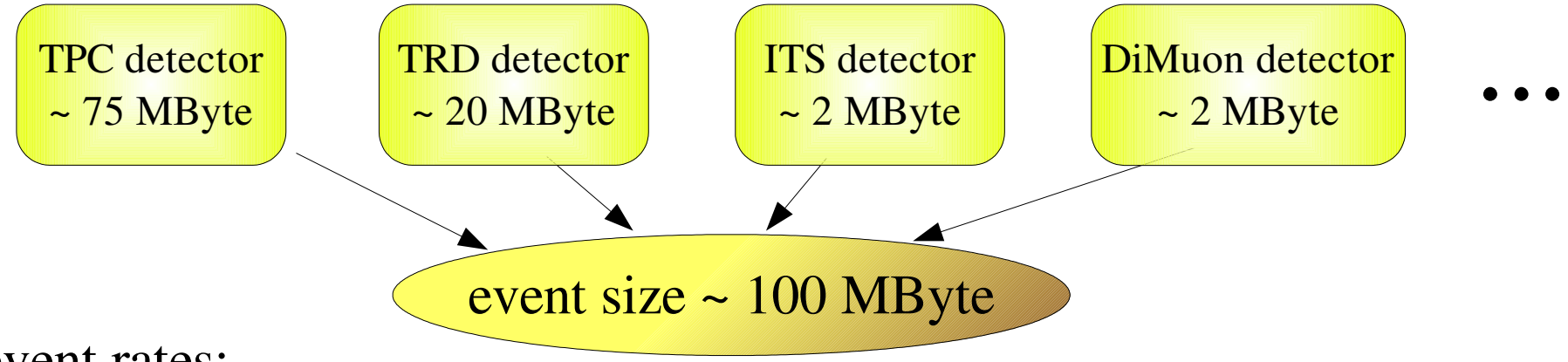
Motivation: Data Rate Reduction

event sizes (zero suppressed):



event rates:

central Pb Pb: ~ 200 Hz
(for events including TPC)
min bias p p: ~ 1000Hz

~ 20 – 25 GByte/sec

maximum total DAQ – rate

~ 1.2 GByte/sec.

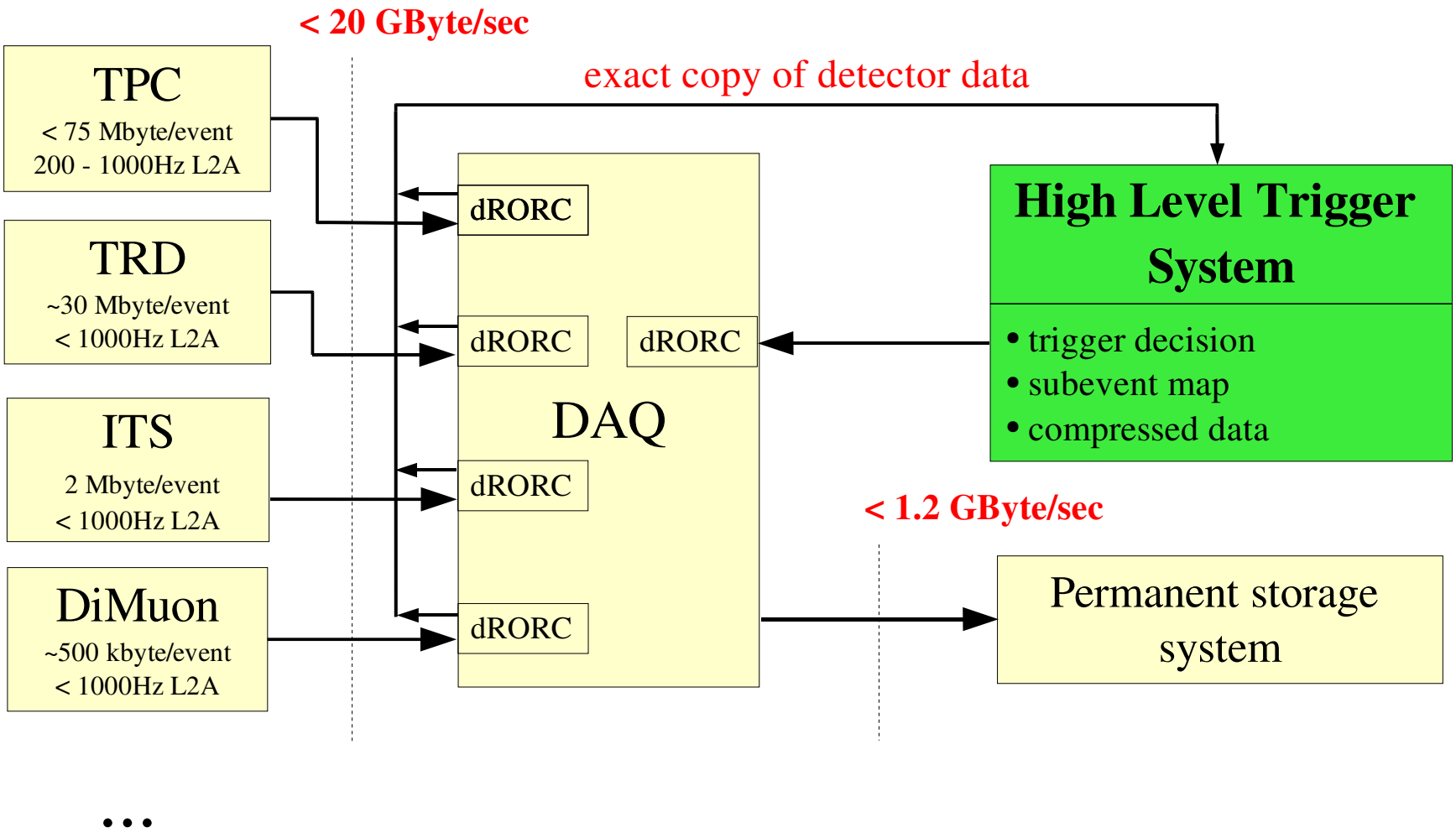
event rate reduction

- low statistics

online event selection

- High Level Trigger

The HLT system in the ALICE data flow



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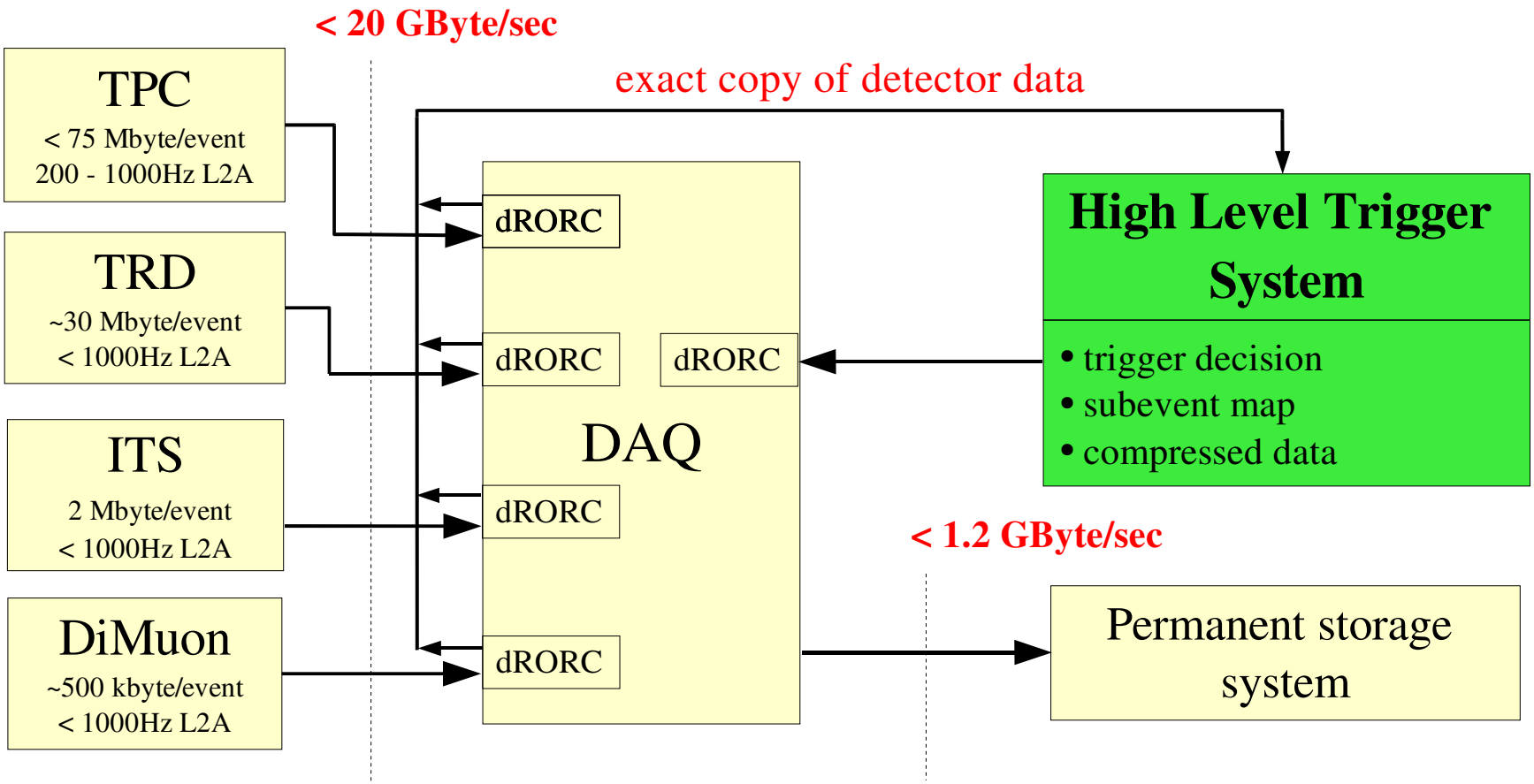
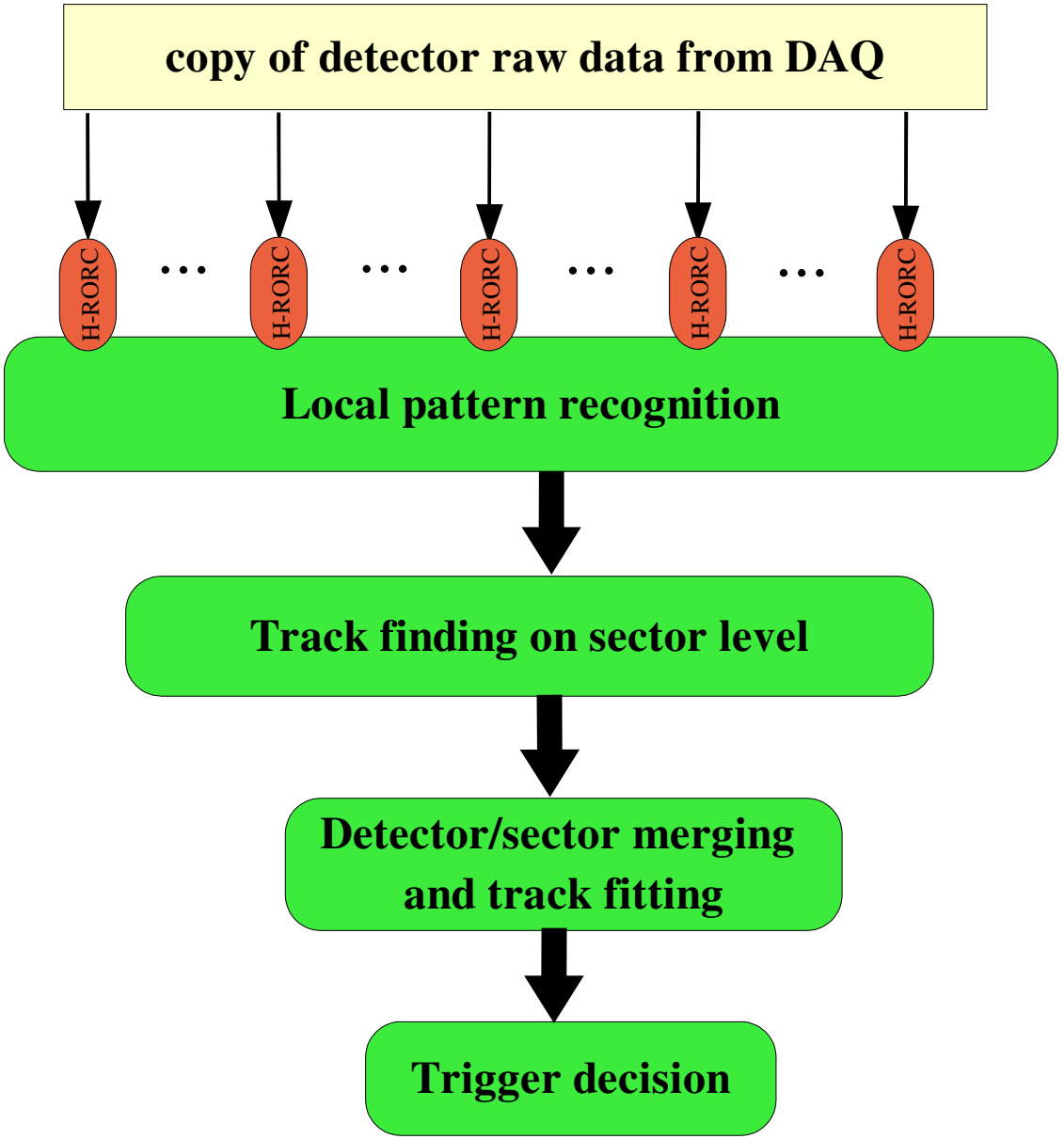


...

Inspected events per year (in TPC)

	Without HLT	With HLT
Pb-Pb	10^7	$20 * 10^7$
p-p	10^9	$10 * 10^9$

Data flow in the HLT



36 TPC sectors, ITS, TRD, ...

DDL: **D**etector **D**ata **L**ink (optical fiber)

HLT-RORC: **R**ead**O**ut **R**eceiver **C**ard
(HLT type with FPGA Co-Processors)

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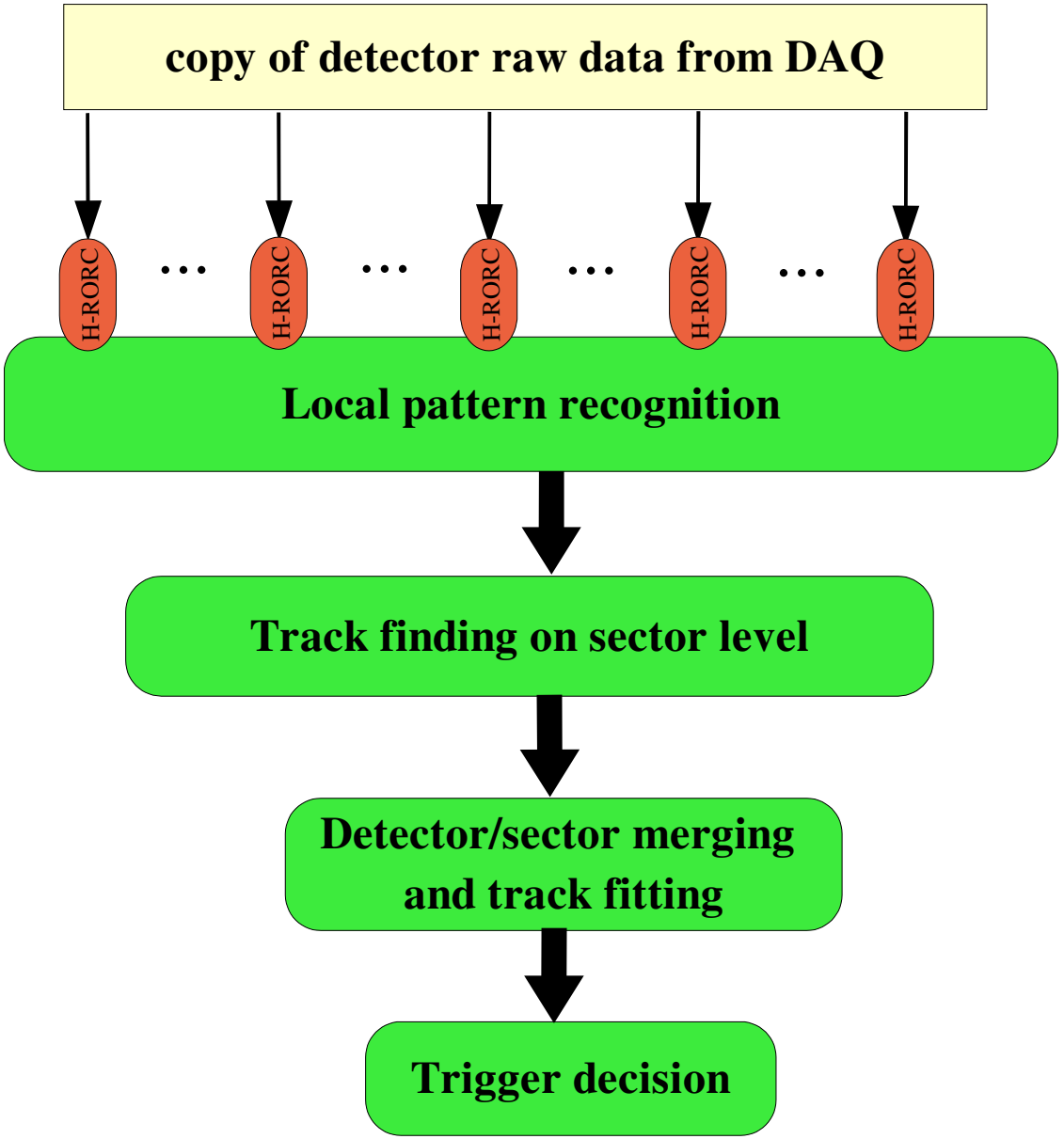

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(HLT type with FPGA Co-Processors)

runs on a PC-cluster

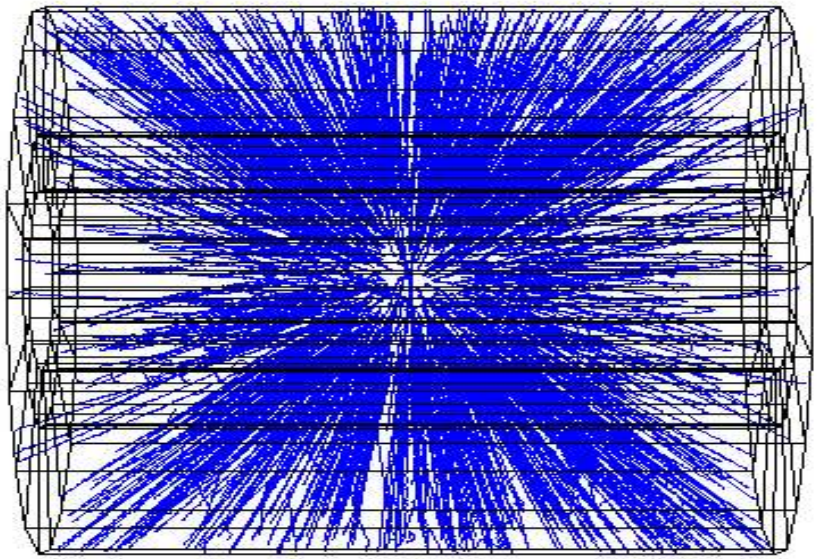
- 450 - 500 nodes
- input from
  ~250 HLT-RORCs

Track reconstruction in the TPC

TPC occupancy:

estimation:

$dN_{ch}/d\eta = 8000$: **20000** tracks in the TPC



two approaches:

Cluster finding

Reconstruct space points from 2D clusters

Sequential tracking

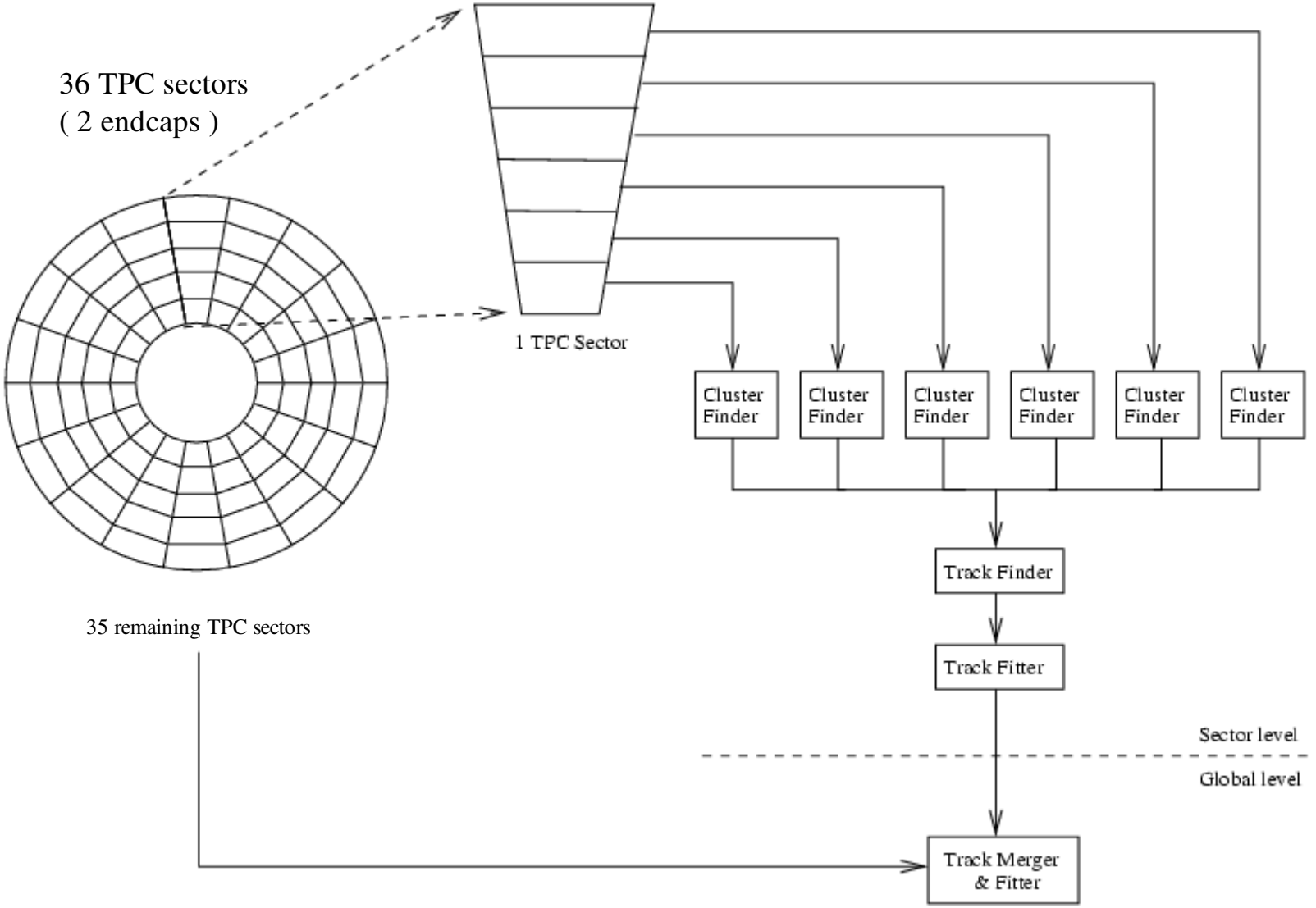
Iterative tracking

Track reconstruction

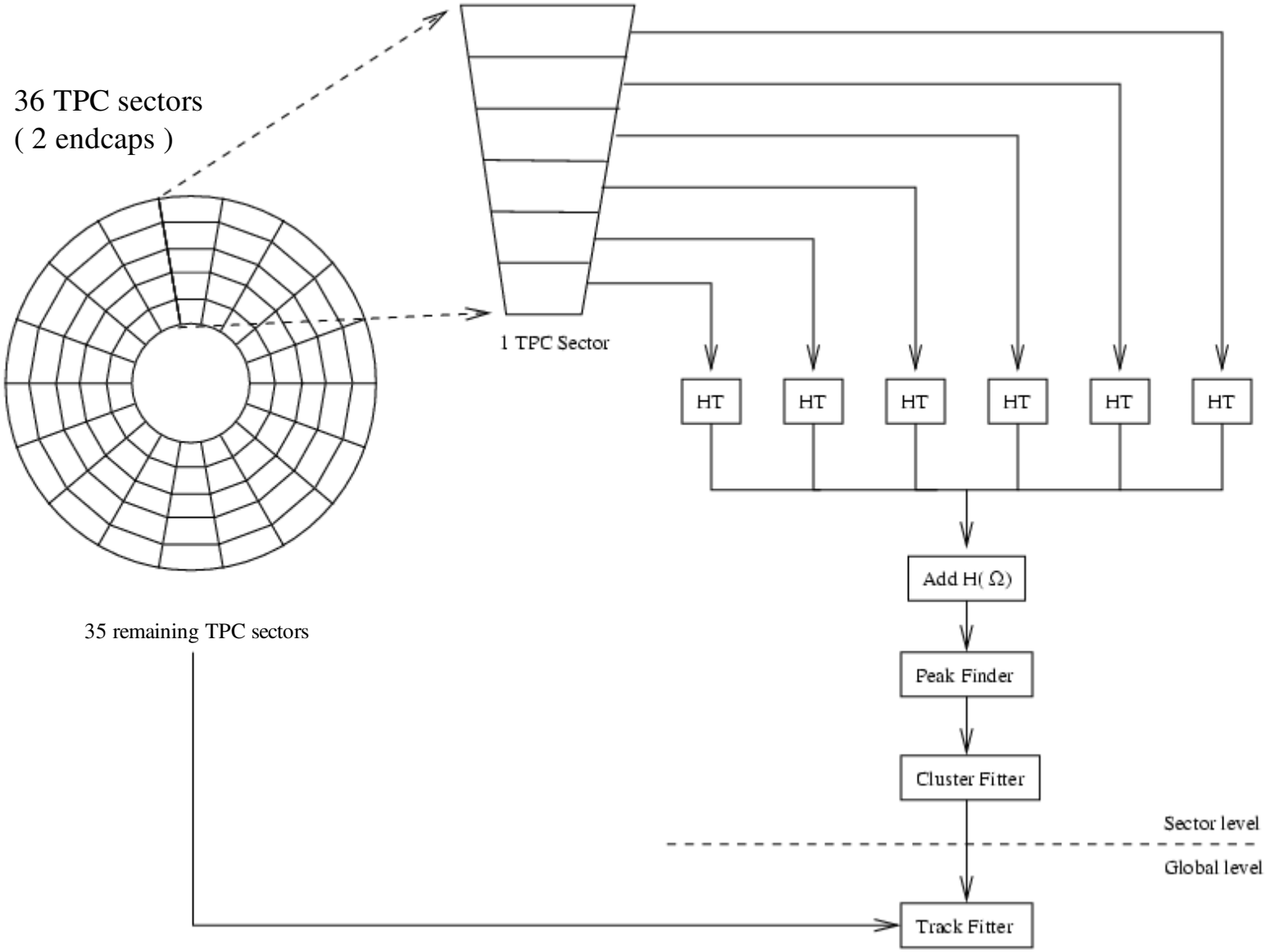
Connect space points into tracks and fit them to a model (helix)

- Sequential tracking
  - Cluster finding (weighted mean)
  - Track follower
- Iterative tracking
  - Hough transform on Raw ADC-Data gives track candidates
  - Cluster fitting with respect to track parameters

Sequential tracking – dataflow



Iterative tracking – dataflow



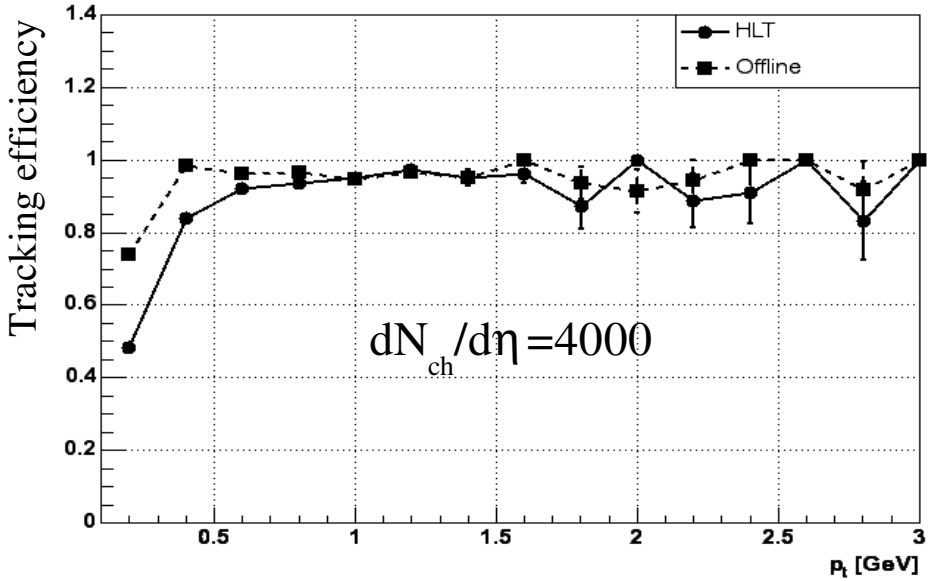
Optical links

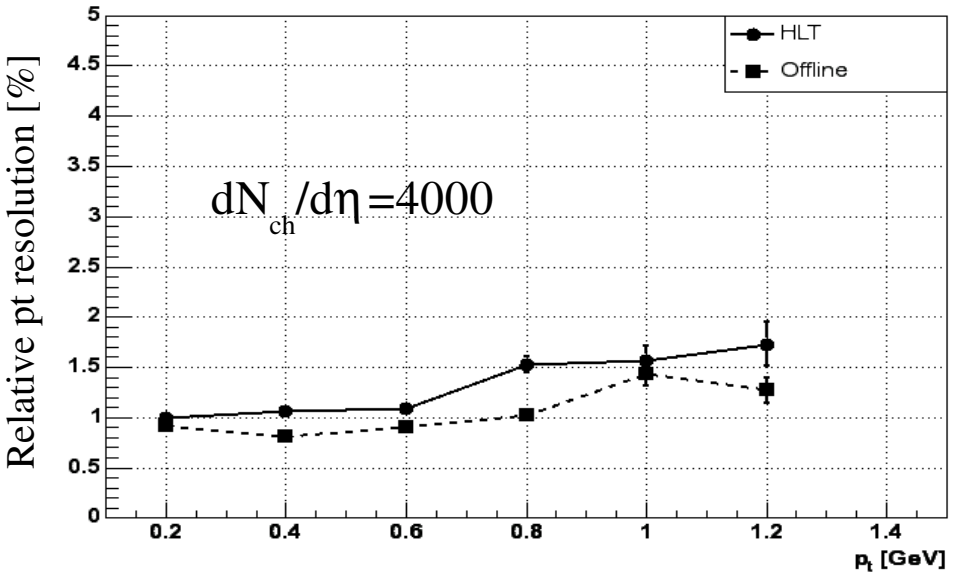
Front-End Processors:
HLT-RORC
(Readout Receiver Card)

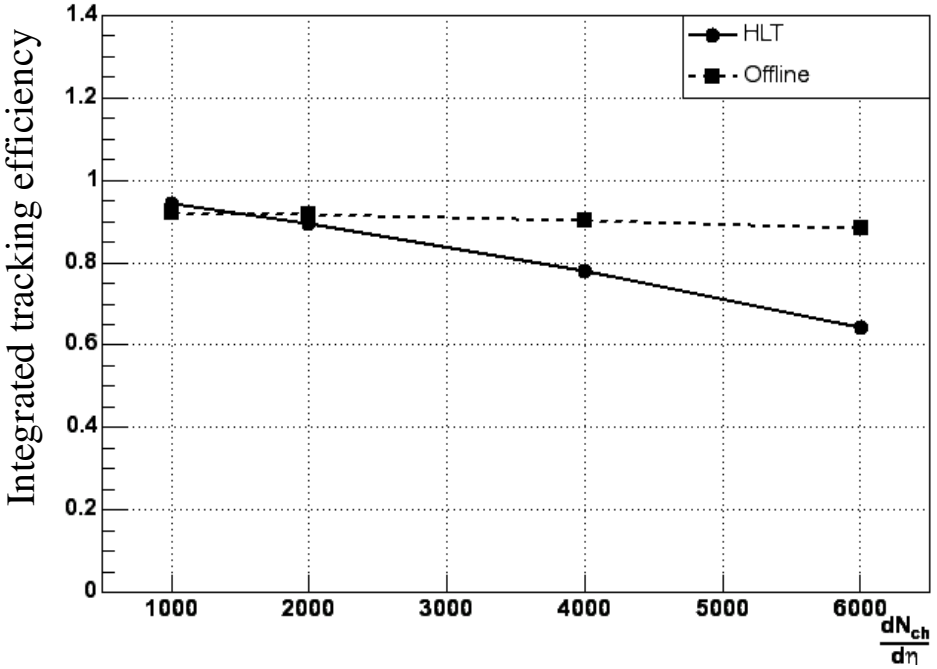
Sector processors

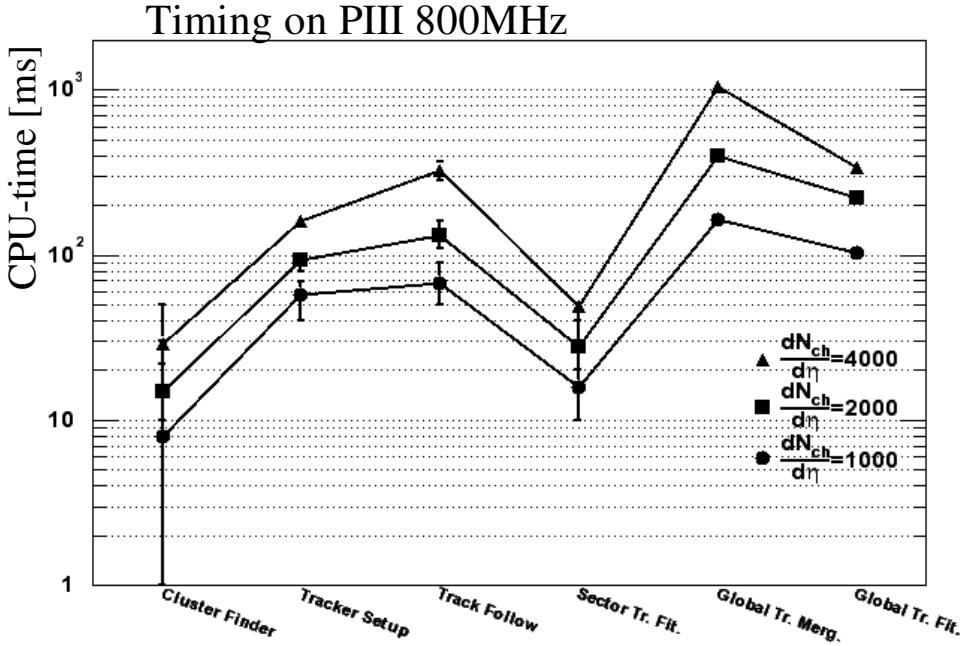
Global/event processors

Performance of track reconstruction









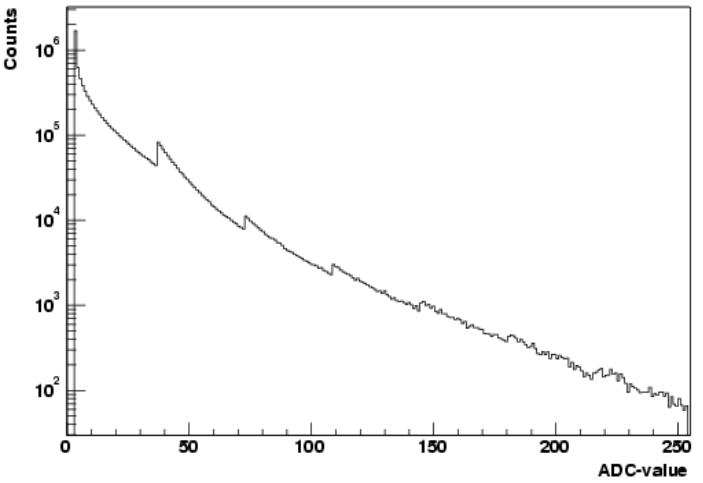
Data compression for TPC data

Local techniques: Applied on the scale of ADC-data.

(NIM **A489** (2002) 406)

	Type of encoder	**Relative event size [%]**
Lossless	Arithmetic Coding	80
	Huffman Coding	71
Lossy	Vector Quantization	64-48

Prob. distribution of ADC-values



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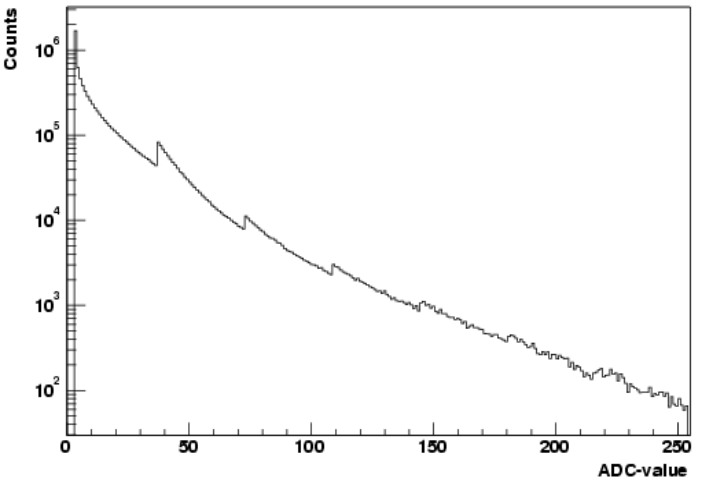
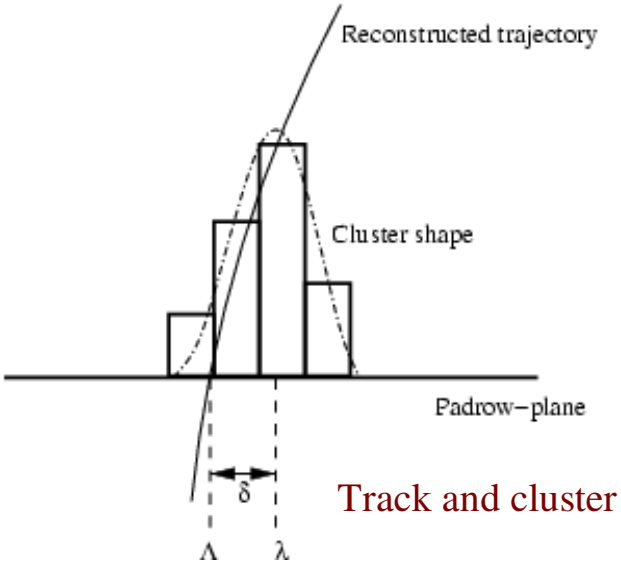


Global techniques: Applied on the scale of clusters and tracks.

Cluster position represent small deviations, δ,
from the track fit and is subject to detector resolution.

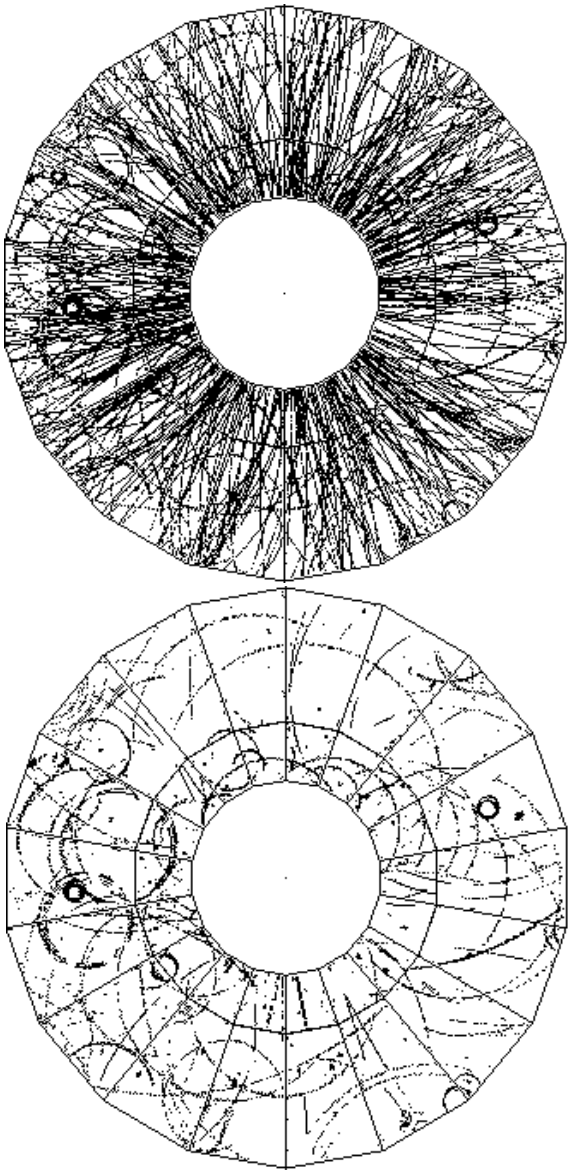
Cluster widths are a function of track parameters

Describe the clusters within the track model,
and store only deviations from the model.

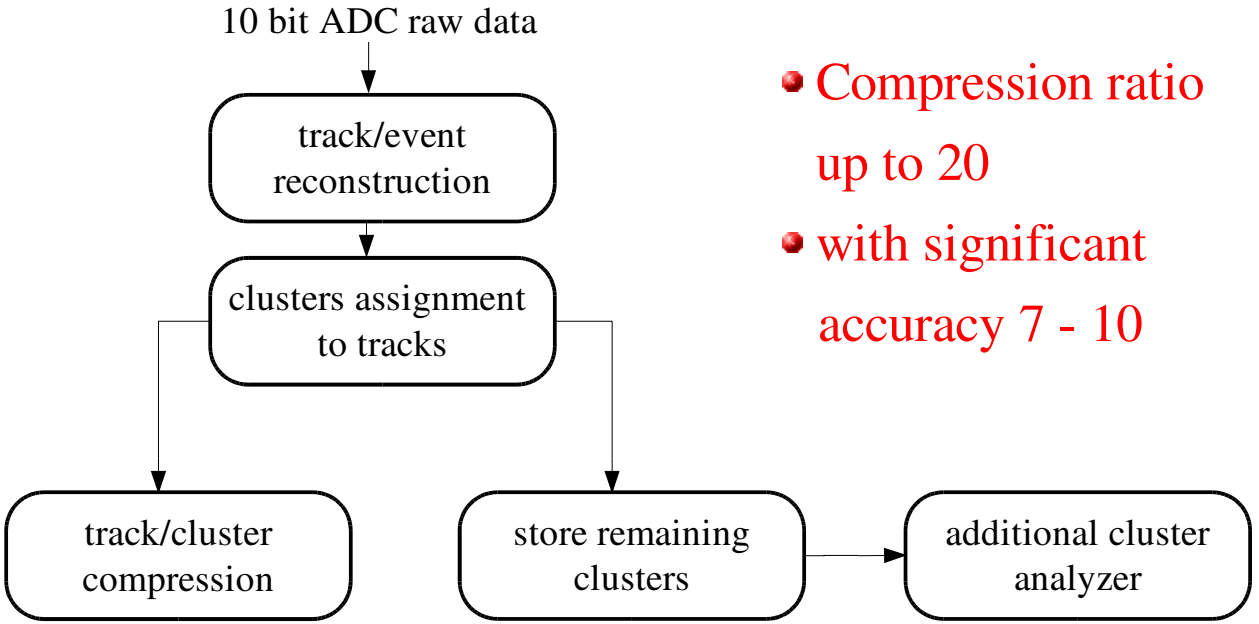


Track and cluster modeling

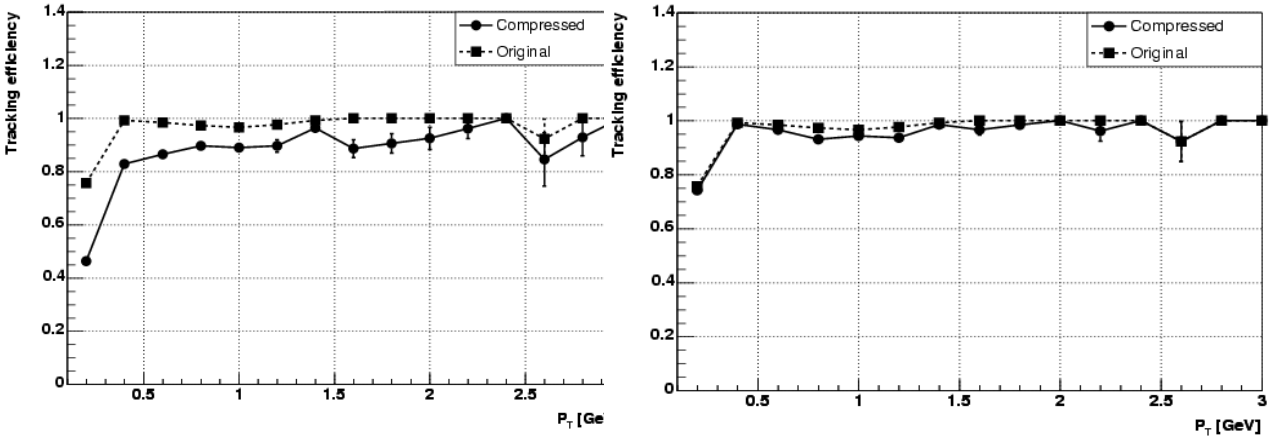
Data compression II



TPC display before and after cluster asignment and removal



- Compression ratio up to 20
- with significant accuracy 7 - 10

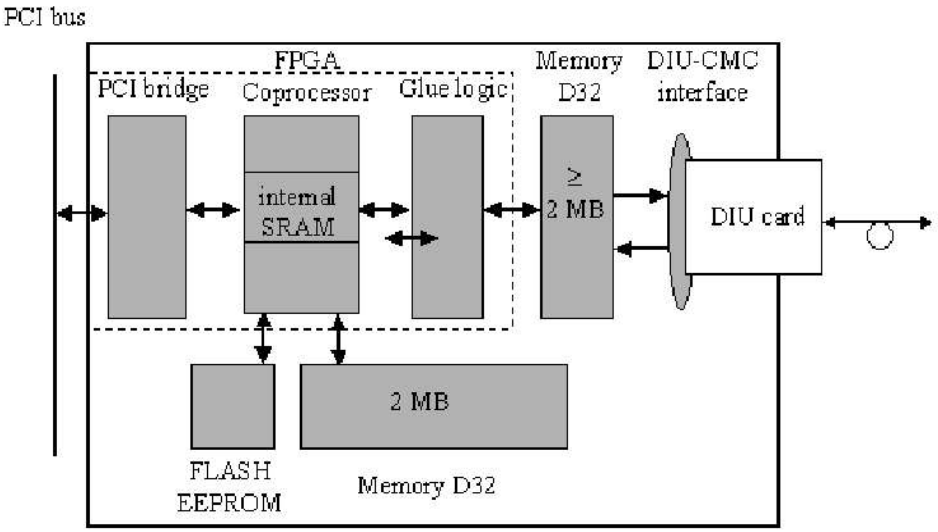


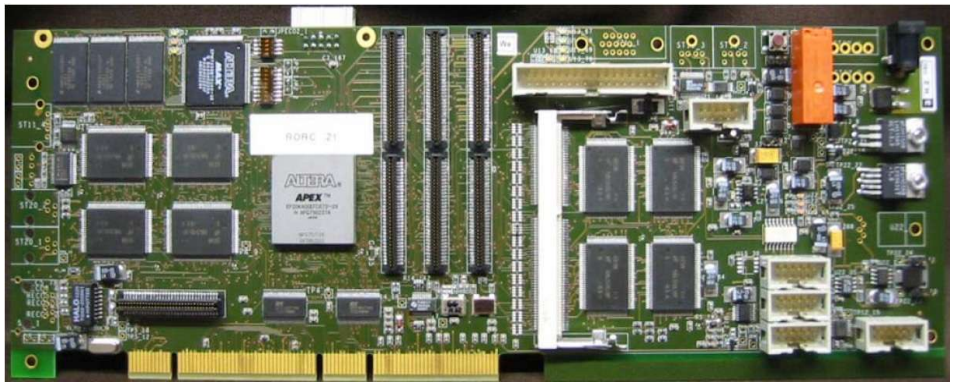
Tracking efficiency: left removing all remaining clusters, right keeping selection

Components of the HLT system

- Commercial off-the-shelf PCs
  - ~250 dual processor PCs equipped with HLT-RORC cards with FPGA Co-processor
    HLT Front End Processor (FEP)
  - ~250 dual processor compute nodes

HLT Readout Receiver Card





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  - NIC (Gigabit Ethernet, InfiniBand,...)
  - Network protocol (TCP)

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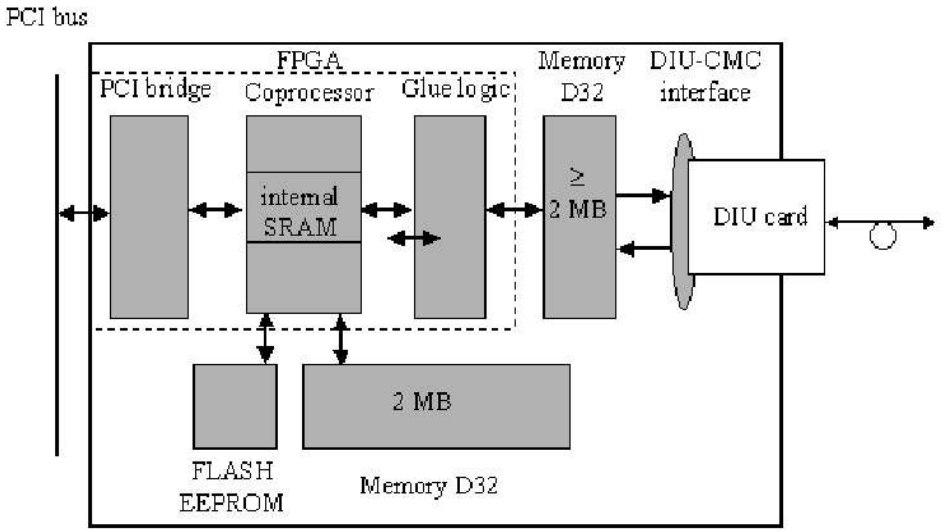

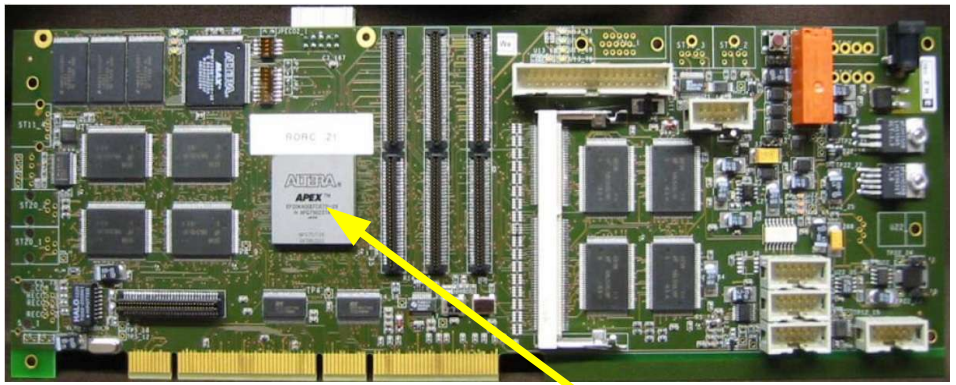

Local Pattern Recognition in the onboard FPGA

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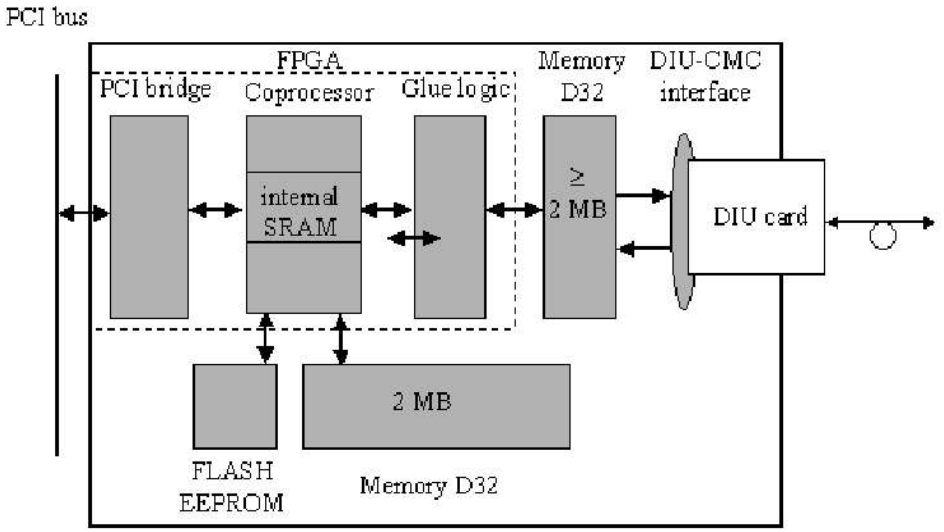
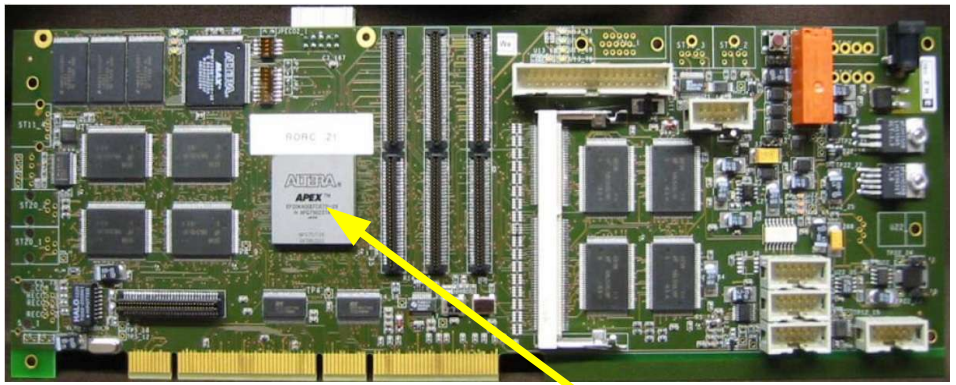
- Network Communication
  - NIC (Gigabit Ethernet, InfiniBand,...)
  - Network protocol (TCP)
- Fault-tolerant cluster management
  - Cluster Interface Agent (CIA)
    - low cost sensor and actuator
    - allows system detection and repair decoupled from the node's software system
  - see talk of R. Panse this conference for details

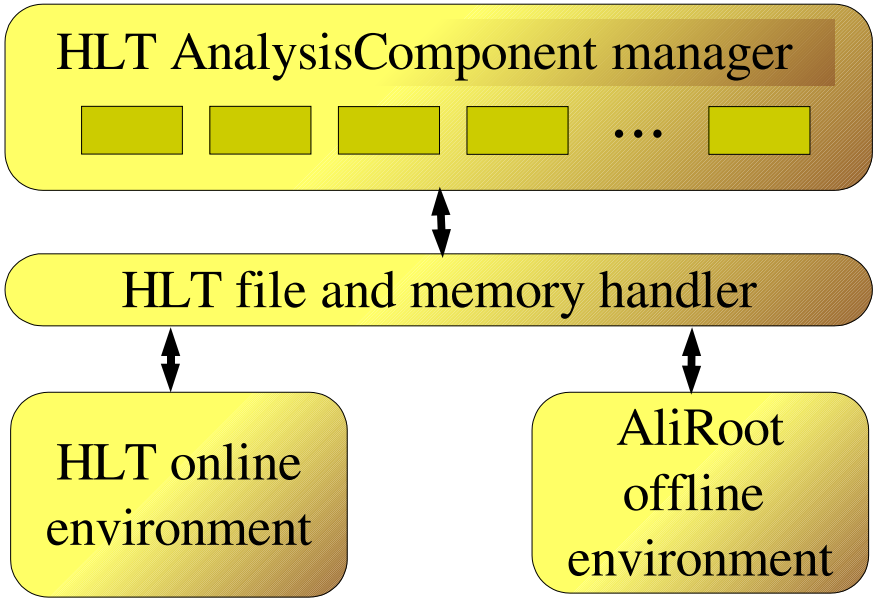
HLT Readout Receiver Card





Local Pattern Recognition in the onboard FPGA

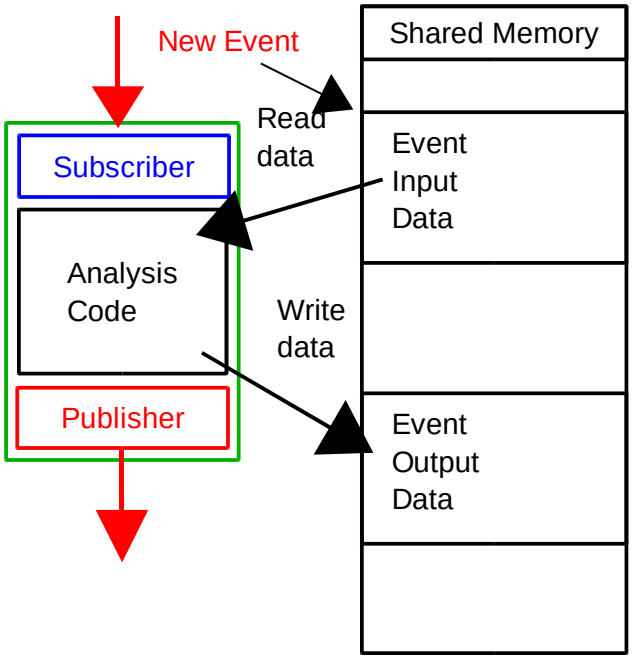
Management of the HLT software



- Analysis components
  - developed in the ALICE offline framwork AliRoot
  - written in C++
  - data internally organized in simple C structures to minimize size
  - abstract interface connects analysis components to either online or offline framework

- Publisher-Subscriber Interface
  - Communication framework running on HLT cluster
  - Common interface for communication between processes on the same node and also between different nodes across the underlying network
  - Generic modular framework allowing arbitrary connectivity metric (one-to-many, many-to-one)

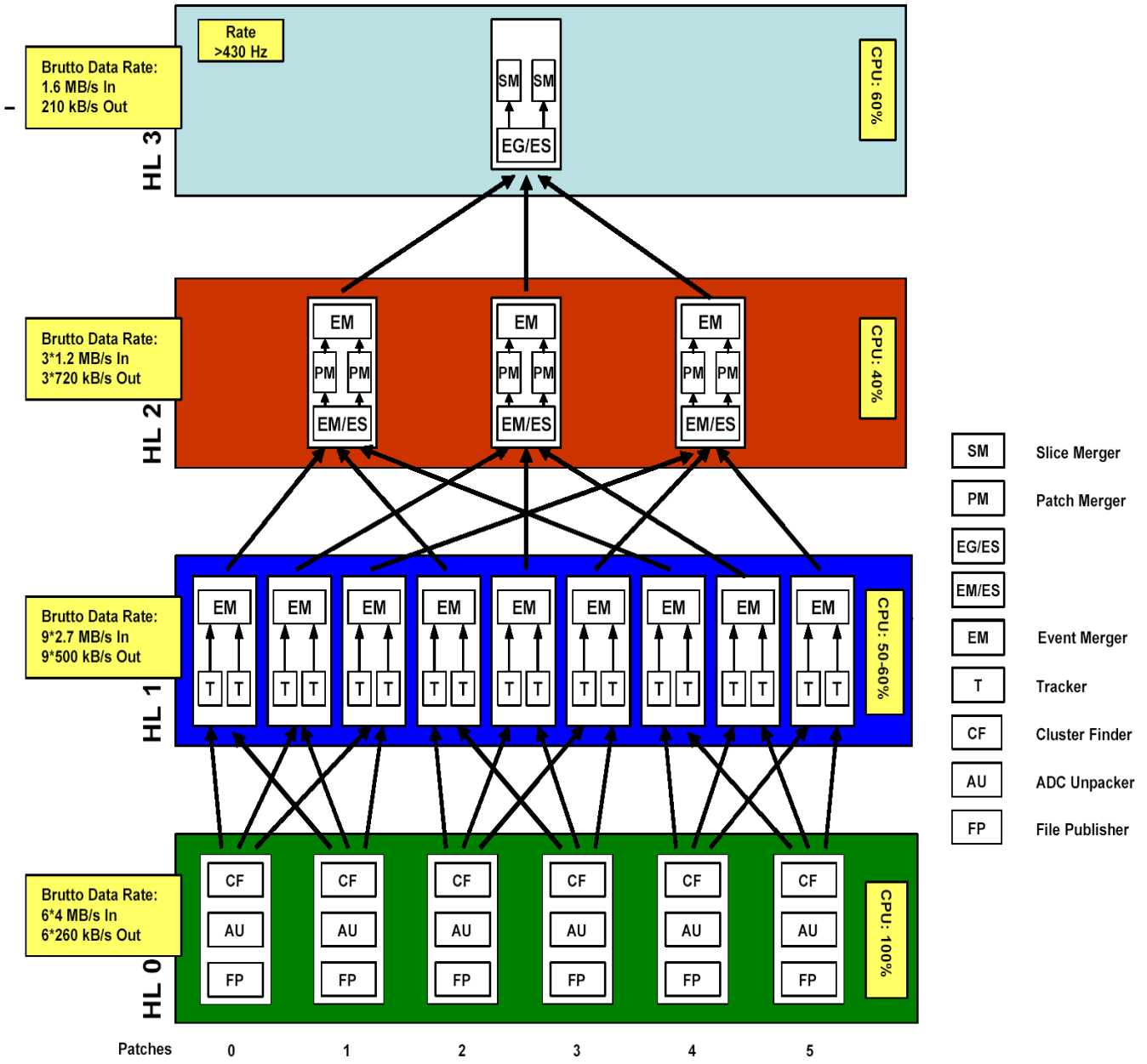
  - see talks of T. Steinbeck this conference for more details

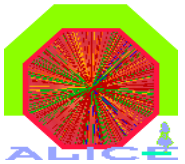


Prototype for one TPC sector

- Simulated 'realistic' pp events
  - 25 piles (~400 particles in TPC)
- Full track reconstruction
  - Cluster finder + Track finder
- 19 Nodes, P3 800 MHz dual proc., Fast Ethernet

Heidelberg HLT cluster





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- The system will consist of up to 500 dual processor PCs, partially equipped with FPGA Co-processors
- Current online tracking performance is sufficient for $dN_{ch}/d\eta < 4000$ already now
- Data modeling indicate compression factors of about 10 with acceptable efficiency loss
- HLT prototype performance on p-p for pileup-removal already very satisfactory, next integration tests following fall 2004

Thank you for your attention

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