Development in electronics and packaging for future pixel detector systems

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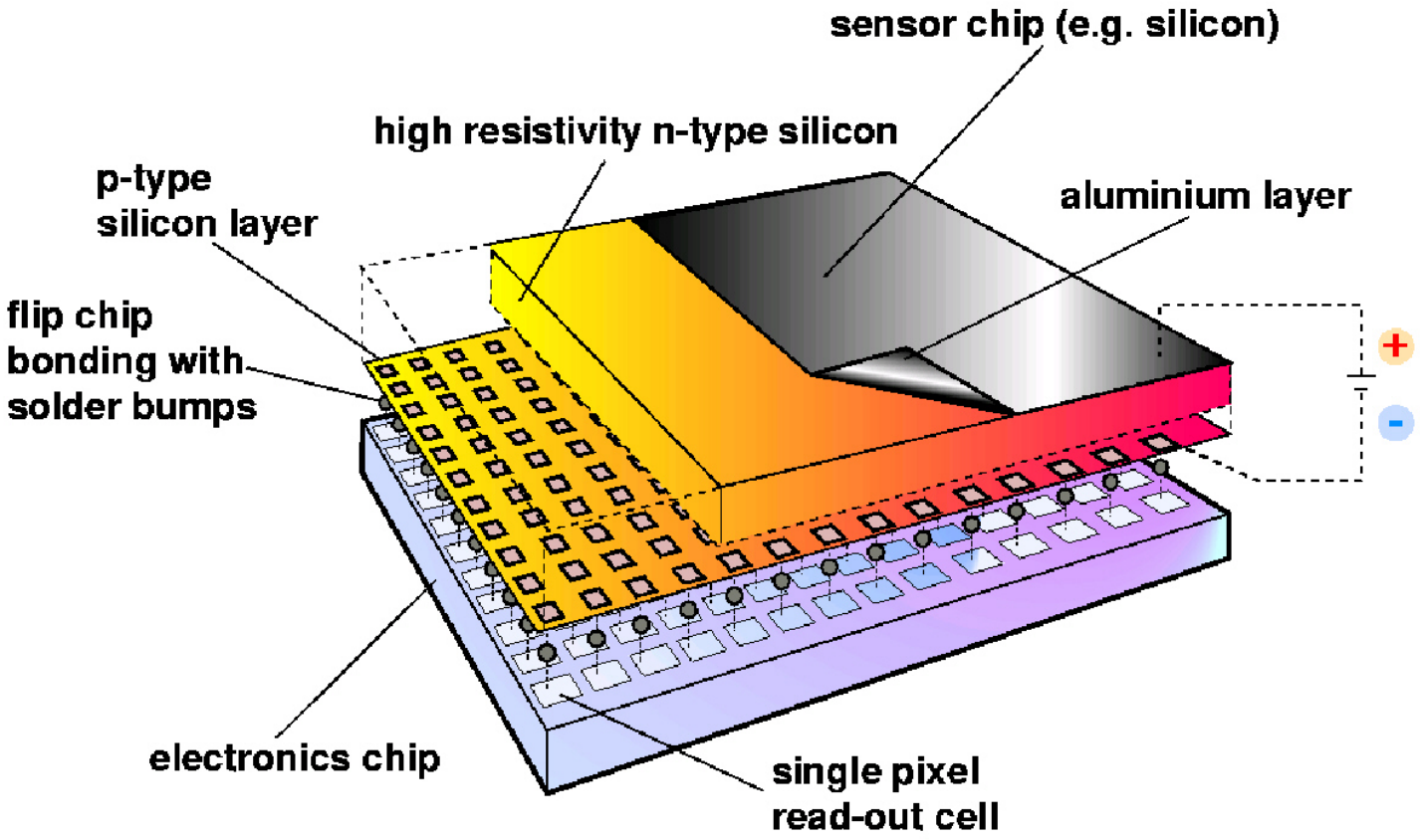
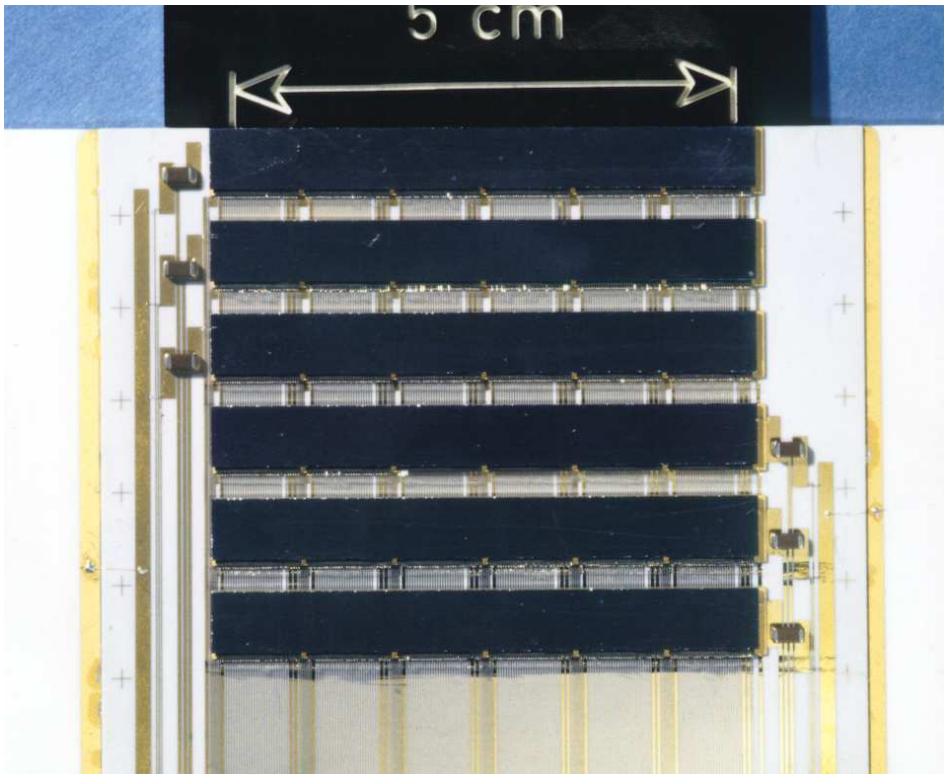
Outline

- Introduction
- Developments in CMOS
- Status of flip chip packaging
- HEP specific requirement - radiation hardness of CMOS
- An LHC detector using Deep Sub Micron CMOS and state-of-the-art packaging - the Alice Silicon Pixel detector
- Beyond LHC

Hybrid Pixel Detector



A (by now rather old) pixel detector array



36 000 pixels

6 ladders of 6 chips

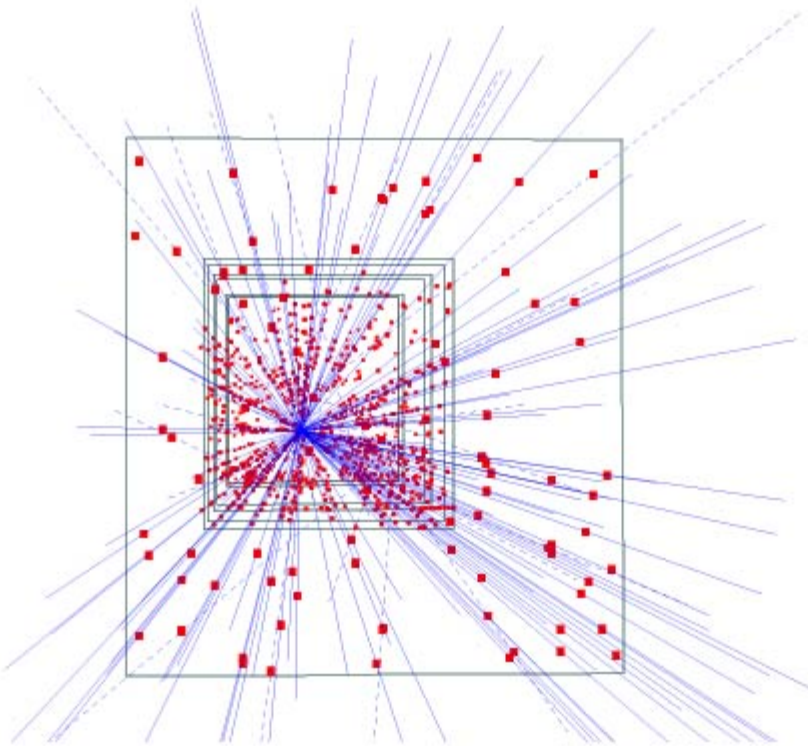
Each chip has 1000 pixels

2 arrays make up one logical plane

[E. Heijne, E. Chesi]

Work carried out by RD19 for WA97.
Basic development funded by CERN-LAA programme.

A Clean Heavy Ion Physics Event



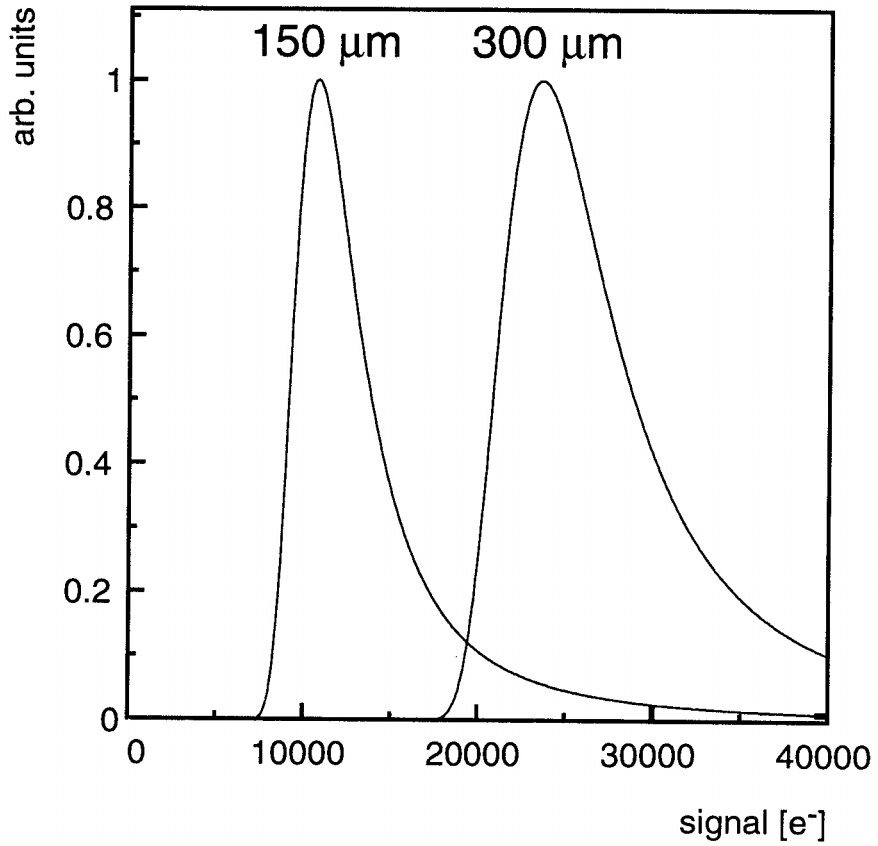
CERN Experiment WA97 (1995)

5 x 5 cm^2 area
7 logical planes
Pixel dimensions 75 x 500 μm^2

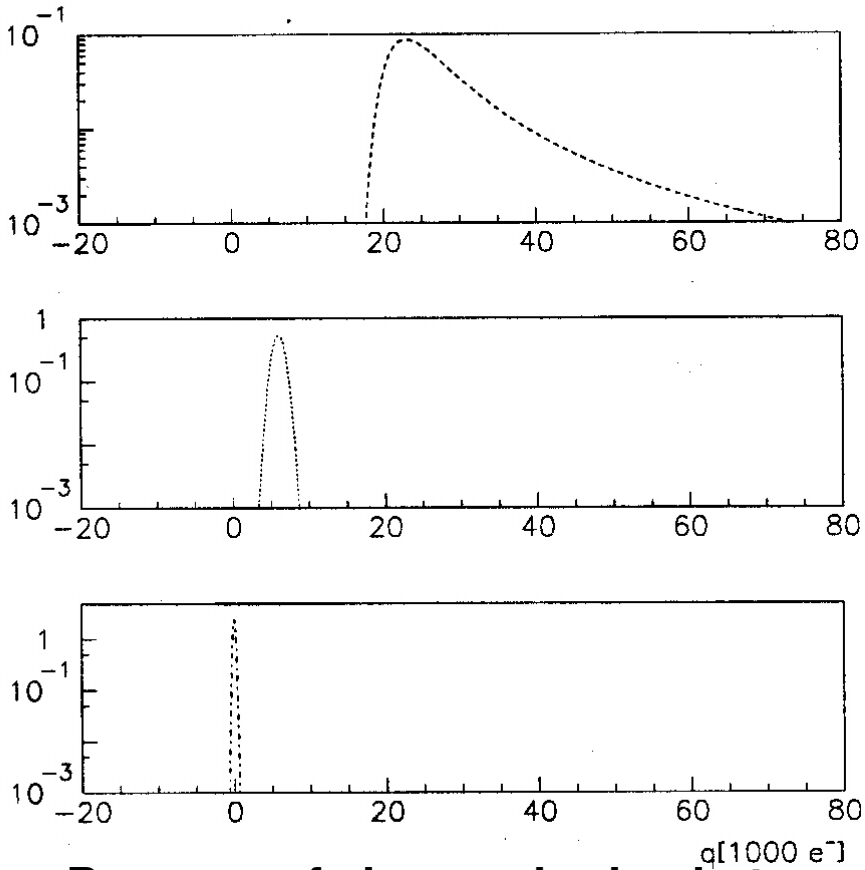
But…

Trigger precision 1 μsec
Radiation tolerance ~ 30kRad

Minimum Ionizing Charge Deposition in Si



Signal, Threshold, Noise



Landau for 300 μm detector

Threshold and threshold variation

Noise

Because of charge sharing between pixels the threshold is normally set around 1/3rd Landau peak while maintaining optimum detection efficiency and spatial resolution

Noise hit rate for a discriminator with bandwidth, f_b

$$f_n = \frac{1}{\sqrt{3}} f_b \exp\left(\frac{-Q_{th}^{\,2}}{2\sigma_n^{\,2}}\right)$$

Q_{th} = threshold
σ_n = noise

(It can be shown that σ_{th} - the threshold variation - adds to σ_n quadratically on the denominator.)

In a large bandwidth system (such as an HEP experiment) noise and threshold must be well separated to produce clean event information.

Some typical numbers… (from WA97 telescope)

- Noise < 200 e- rms
- Threshold ~ 6 000 e-
- Threshold variation ~ 350 e- rms
- Around 3% loss of sensitive area due to dead or ‘singing’ (masked) pixels
- 60 000 false triggers applied
  - NO noise hits recorded in 97% of good pixels
  - Therefore noise rate per channel < 10^{-10}

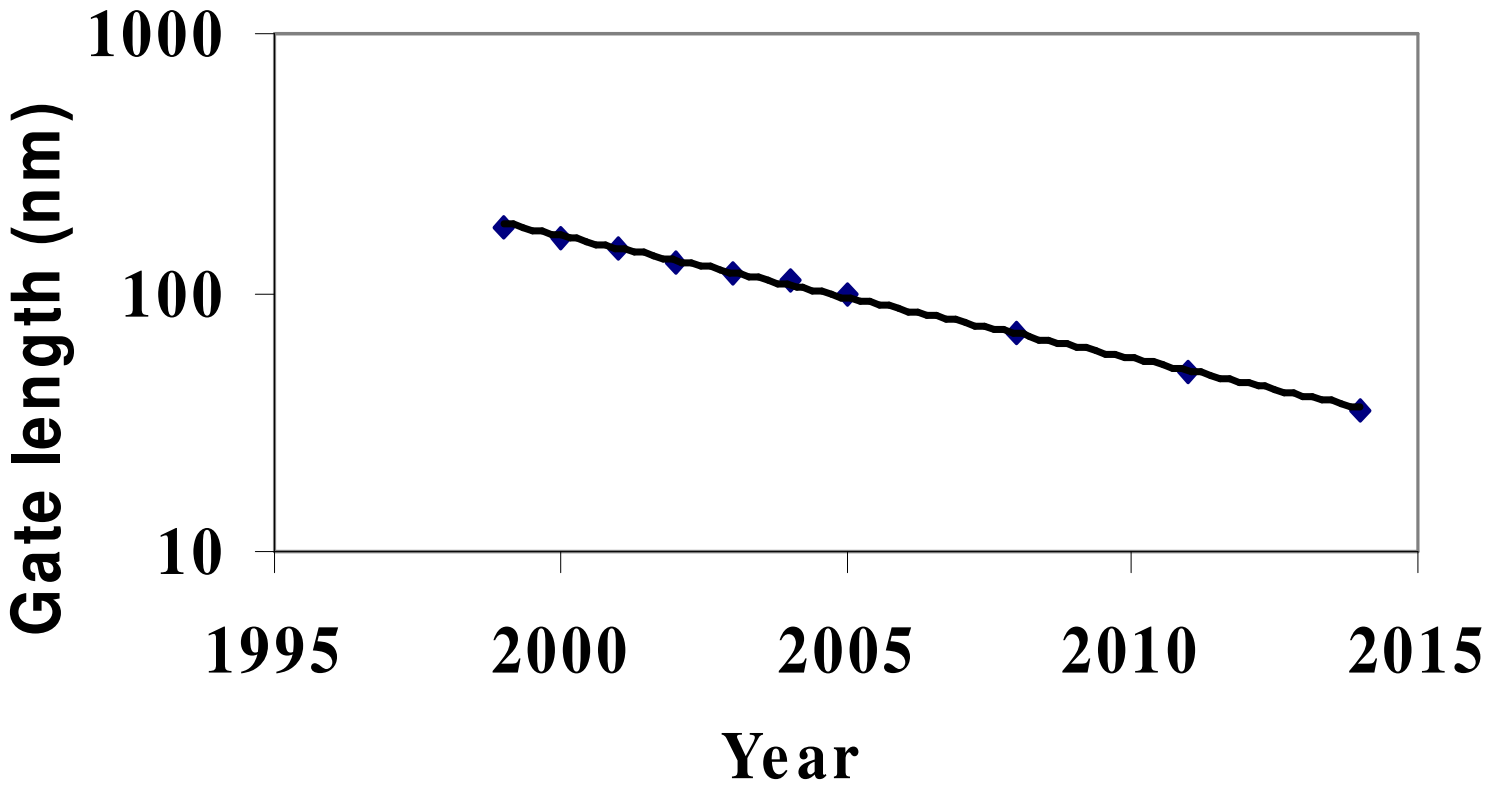
In a high multiplicity environment pixel detectors are crucial to pattern recognition. Technical choices are bound by this. Limits of present and future systems will be discussed later in this presentation.

In low multiplicity or low rate environments signal to noise constraints can be relaxed leading to simpler lower power solutions.

Developments in CMOS

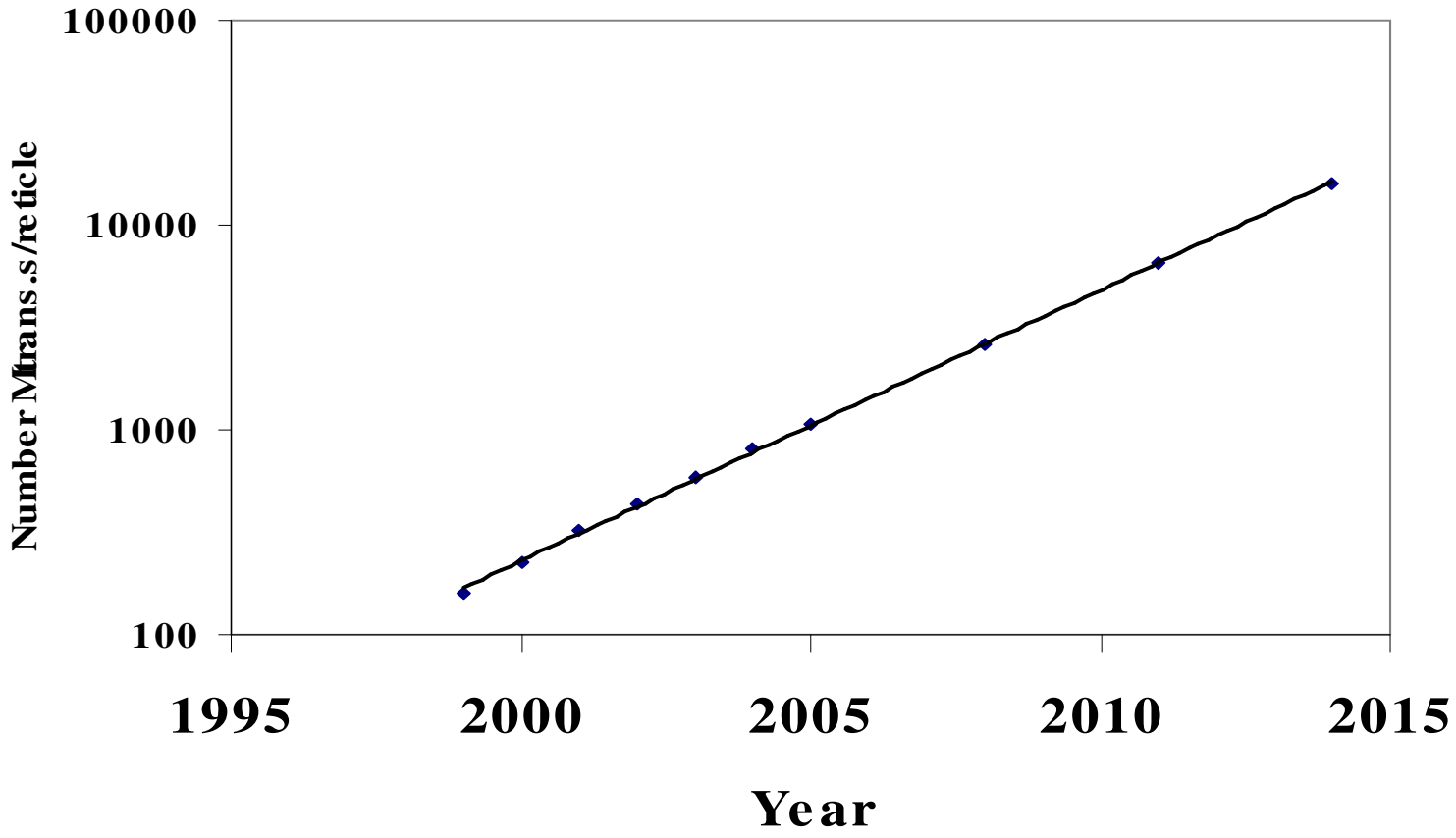
- CMOS is the workhorse for the entire industry
- Other technologies (e.g. bipolar, SiGe, GaAs) are used in niche applications but none can compete with CMOS in terms of yield, component density and chip size.
- Experience from the LHC developments indicates that CMOS is the only viable solution for large scale systems

Transistor feature size



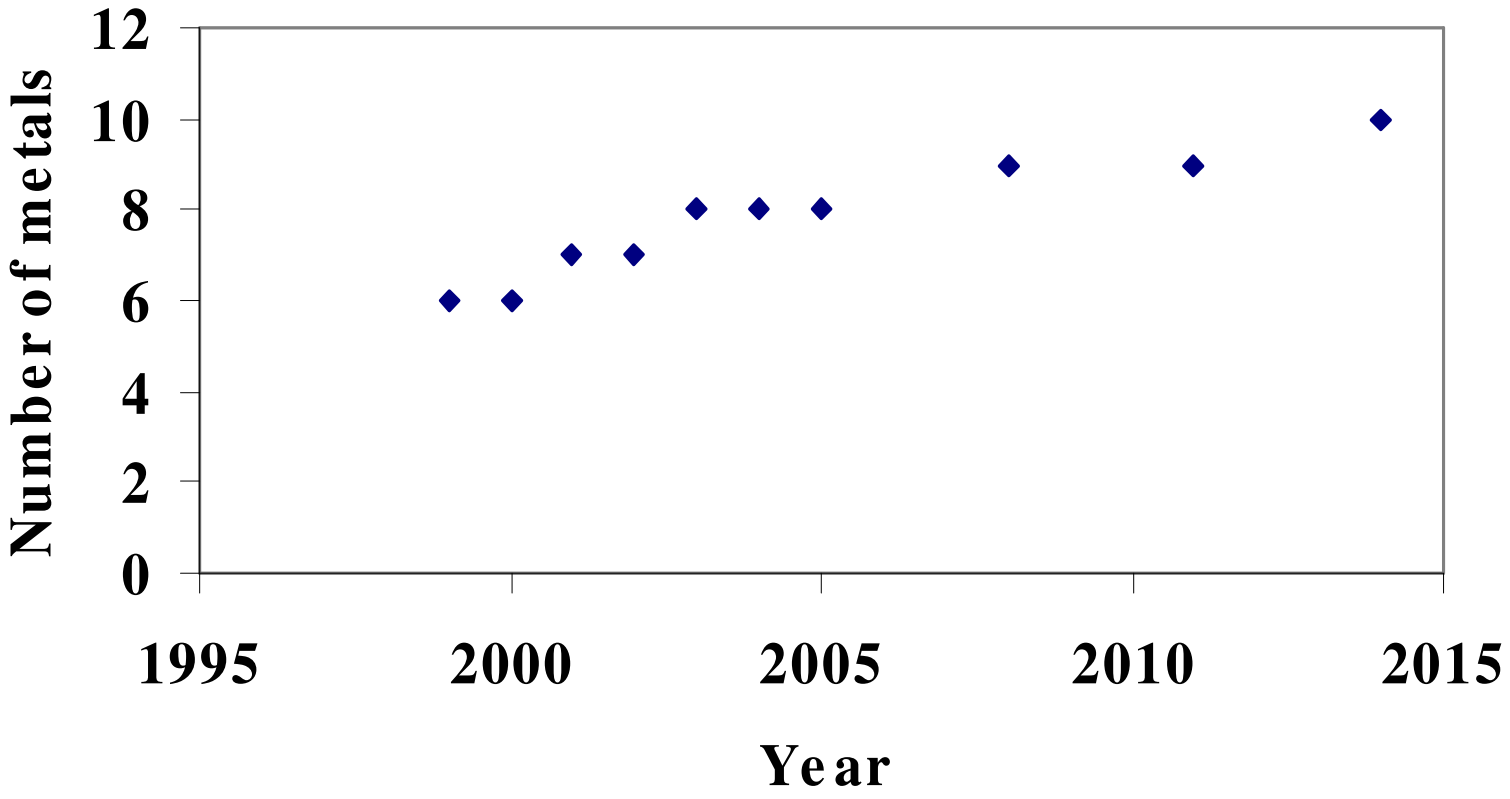
SIA Roadmap 1999

Components per chip



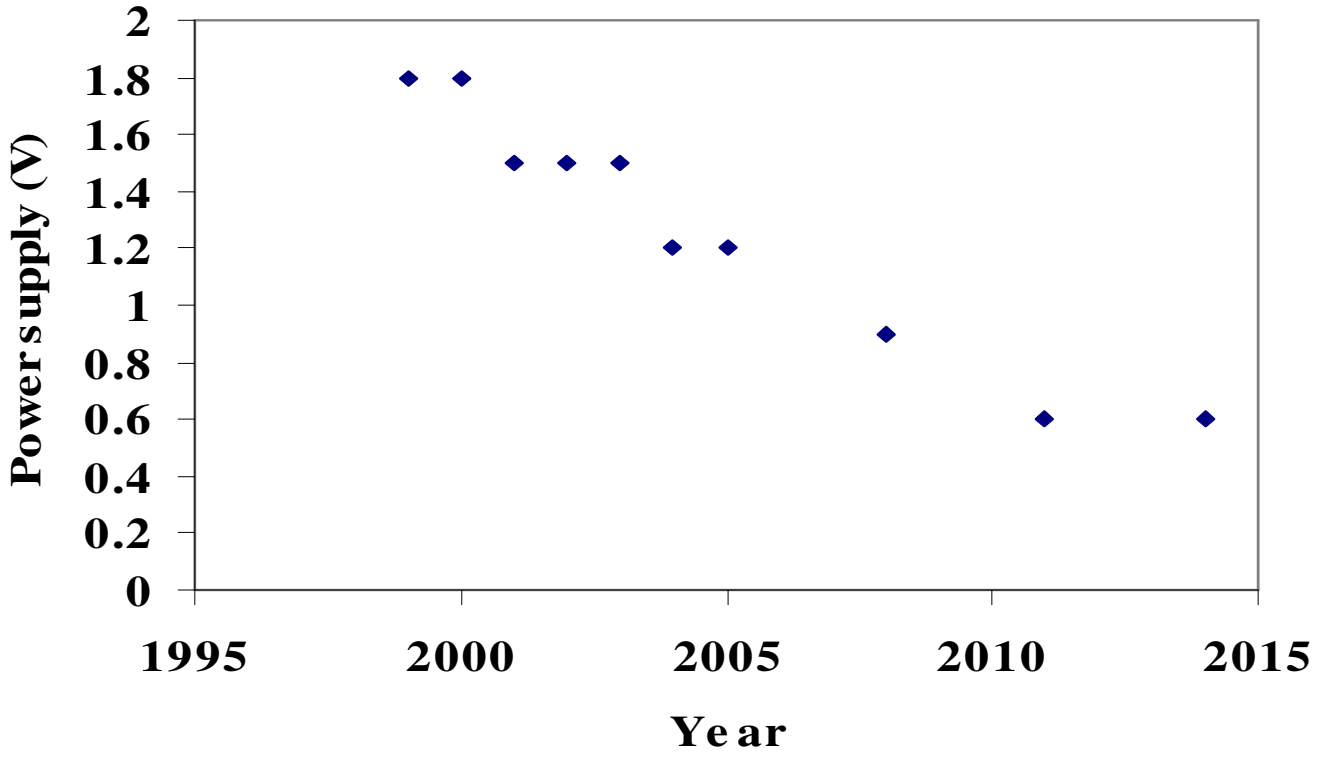
SIA Roadmap 1999

Metal layers



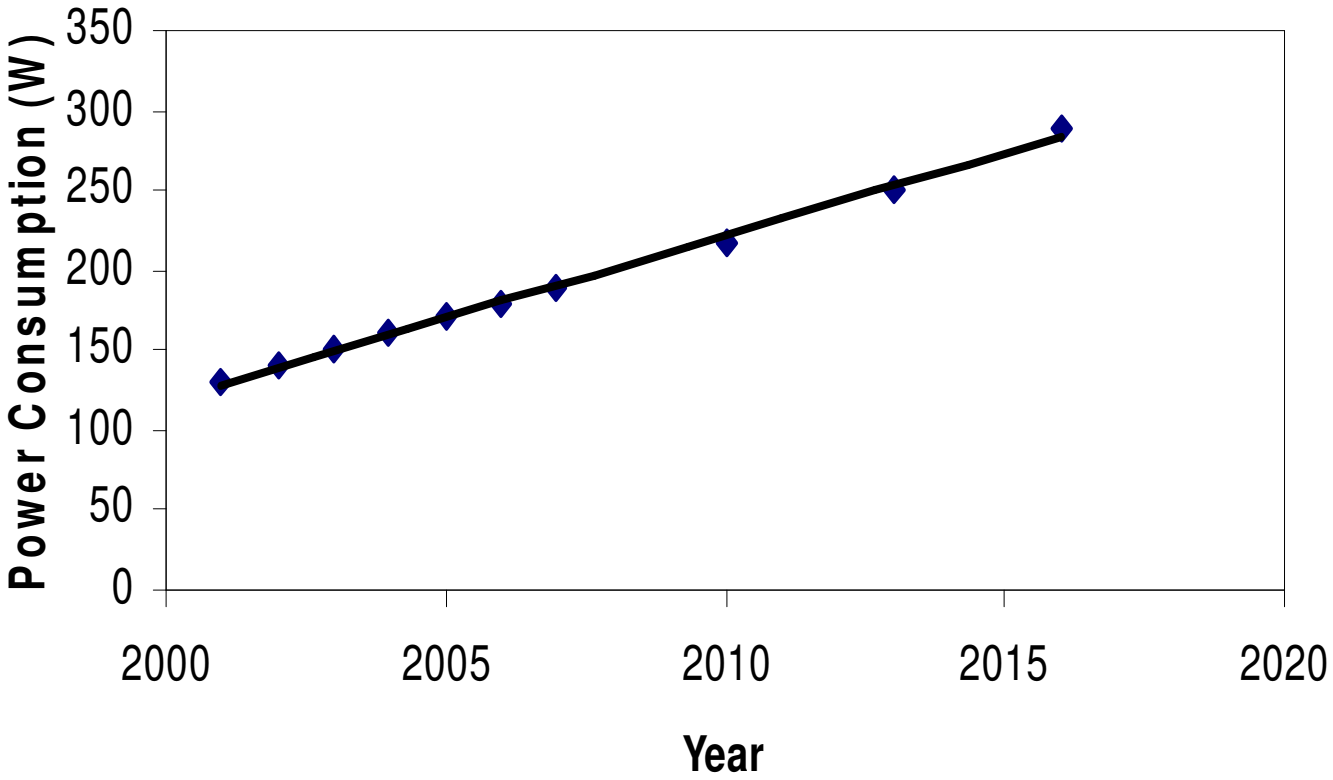
SIA Roadmap 1999

Power supplies



SIA Roadmap 1999

Power per processor chip



SIA Roadmap 2001

Present day CMOS - 1

A 90nm Logic Technology featuring 50nm strained Silicon Channel Transistors, 7 layer of Cu Interconnects, Low k IDL and 1um2 SRAM Cell
Intel

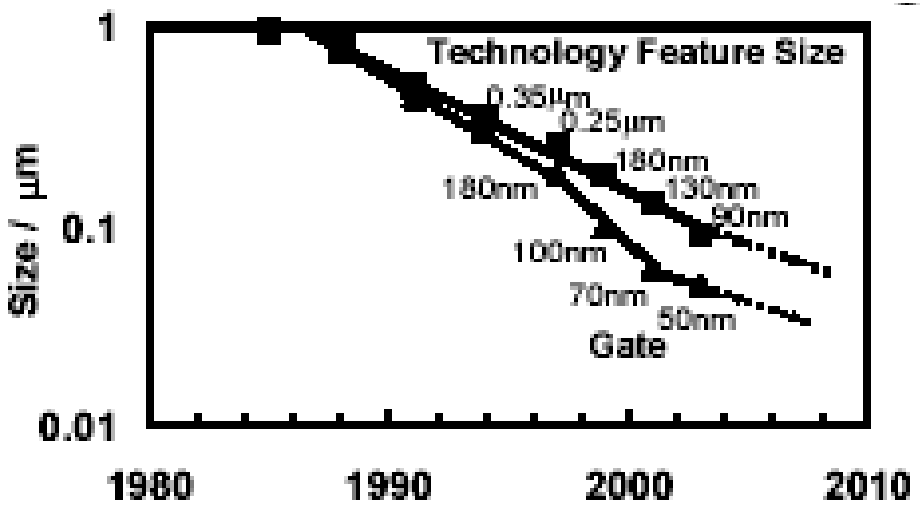
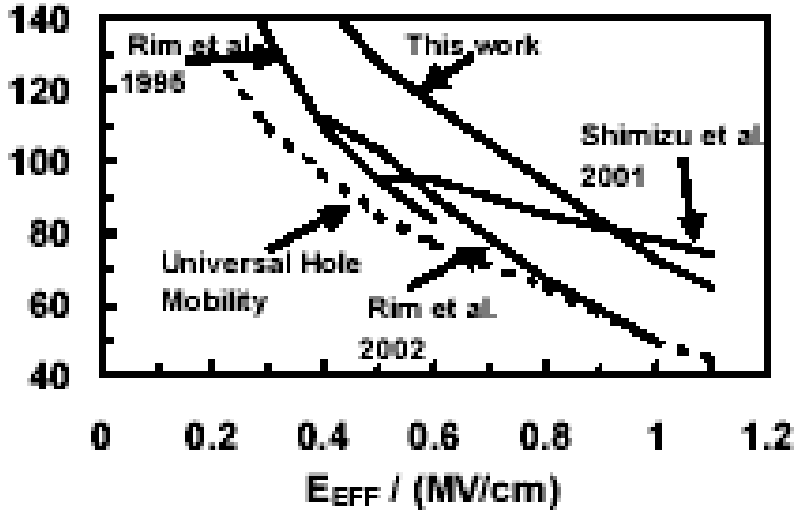


Figure 5: Transistor size and technology trend.



gure 9: Hole mobility as a function of effective field.

[S. Thomson et al., IEDM, San Francisco, 8-11 Dec. 2002 (next 2 slides)]

Present day CMOS - 2

A 90nm Logic Technology featuring 50nm strained Silicon Channel Transistors, 7 layer of Cu Interconnects, Low k IDL and 1um2 SRAM Cell
Intel

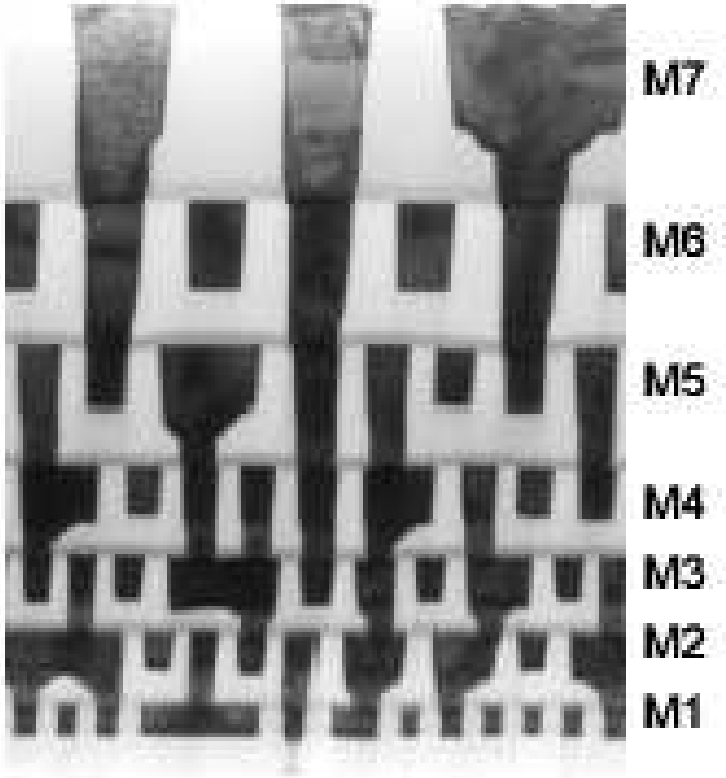


Figure 13: Cross-section SEM image of a processed wafer.

Present day CMOS - 3

A 90nm CMOS Device Technology ….
TSMC

TSMC Process	LP			G			HS		I/Os		
	Low-Vt	Std-Vt	High Vt	Low-Vt	Std-Vt	High Vt	Std-Vt	High-Vt			
V_{dd} (V)	1.2			1 (1.2)			1		1.8	2.5	3.3
T_{ox} (nm) [EOT]	22			16			<14		28	~53	~70
L_g (um)	80			65			45/50	50/55	145	265	365
I_{ds} (uA/um)	540/250	420/180	370/130	755/335	640/280	520/215	830/380	670/310	660/300	580/290	580/290
I_{off} (nA/um)	0.4	0.015	0.00[illegible]	50 (75)	5 (7.5)	1 (1.5)	75	10	<300	<300	<300
J_g (A/um^2)	100p/30p			2.4n/1n (6n/2.4n)			0.3-1u		<5p	<1f	<<1f
C_i (fF/um^2)	1.3/1.2			[illegible]							
Inverter delay (ps)	15	21	26	9.5 (8.4)	11.3 (9.5)	14.5(11.6)	7.9	10.5	<23	<32	<42

I_{ds} (off) = 50 nA/μm of gate length
I_g (leak) = 2.4nA/μm^2 of gate area (5A/cm^2 !)

[C.C. Wu et al., IEDM, San Francisco, 8-11 Dec. 2002]

Future Technologies

FinFET scaling to 10nm gate length
AMD

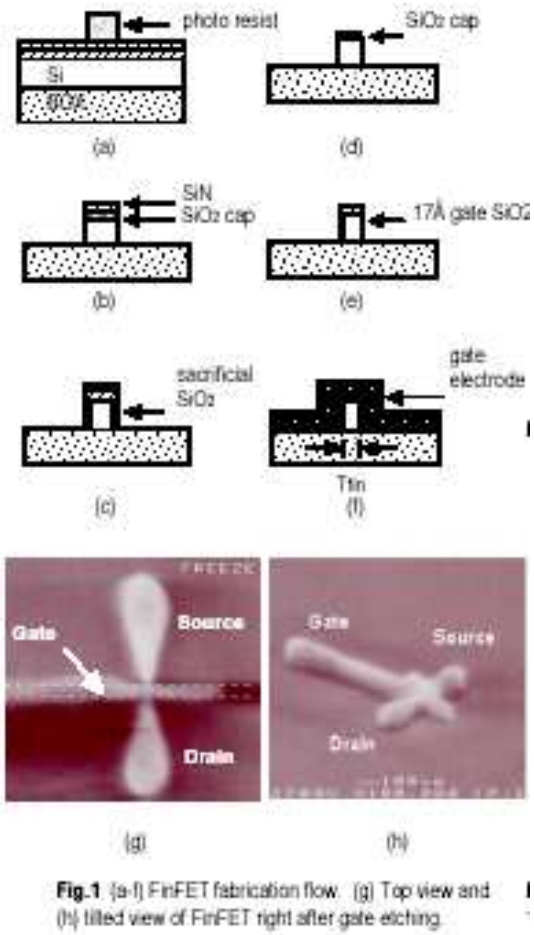


Fig.1 (a-f) FinFET fabrication flow. (g) Top view and (h) tilted view of FinFET right after gate etching.

[Ben Yu et al., IEDM, San Francisco, 8-11 Dec. 2002]

Future Technologies - 2

Charge trapping in high-k dielectric stacks
IBM

Radiation hardness!

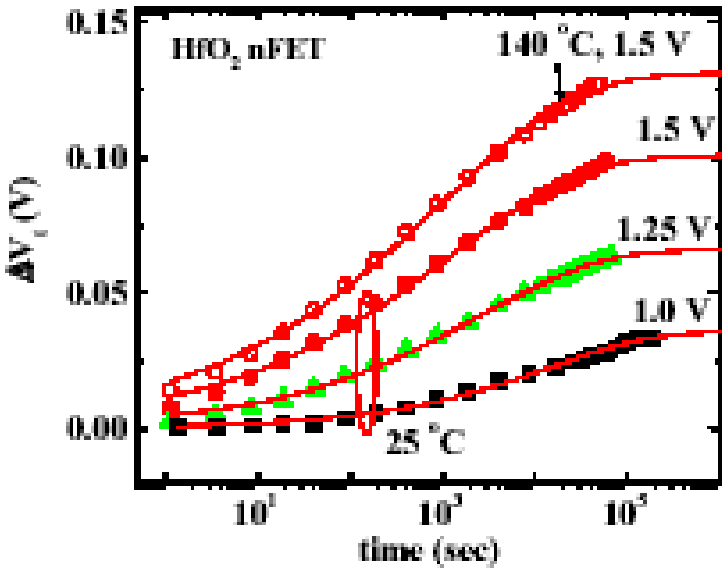
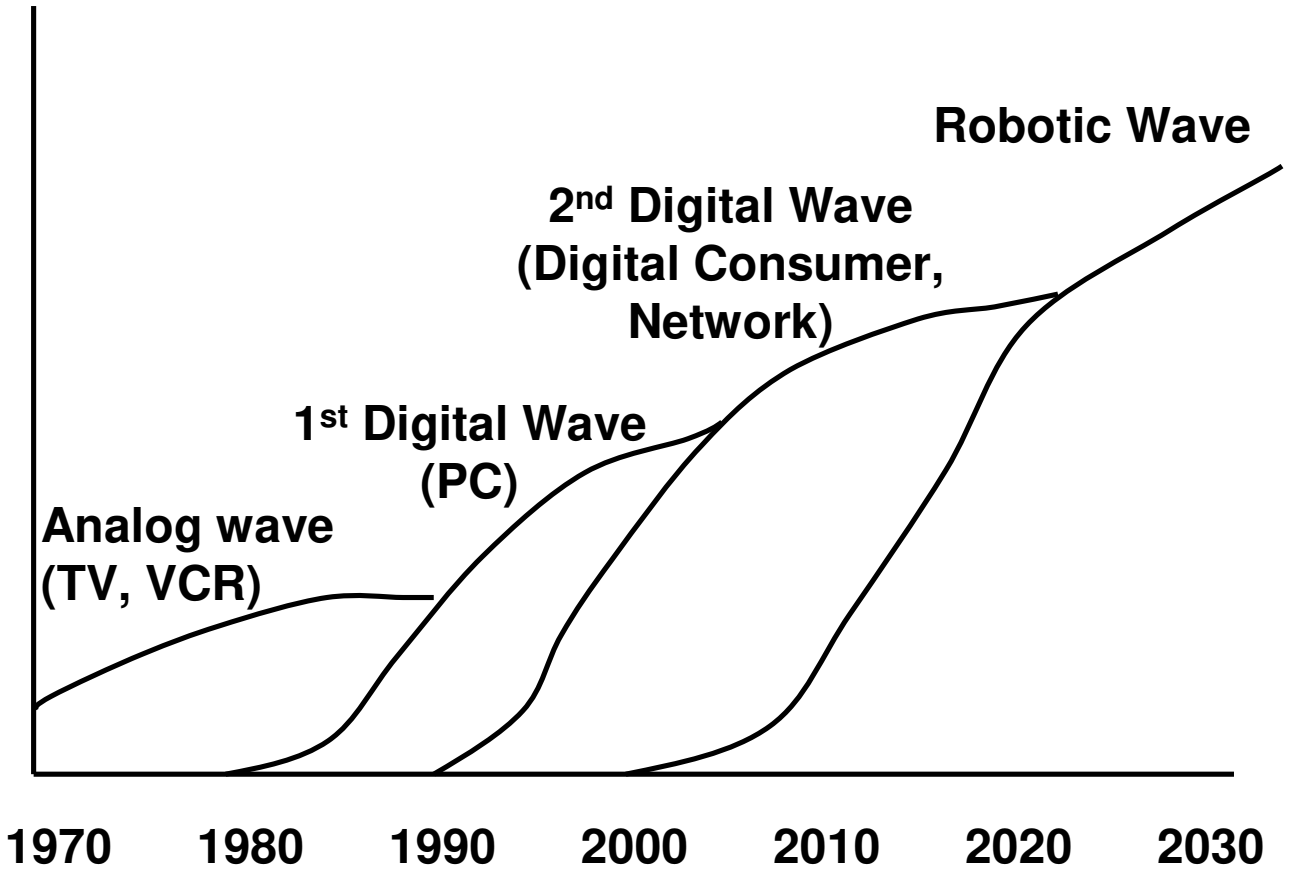


Fig 6: Dependence of measured ΔV_t (symbols) on total stress time for various V_g and temperatures (25 °C,140 °C) for HfO_2 nFET; solid lines are the model calculations.

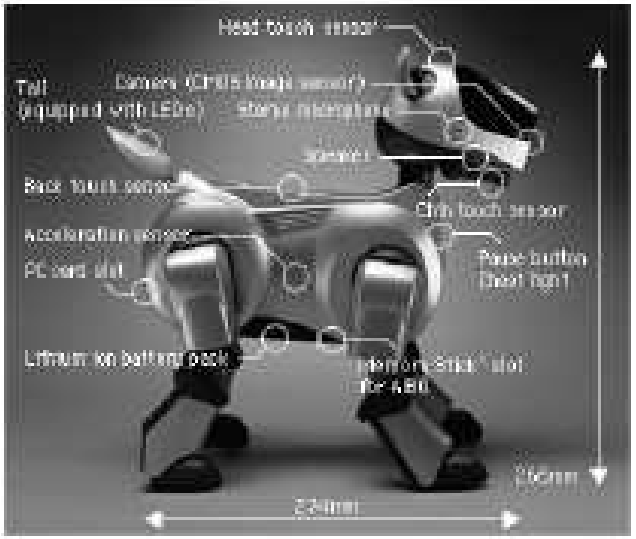
The Sony Motivation



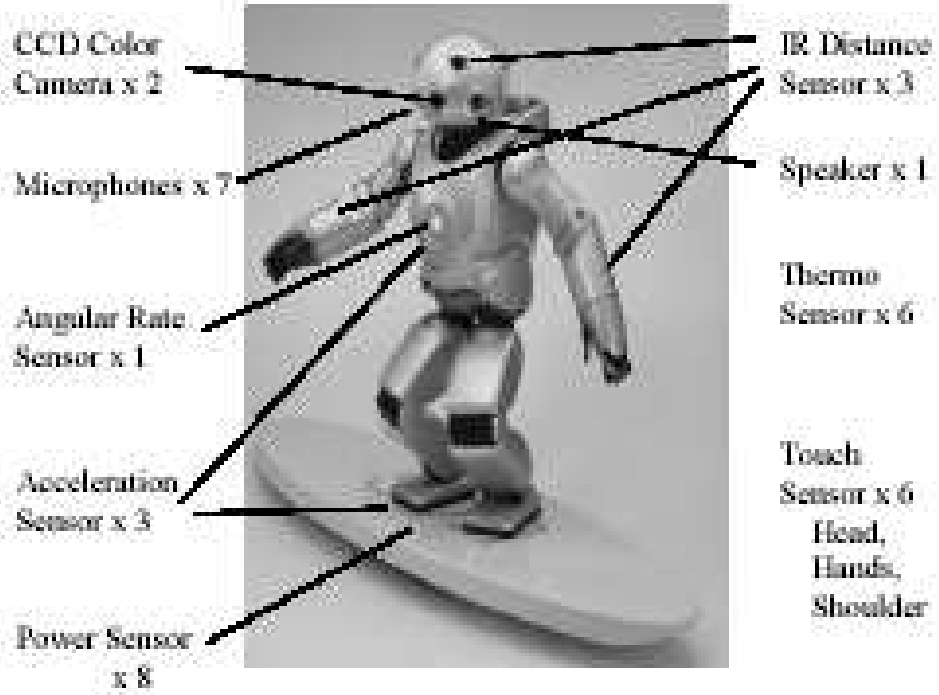
[T. Kamimoto and T.T.Doi, IEDM, San Francisco, 8-11 Dec. 2002 (next 3 slides)]

Technology drivers

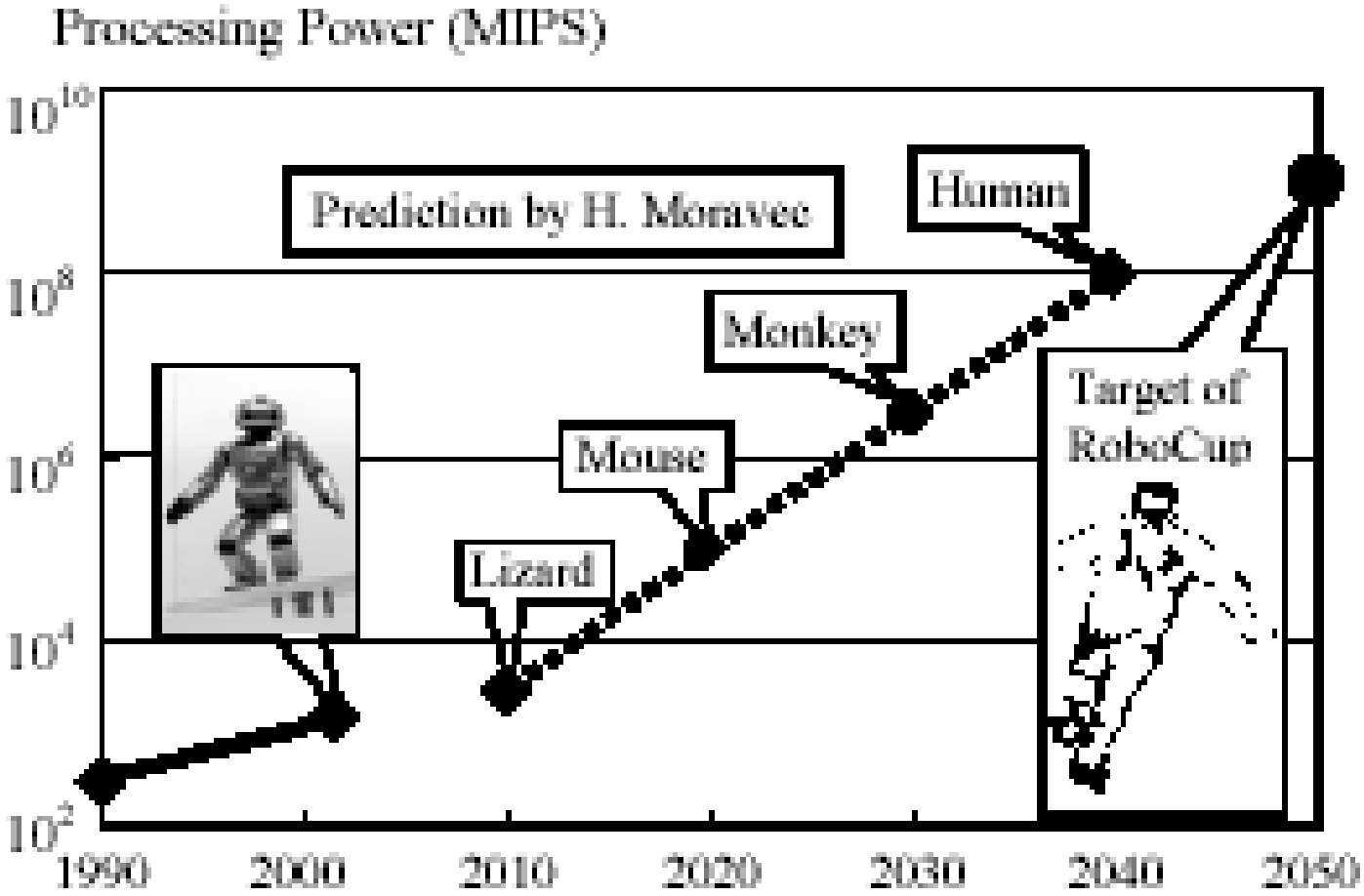
IABO



SDR-4X



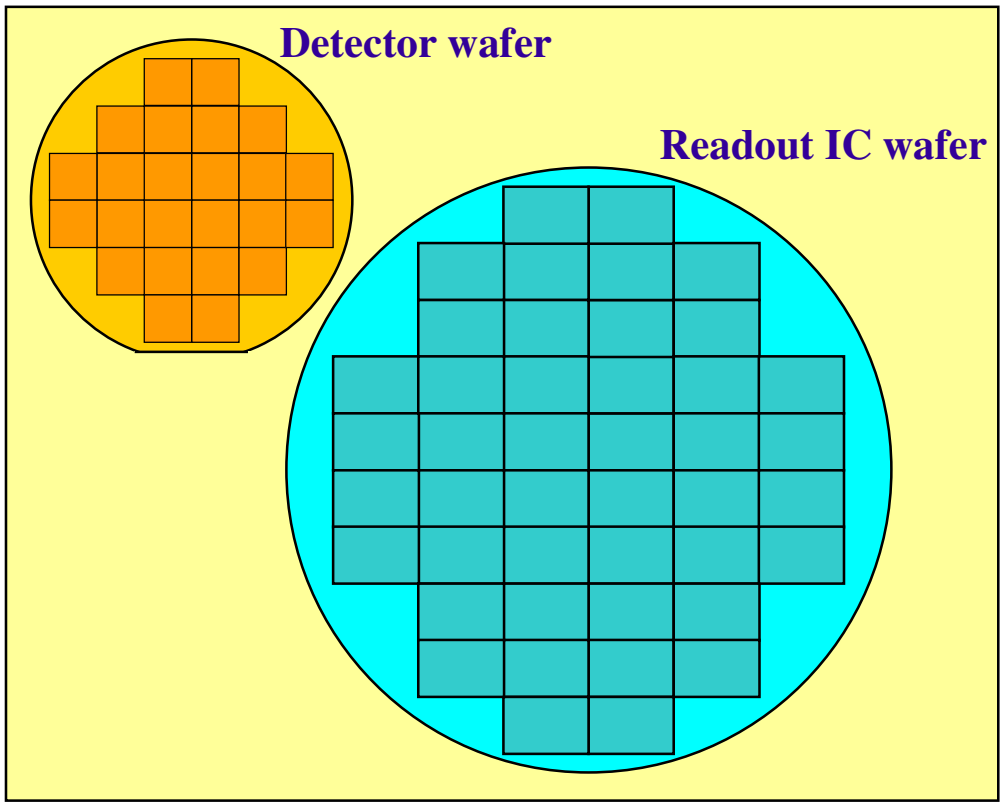
The Sony Vision



A team of Sony robots should beat the football World Cup champions in 2050….

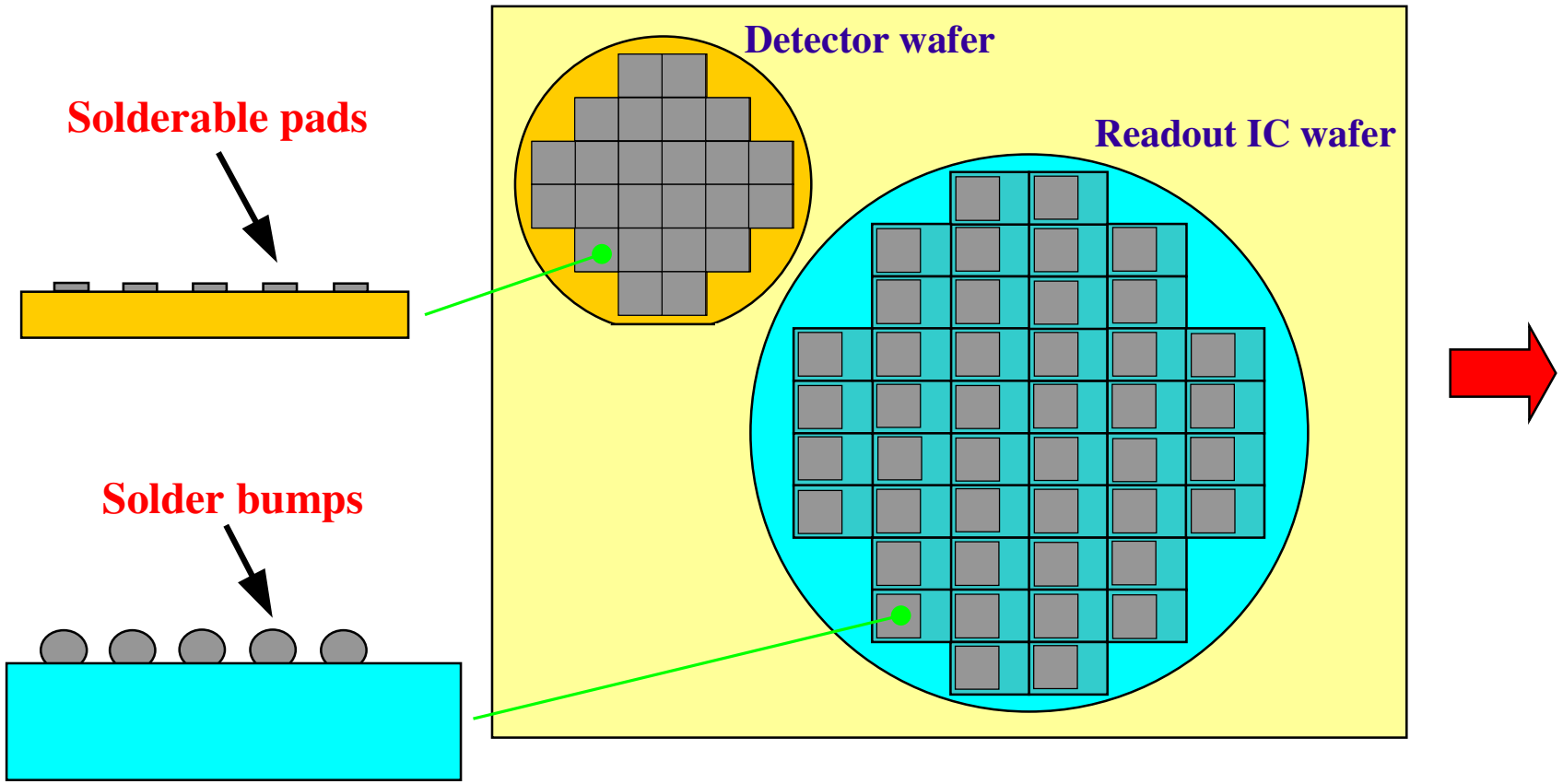
Flip chip technology

Detector & Readout wafers

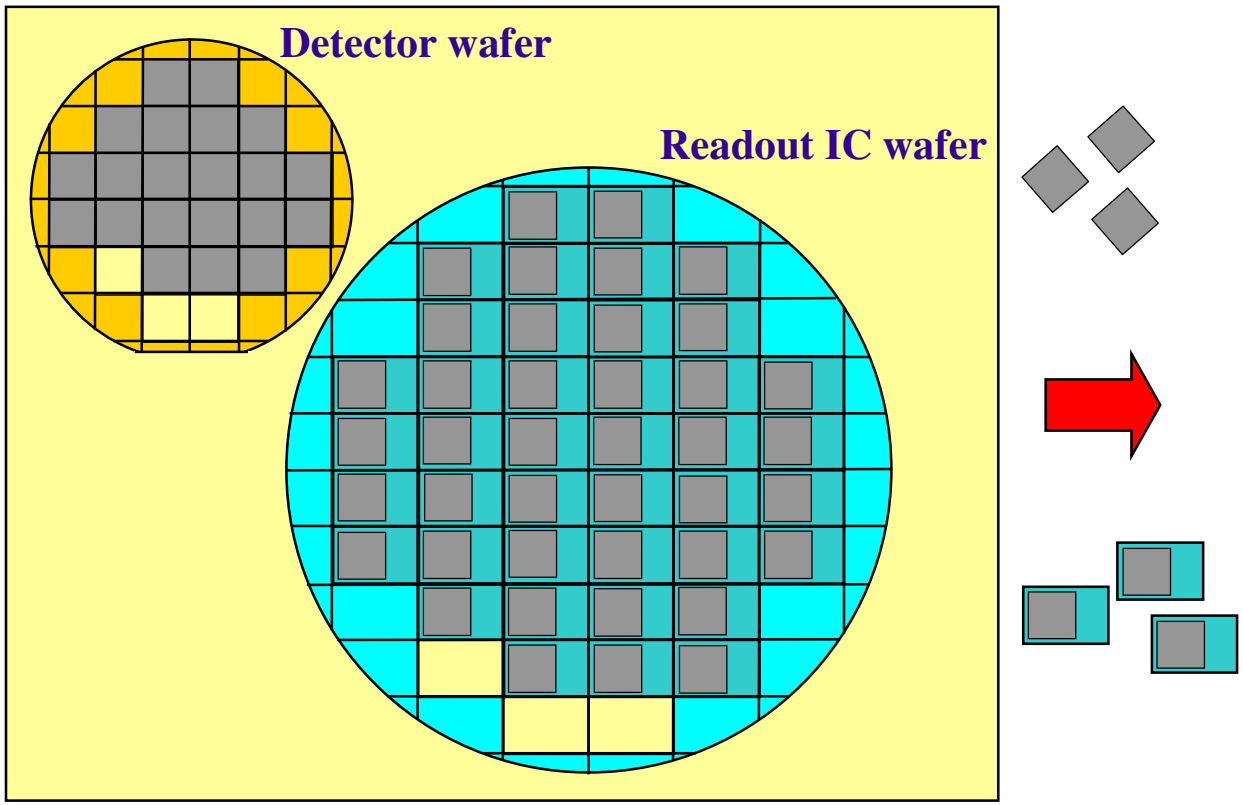


[Slides courtesy of J. Salmi, VTT, Finland]

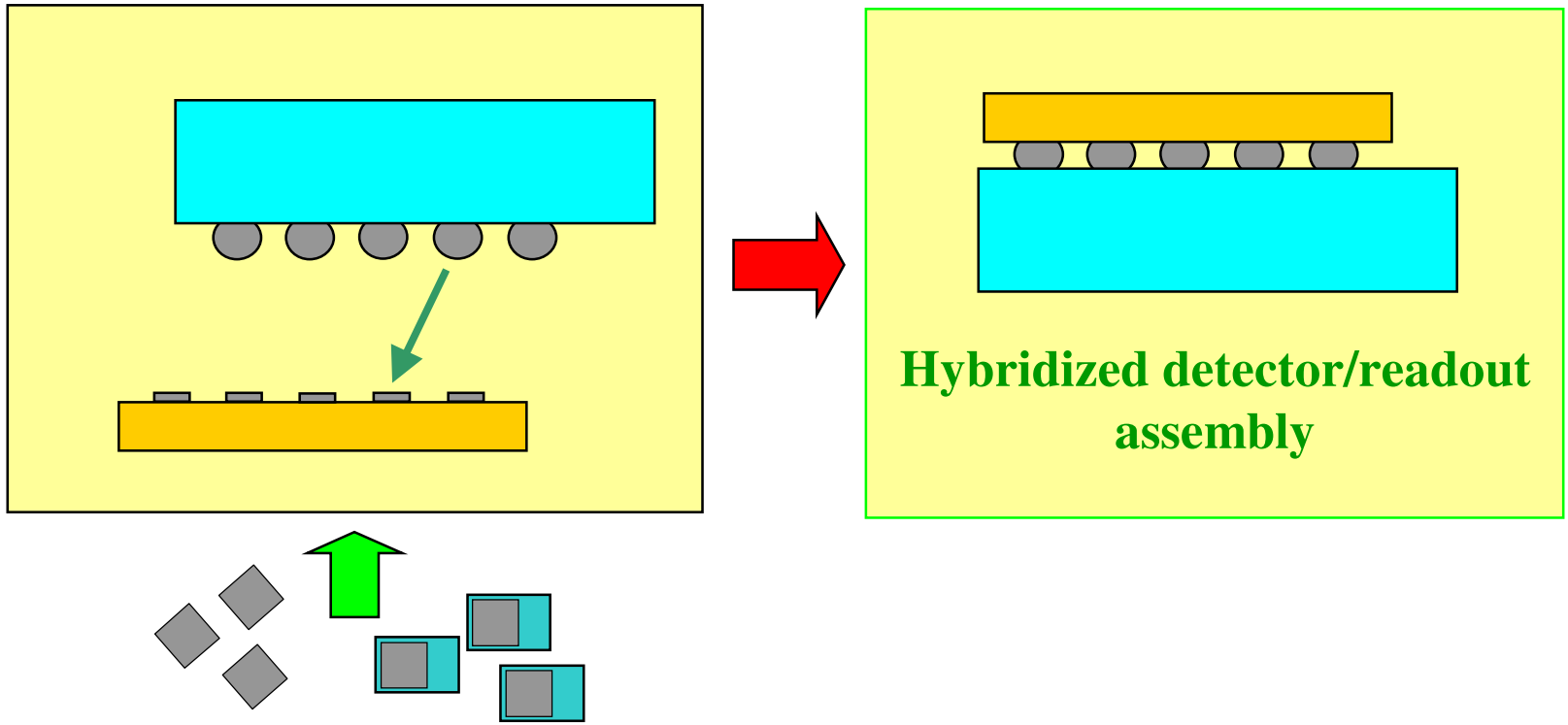
Bumping process (at wafer level)



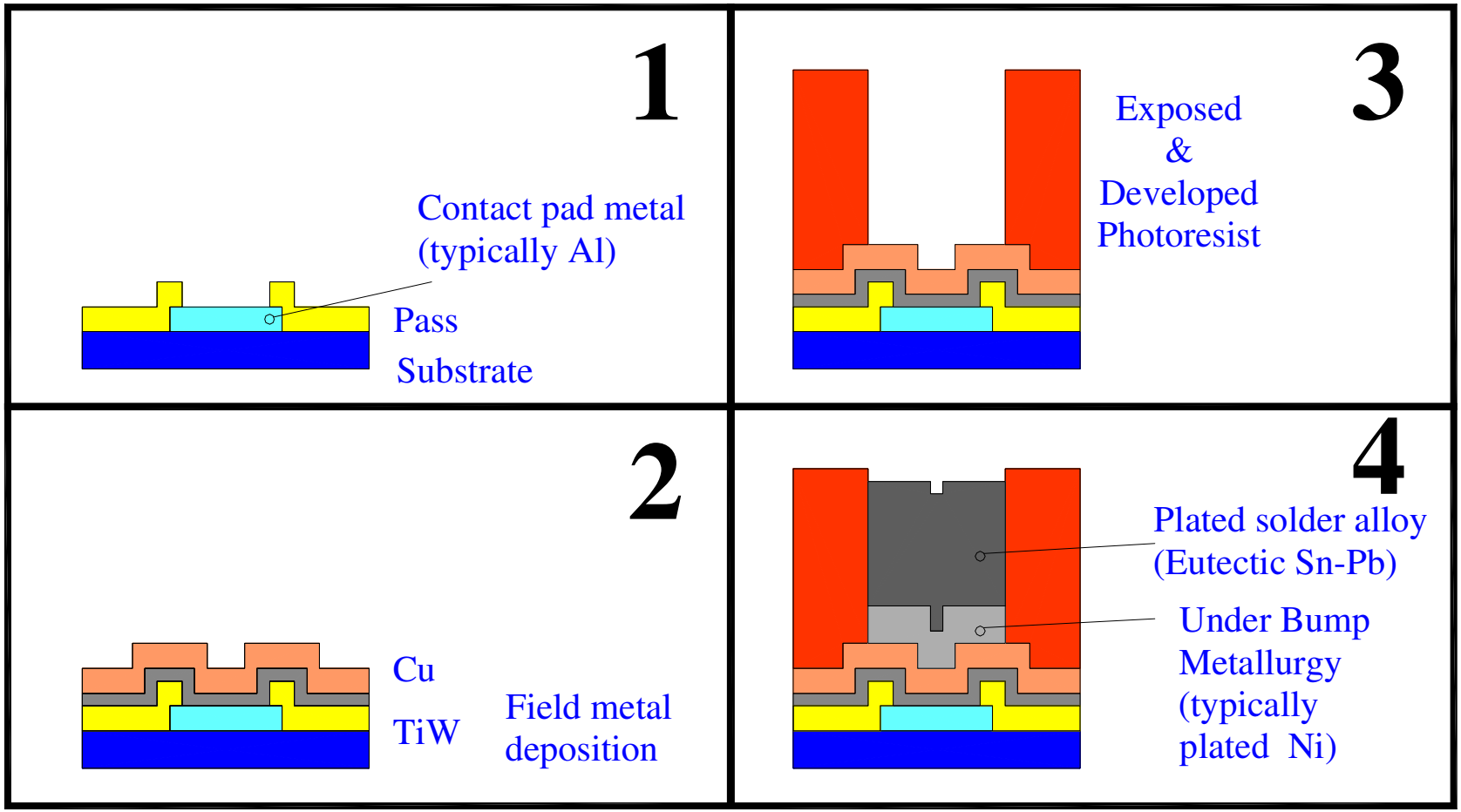
Dicing & chip pick-up



Flip chip bonding (chip-by-chip)

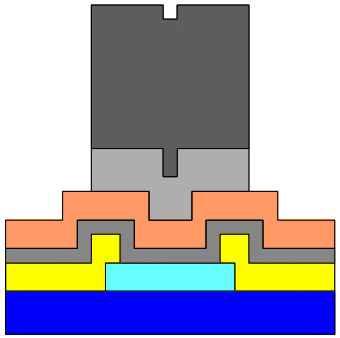


Bumping Process



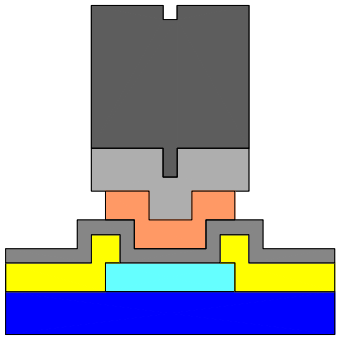
Bumping Process [cont'd]

5



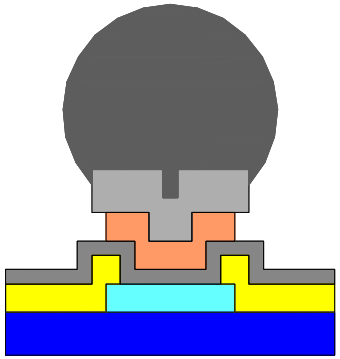
After photoresist stripping

6



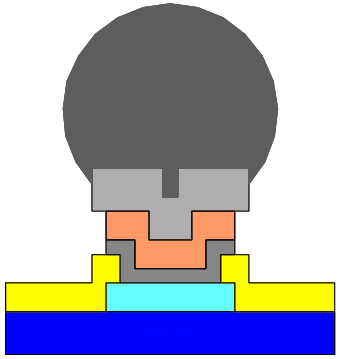
Wet etching of field metal Cu

7



Solder reflow

8

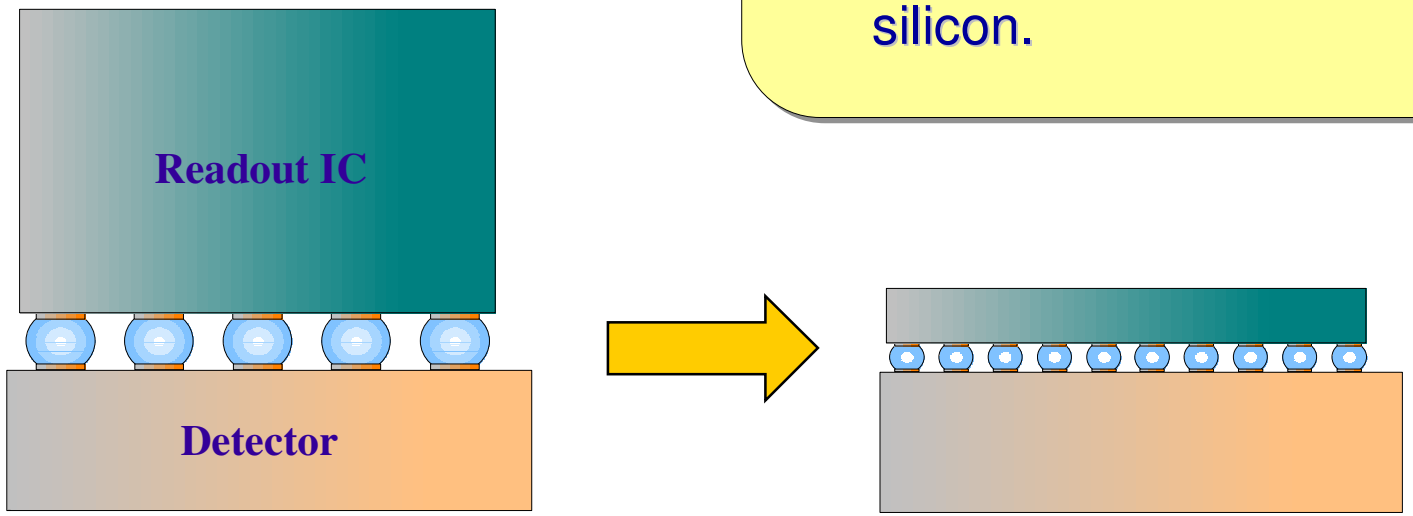


Wet etching of field metal TiW

Wafer Thinning

MOTIVATION

- Low profile assemblies.
- Low mass assemblies to minimize radiation interaction with asic's bulk silicon.



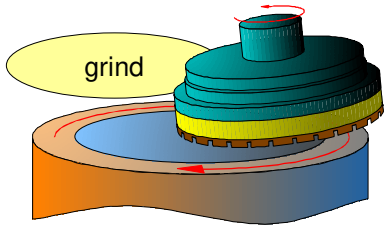
Thinning Process

Thinning is preferably done after bumping but before dicing and assembly.

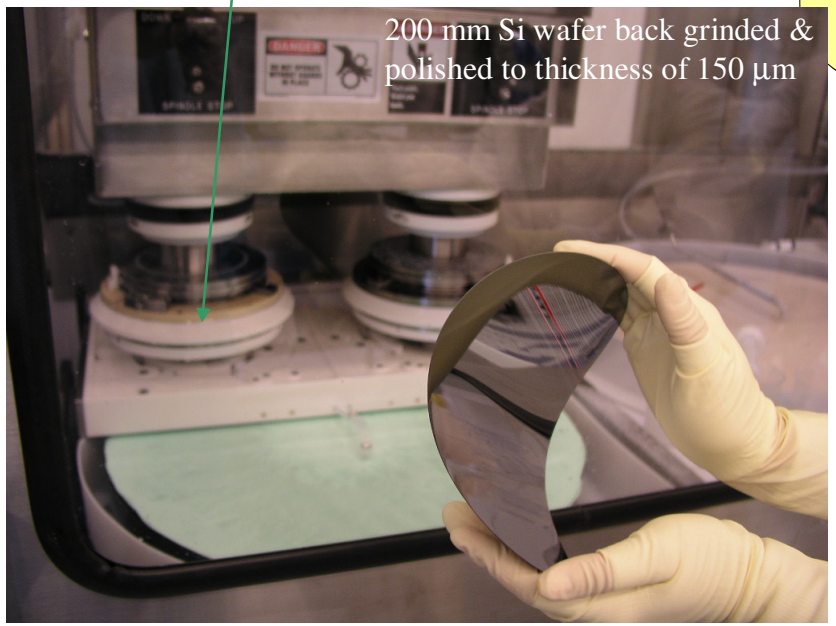
PROCESS STEPS

- Front side protection/planarization: UV-curable back grinding tape laminated on bumped wafer.
- Back grinding using diamond wheels with two different grit sizes (coarse + fine).
- Defect layer left by mechanical grinding is removed by wet chemical etching or CMP (Chemical Mechanical Polishing).
- Protective tape is UV-exposed and delaminated.

Strasbaugh 7AF Intelligent Grinder



Thinning Process [cont'd]

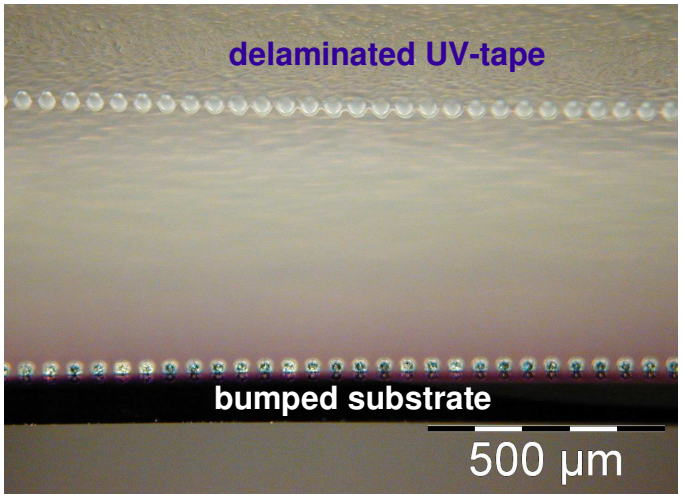


Strasbaugh 6DS-SP CMP System

NOTES

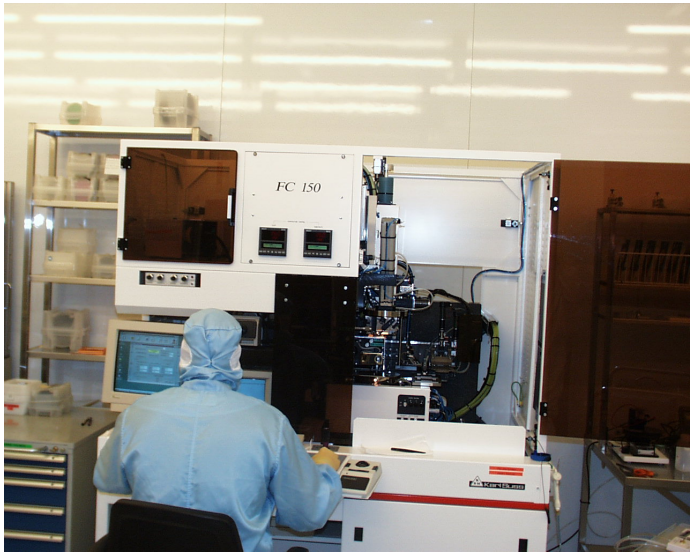
- Thickness down to 150 µm (200-mm/8" wafers).
- Total thickness variation (TTV) with protective tape < 5 µm over wafer.
- Post-grinding defect layer removal improves mechanical strength of die.

Delamination of back grinding tape

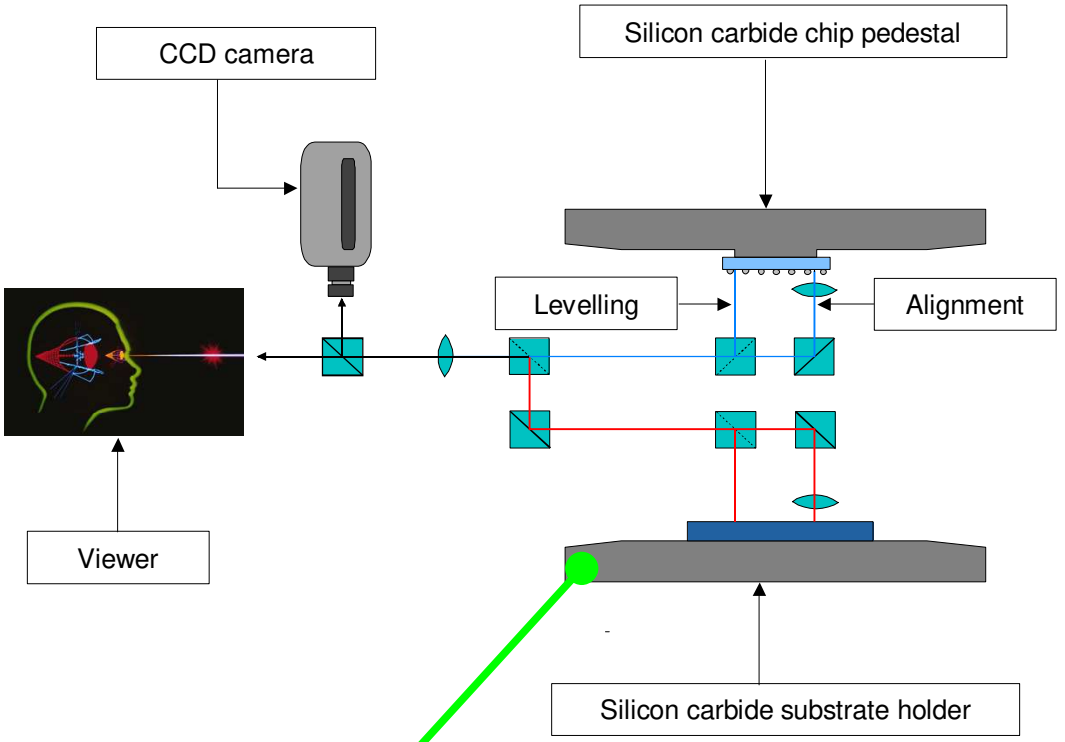


Flip Chip Bonding

Flip chip assembly is done in a Class-10 clean room.



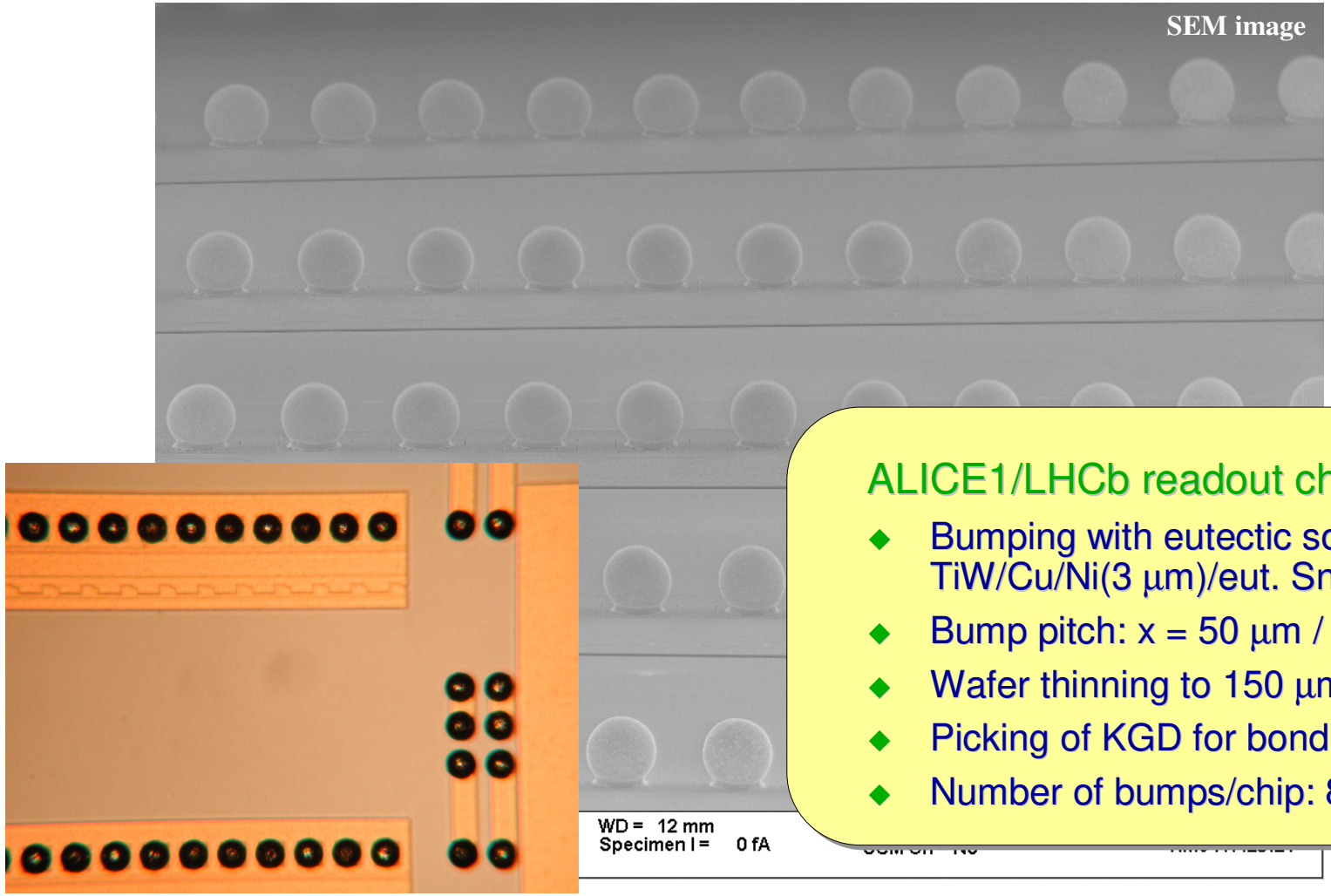
Suss MicroTec FC150 Flip Chip Bonder with both Universal and Solder Reflow Bonding Arms.



Custom SiC tools needed for readout & detector chip!

Readout Bumping & Thinning

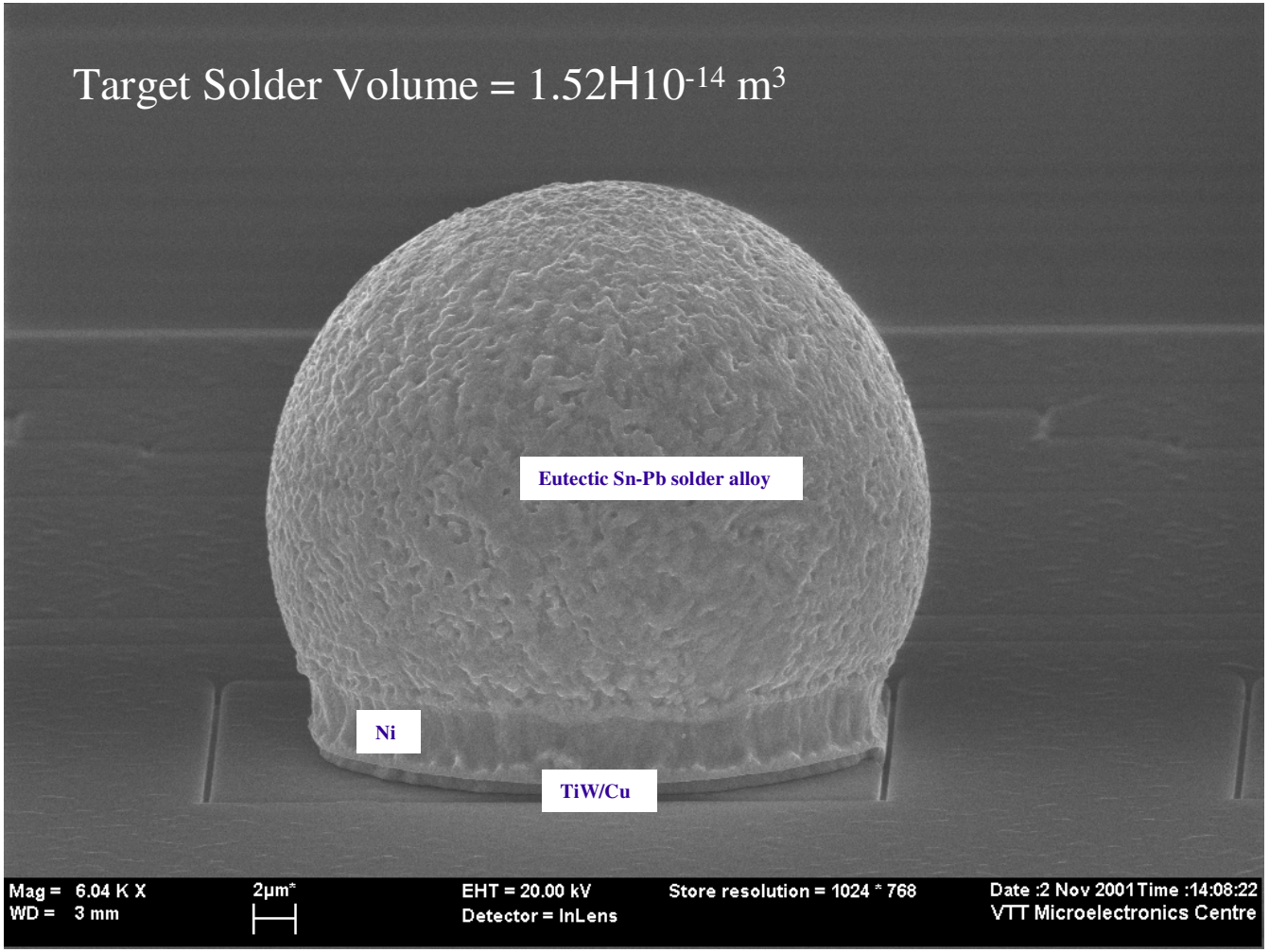
1. Readout process



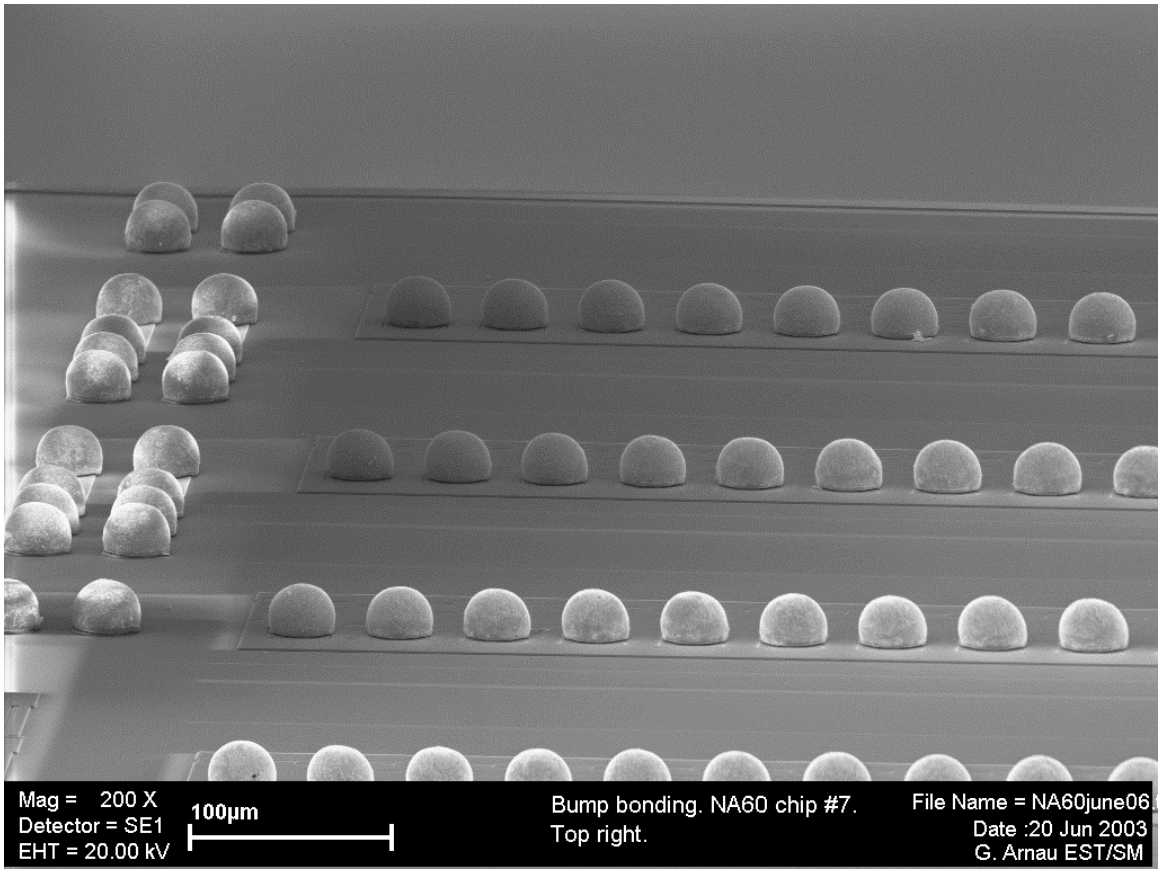
ALICE1/LHCb readout chip process

- Bumping with eutectic solder: TiW/Cu/Ni(3 µm)/eut. Sn-Pb(13 µm).
- Bump pitch: x = 50 µm / y = 400 µm .
- Wafer thinning to 150 µm.
- Picking of KGD for bonding.
- Number of bumps/chip: 8,192.

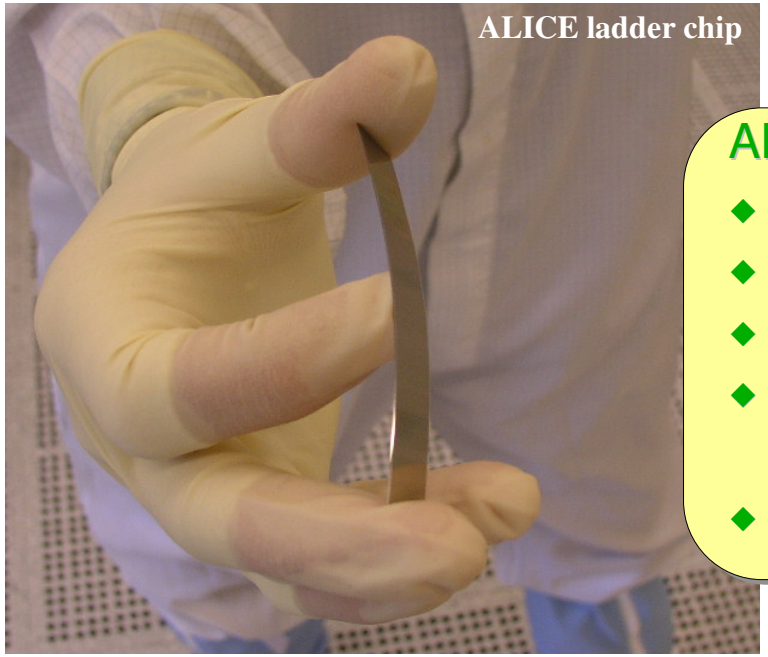
Solder Bump on ALICE1/LHCb Readout Chip After Reflow



Solder Bumps on Alice Pixel Chip



ALICE 'Ladder' Detector



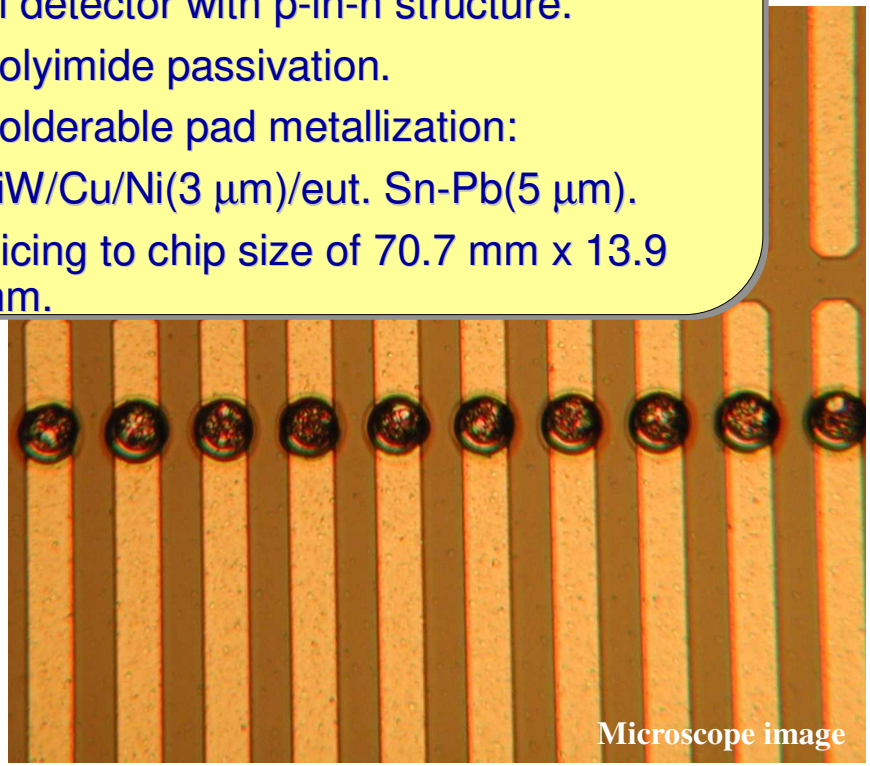
2. Detector process

ALICE detector chip process

- Detector wafer size 125 mm x 200 µm.
- Si detector with p-in-n structure.
- Polyimide passivation.
- Solderable pad metallization: TiW/Cu/Ni(3 µm)/eut. Sn-Pb(5 µm).
- Dicing to chip size of 70.7 mm x 13.9 mm.

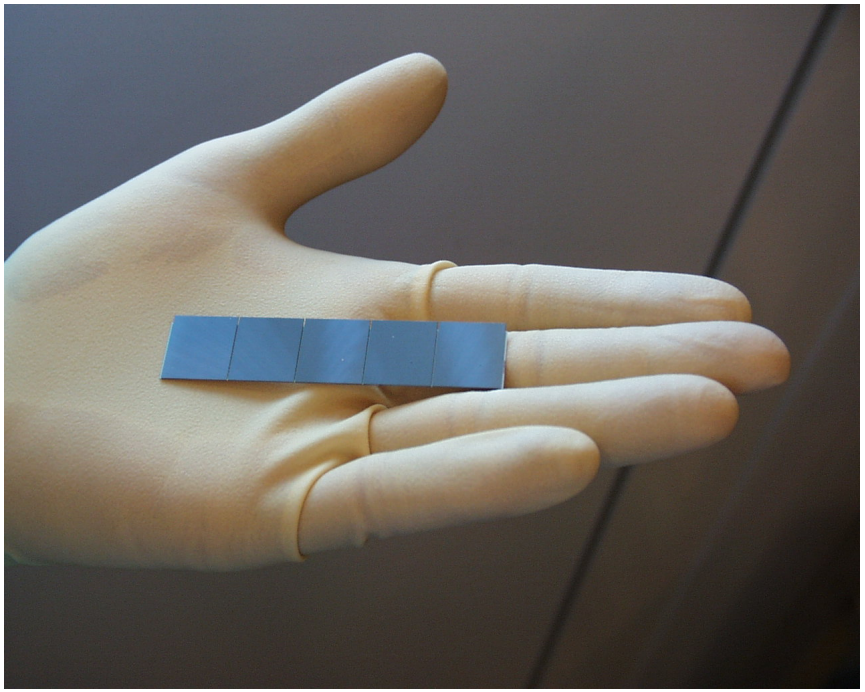
COMMENT

- During solderable pad process a temporary passivation layer is used at back side of detector wafer to protect Al contact layer.



Bonded ALICE 'Ladder' Assembly

3. Flip chip bonding



Hybridized ALICE assembly

- Five ALICE1/LHCb readout chips flip chip bonded on ALICE1 detector ladder chip.
- Assembly reflow using formic acid oven.
- Chip-to-substrate distance: 20 μm.
- Total number of bumps/assembly: 40,960.

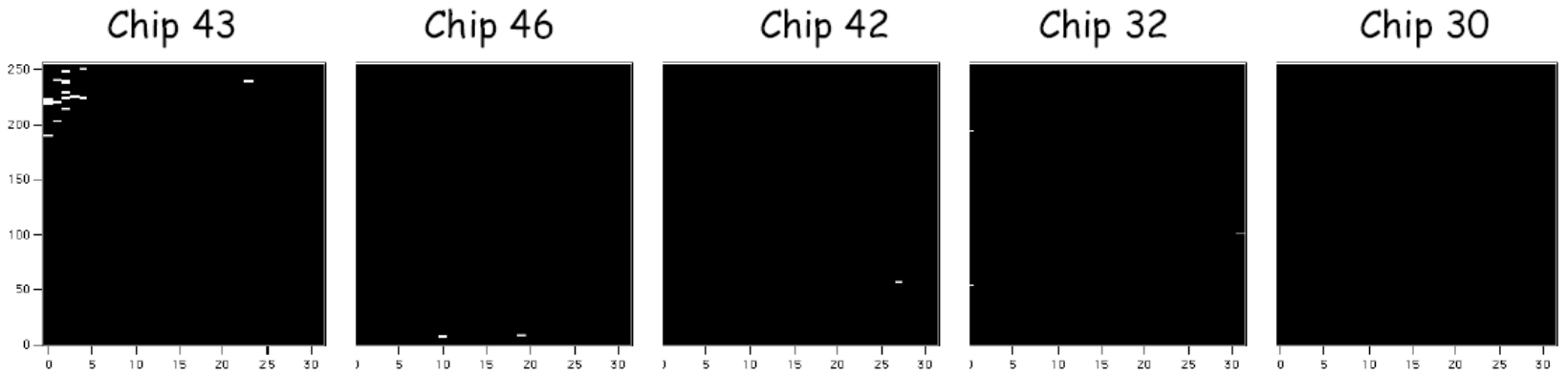
Yield Figures of ALICE 'Ladder' Assembly

COMMENT

- CERN defines 'Class 1' ROC's (as tested *before* bumping) as those with fewer than 82 (*i.e.*, less than 1 per cent) dead pixels.

Sr-Measurements :

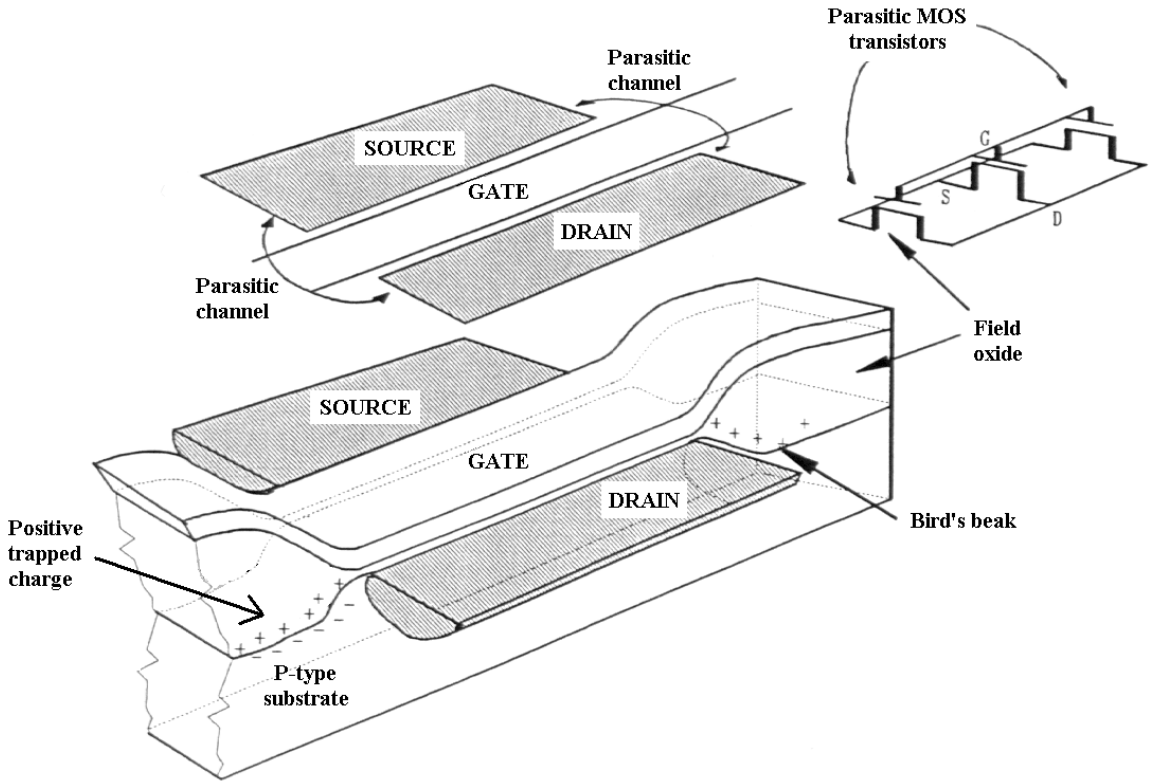
	Chip43	Chip46	Chip42	Chip32	Chip30
Working pixels	99.7%	99.95%	99.98%	99.98%	100%
Missing pixels	28	4	2	2	0



HEP specific challenge – radiation tolerance

- The LHC vertex detectors are expected to receive 10 s of MRad over the machine running time
- Two alternatives were available in the mid 1990's
  - Military radiation hard BiCMOS
  - Use of Deep Submicron CMOS
- Since then deep sub micron has been almost universally adopted for economic reasons
- How was this achieved?

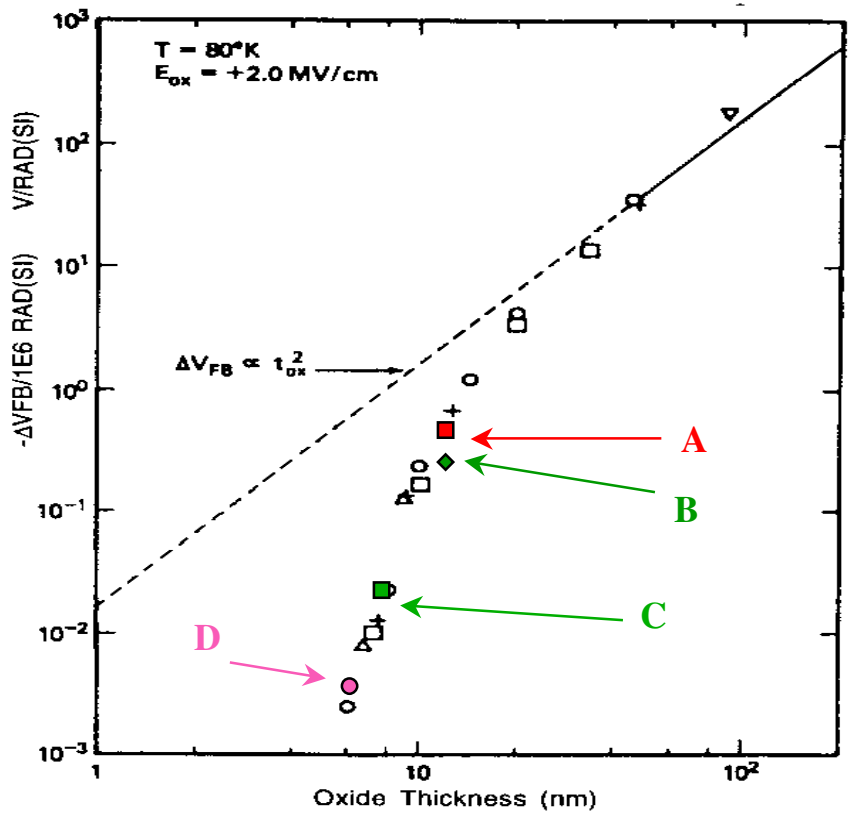
Effect of ionizing radiation on CMOS transistors - total dose



R. Gaillard,J.-L.Leray, O.Musseau, "Techniques de durcissement des composants, circuits et systemes electroniques,"Notes of the short course of the 3rd European Conference on Radiation and its Effects on Components and Systems, Arcachon (France), Sept. 1995.

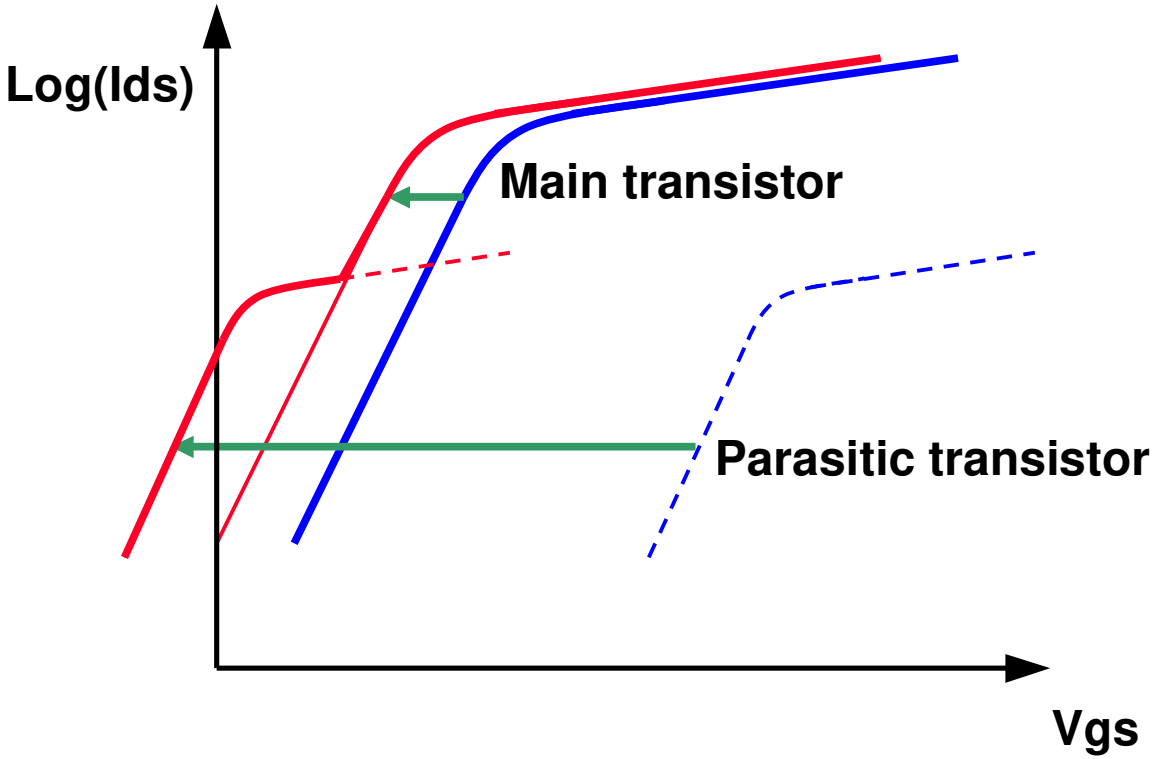
MOS Flatband voltage shift versus gate oxide thickness after 1MRad(Si) @ 80°K

- Tunneling of trapped charge in thin oxides
- $\Delta VT \sim 1/tox^2$ for tox > 10nm
- $\Delta VT \sim 1/tox^3$ for tox < 10 nm



After N.S. Saks, M.G. Ancona, and J.A. Modolo, IEEE Trans.Nucl.Sci., Vol. NS-31 (1984) 1249

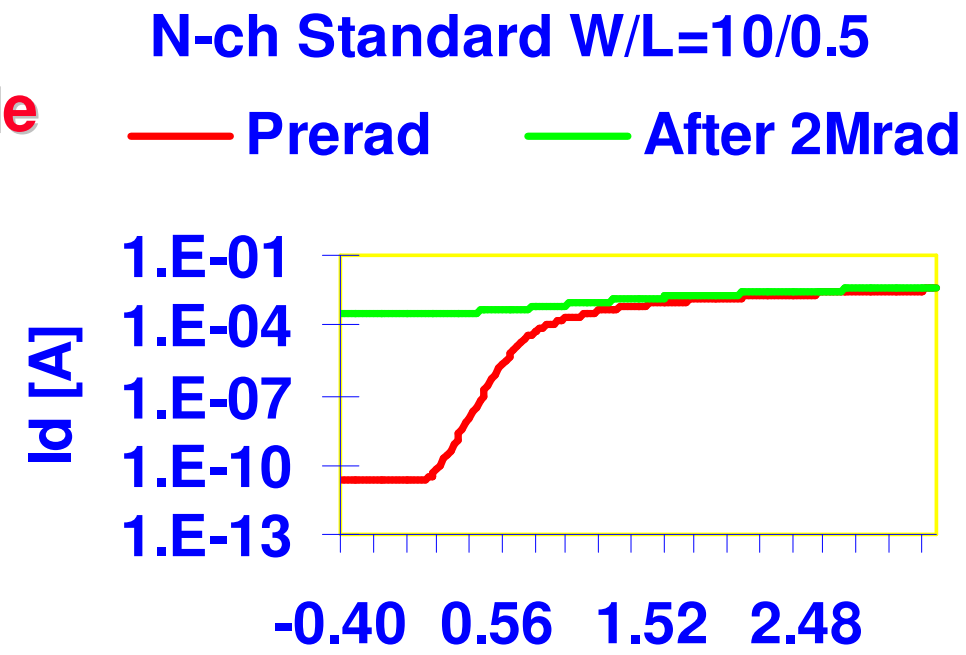
I-V Characteristics of the regular NMOS pre and post rad.



Parasitic Vt shift leads to leakage current - transistor fails

Total ionizing irradiation dose problem in commercial CMOS

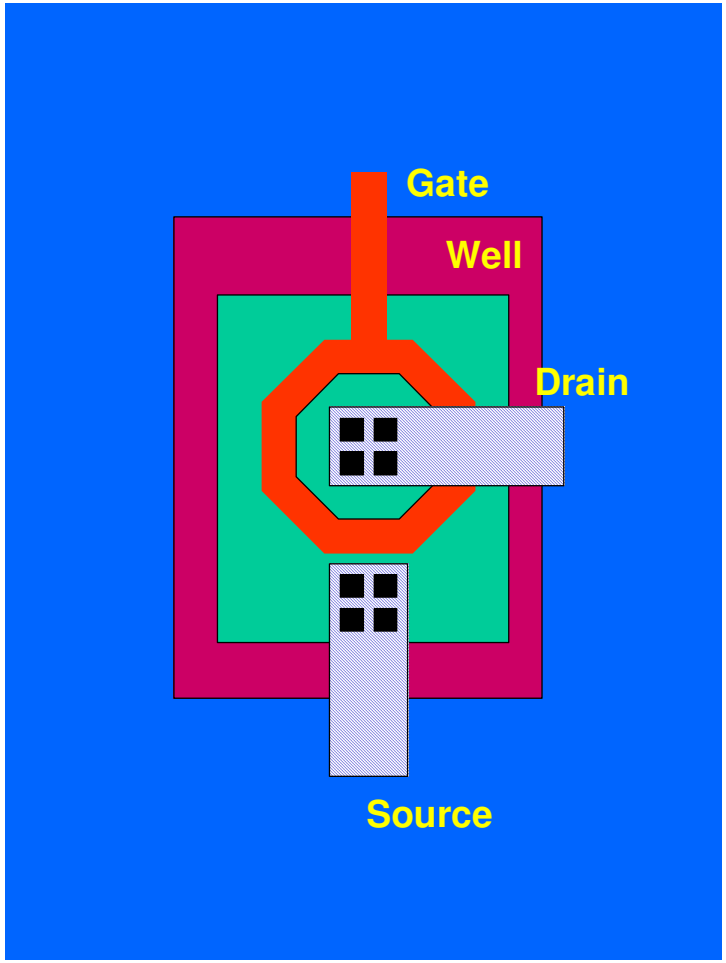
- Radiation induces positive fixed oxide charge and interface states
- Vt - shift
- weak inversion slope change
- mobility change
- LEAKAGE in NMOS transistors

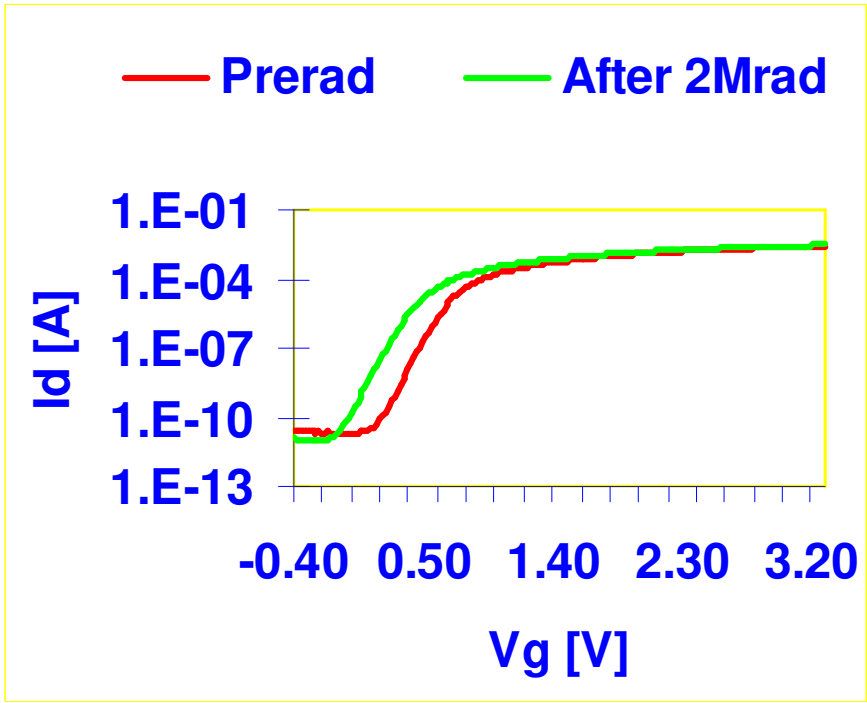


Example from 0.5 μm technology (tox ~ 10 nm)

NMOS TRANSISTOR LEAKAGE

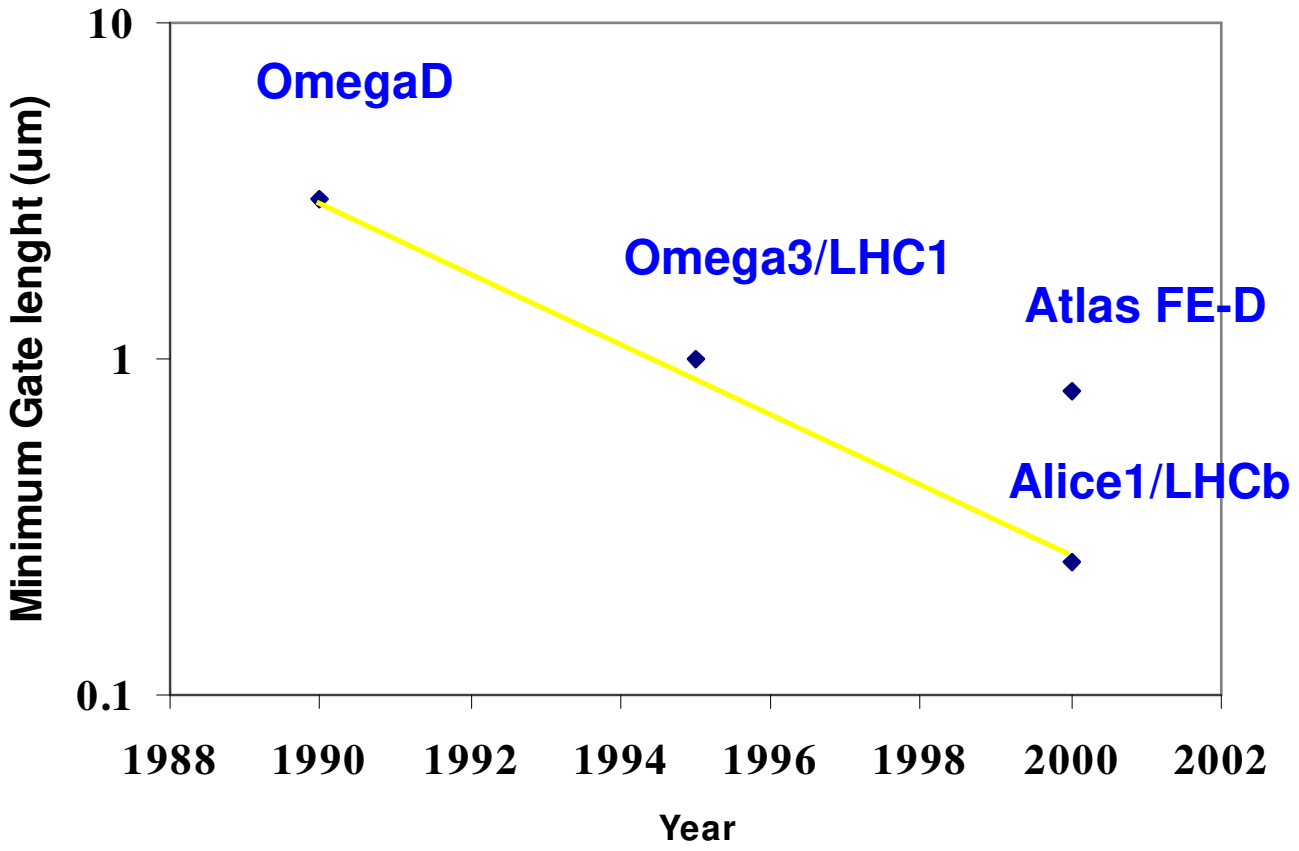
ENCLOSED TRANSISTOR LAYOUT



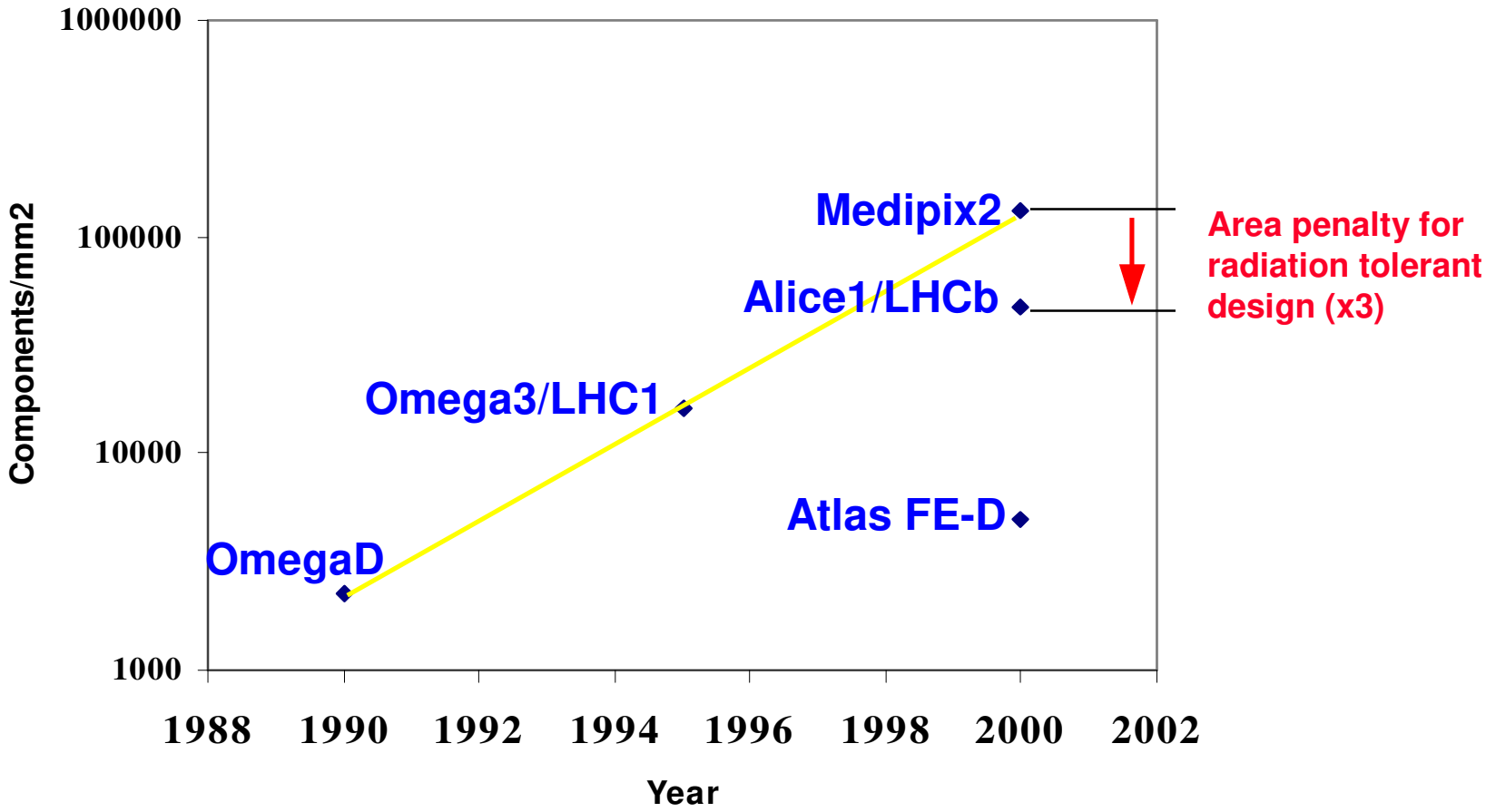


0.5um Technology (tox = 10nm)

Pixel readout chips – technology trends

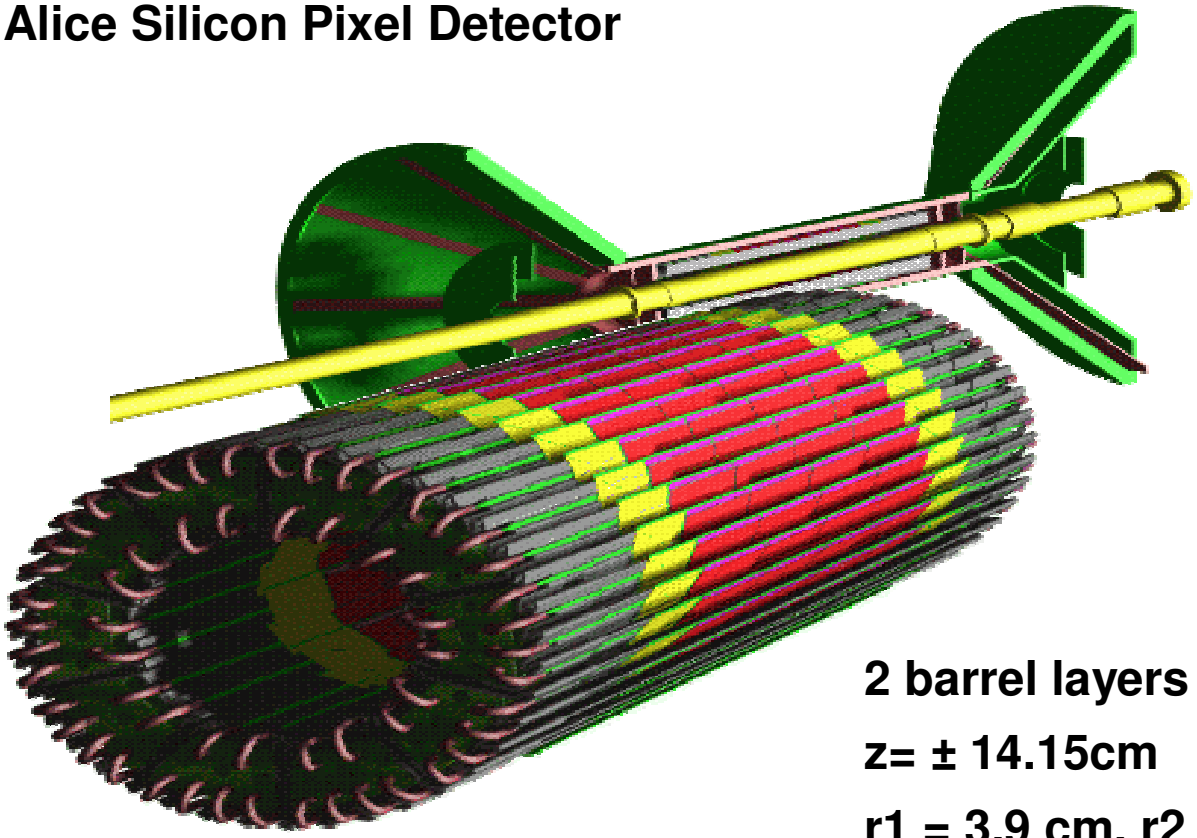


Pixel readout chips- component density



An LHC detector using Deep Sub Micron CMOS and state-of-the-art packaging

The Alice Silicon Pixel Detector

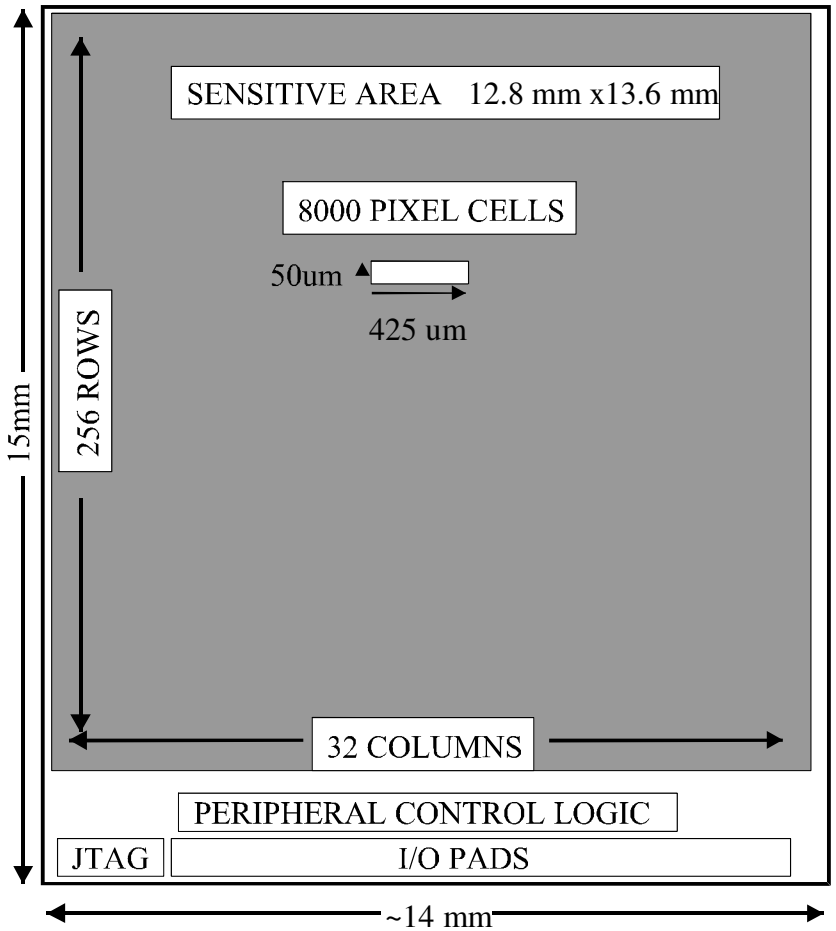


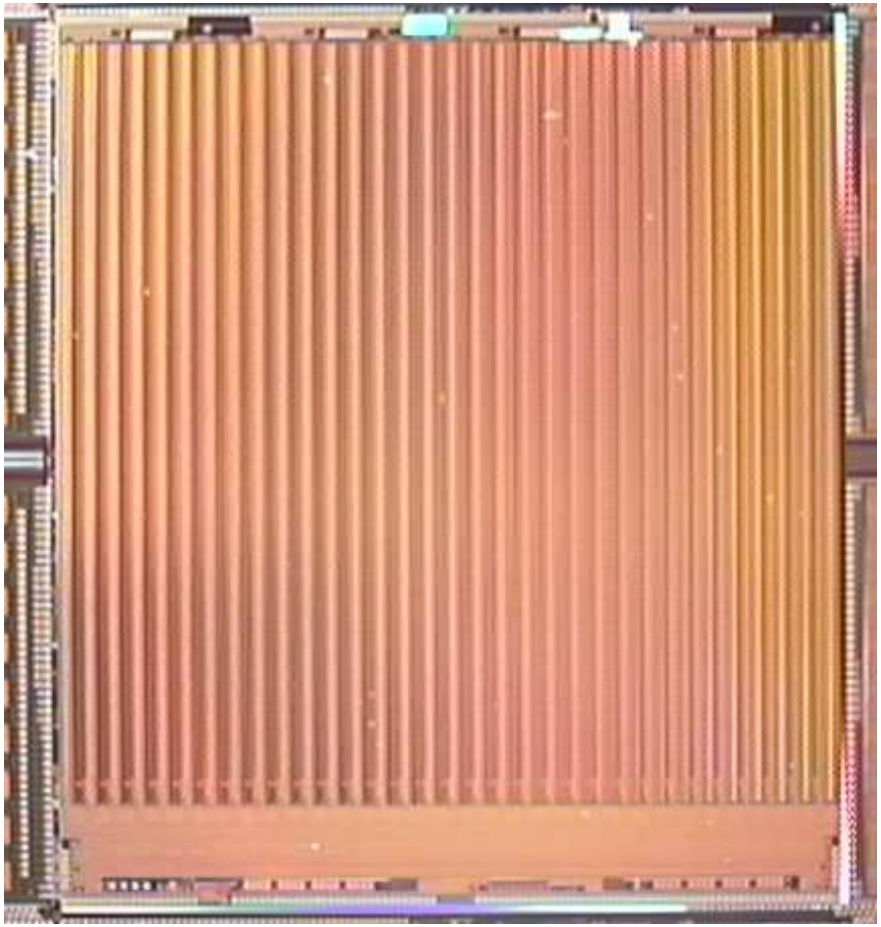
2 barrel layers

z= ± 14.15cm

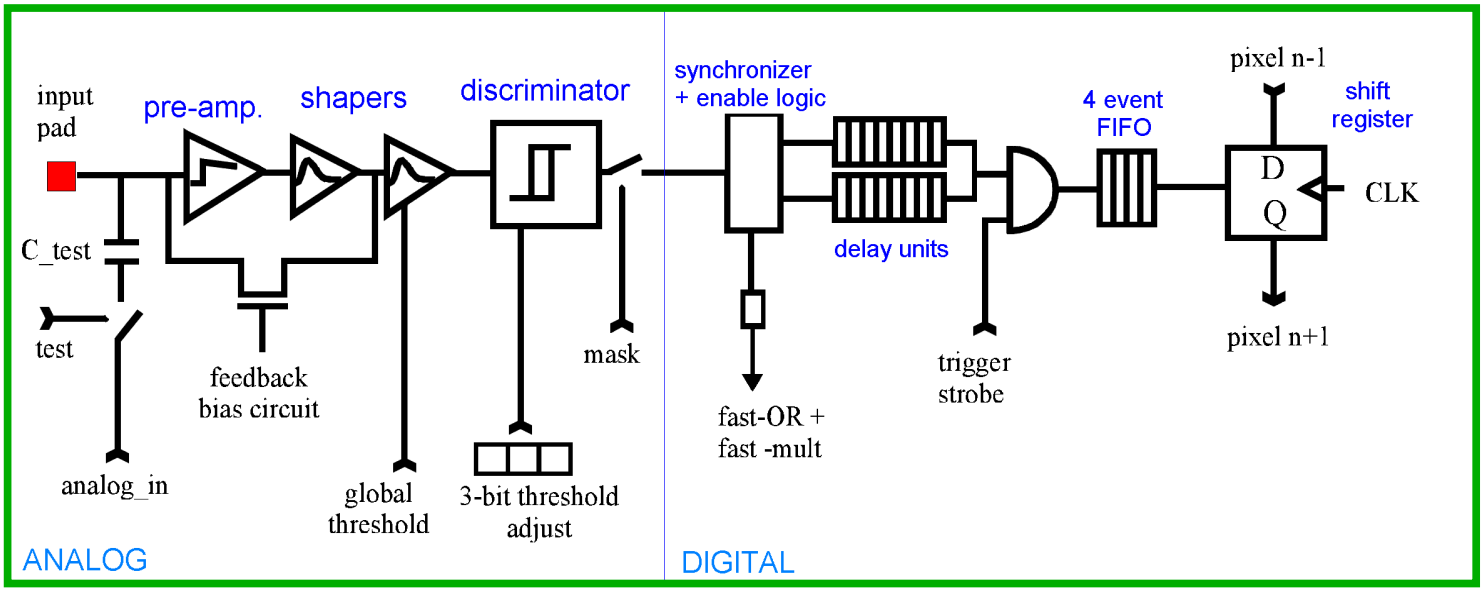
r1 = 3.9 cm, r2 = 7.6 cm

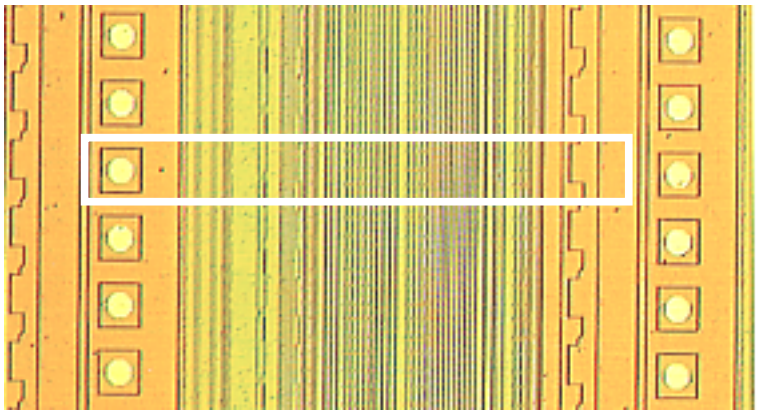
The Alice1LHCb readout chip





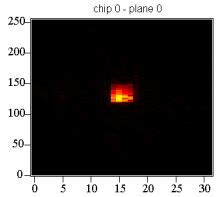
The Alice1LHCb pixel cell

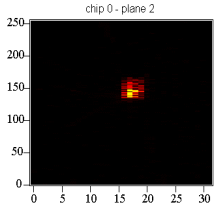




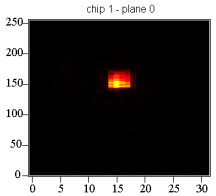
25ns shaping time
50μm x 425μm
Radiation tolerant design
500 transistors per pixel
~ 100μW per pixel

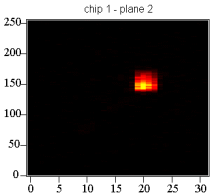
SPD test beam

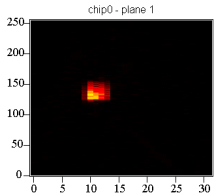




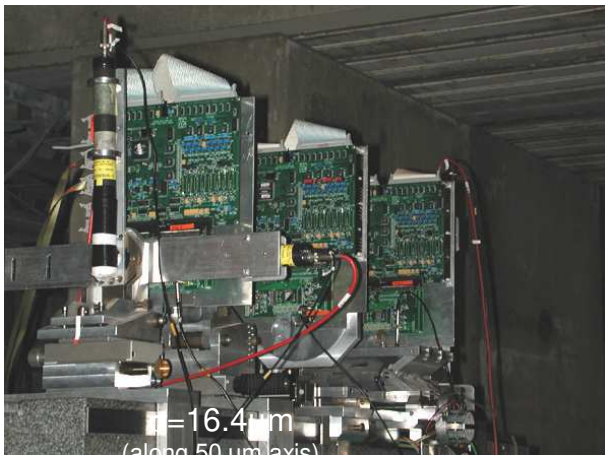
singles



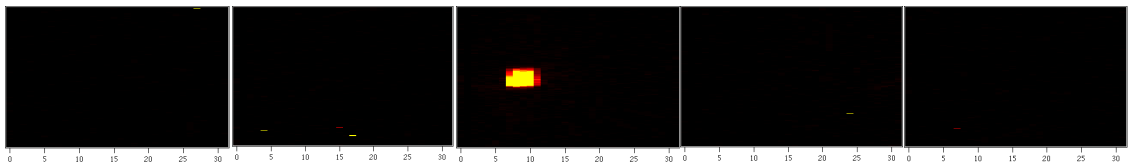




July 2002, CERN-SPS H4 beam

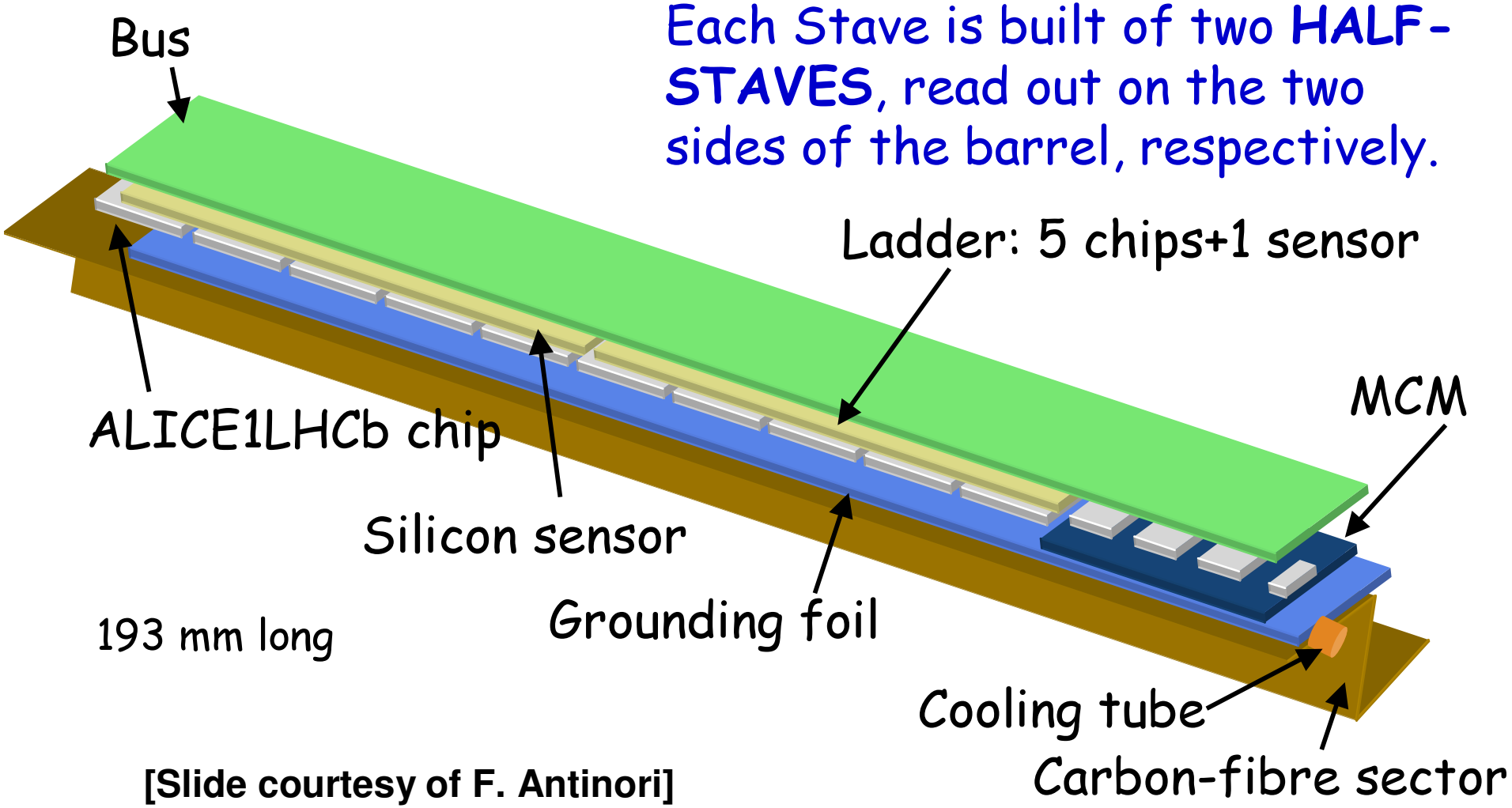


ladder



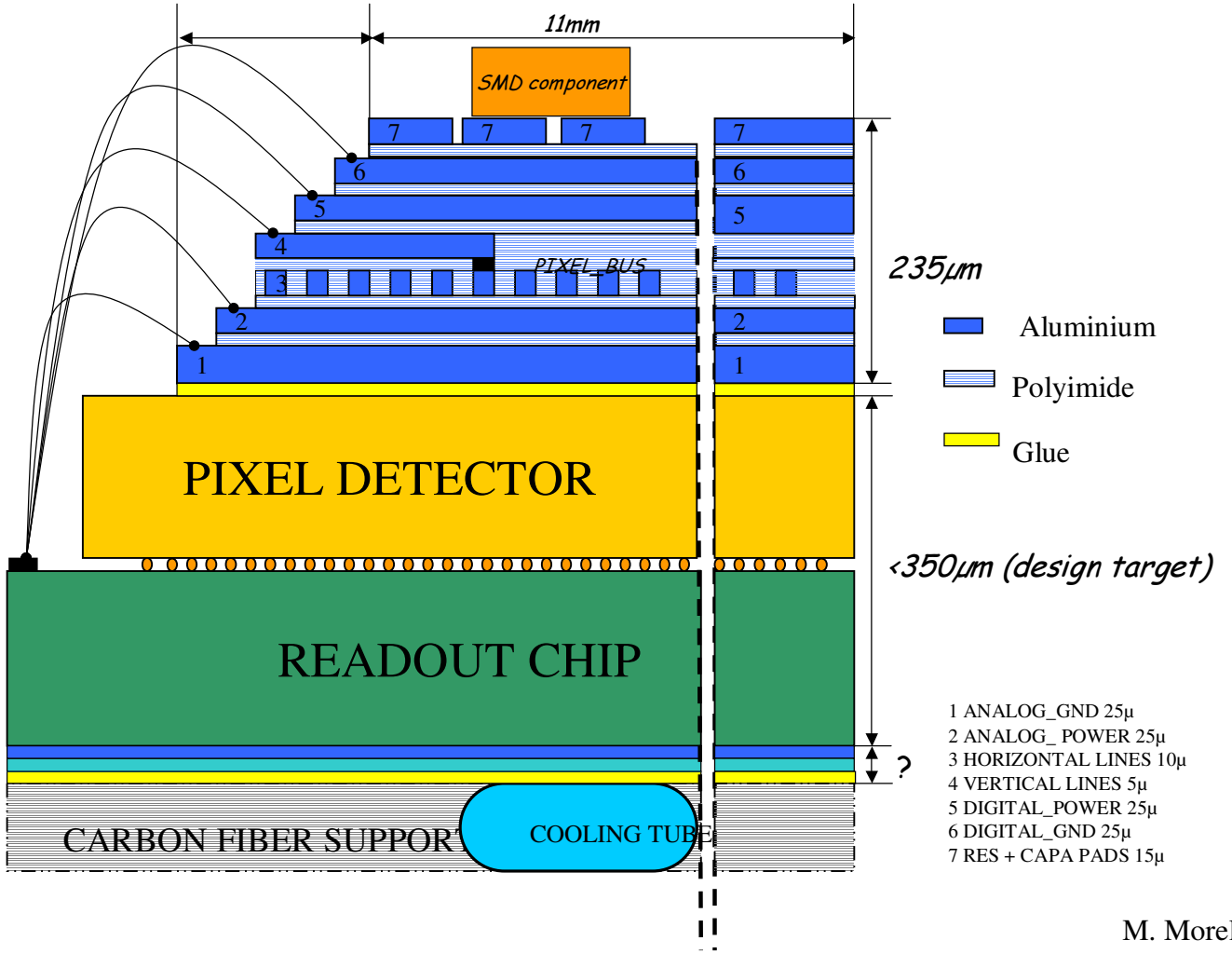
SPD half-stave

Each Stave is built of two **HALF-STAVES**, read out on the two sides of the barrel, respectively.



[Slide courtesy of F. Antinori]

Pixel Bus & Ladders

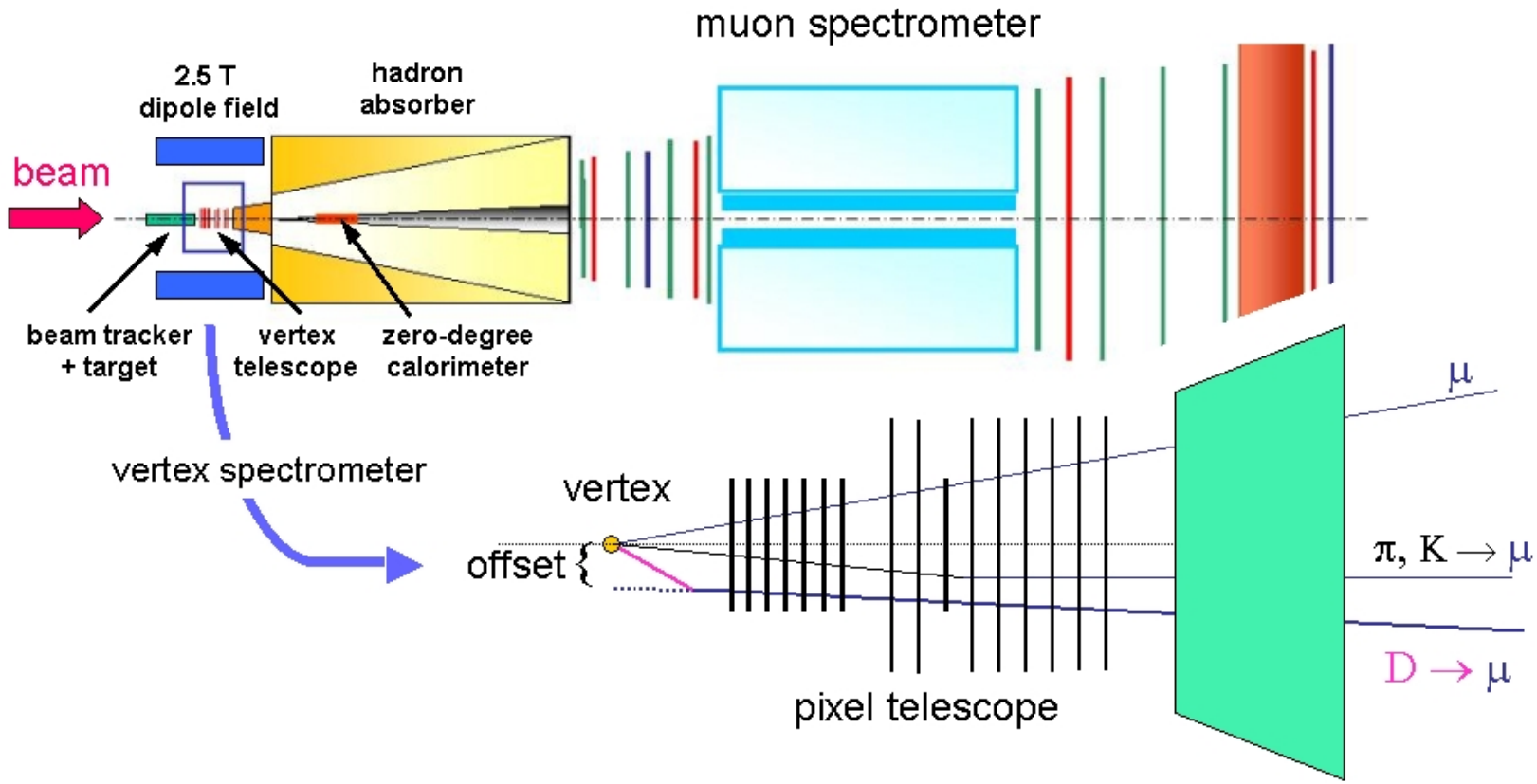


M. Morel

Status of SPD project

- Readout chip and assemblies working to specifications
- Thin ladders (200μm detector and 150μm readout chips) have been produced by VTT
- 1st version of readout MCM has been tested and works
- Test beam of full half stave foreseen in October 2003
- Ladder production to start by year end

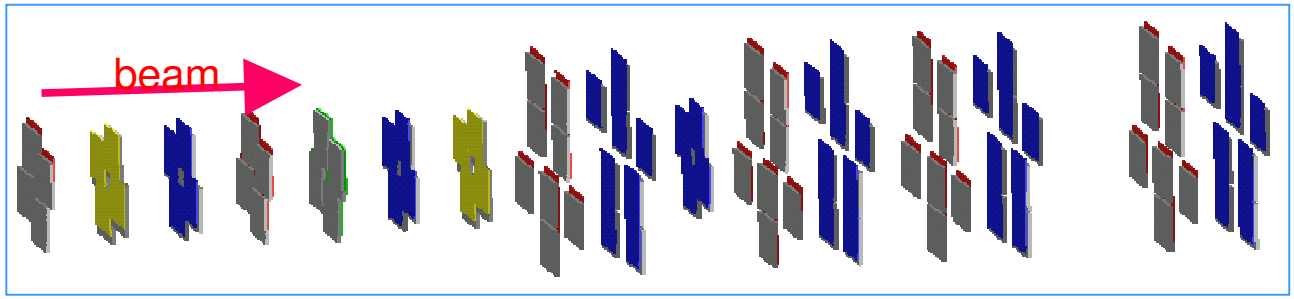
The NA60 Experiment: Study of Prompt Dimuon and Charm Production with Proton and Heavy Ion Beams at the CERN SPS



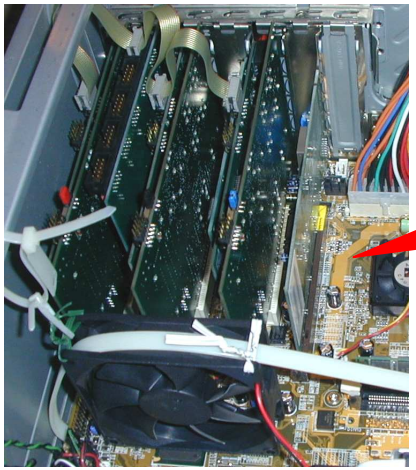
* Muon track matching through the hadron absorber.

* Track offset measurement (<1mm) : Separate **charm** from **prompt** dimuons

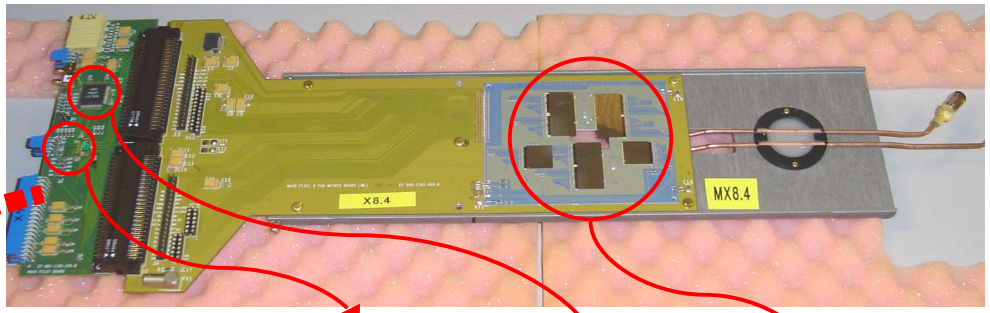
The NA60 Silicon Pixel Telescope

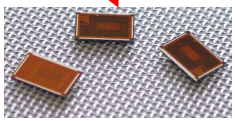


- **8 Planes of 4 chips plus 8 planes of 8 chips: good acceptance, 11 tracking points.**
- **Each chip = 8192 cells of 50 × 425 μm^2.**
- **Thickness = 750 μm readout chip + 300 μm sensors + ceramic hybrid: ~ 3% X_0.**
- **ALICE1LHCB readout chips, 10 MHz chip clock, 200 ns readout strobe.**



DAQ PCs with CFD card and Pilot Mezzanine (around 140 MB/burst)



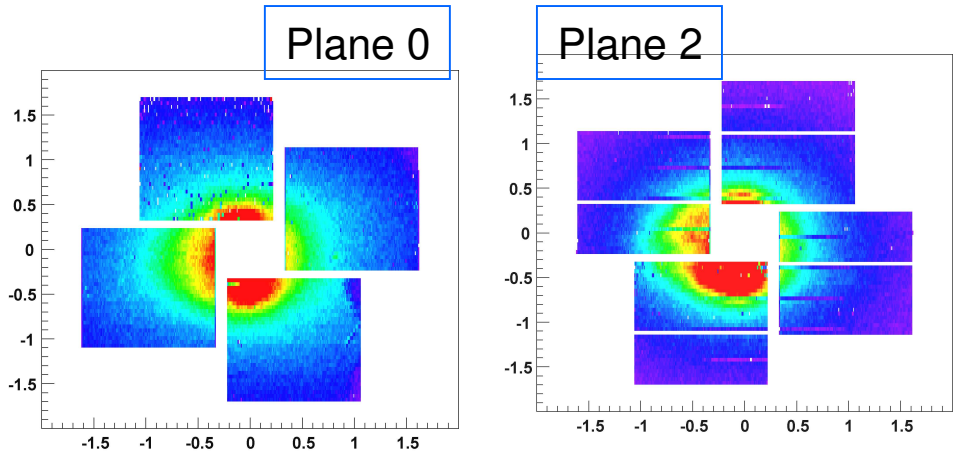


GOL chip

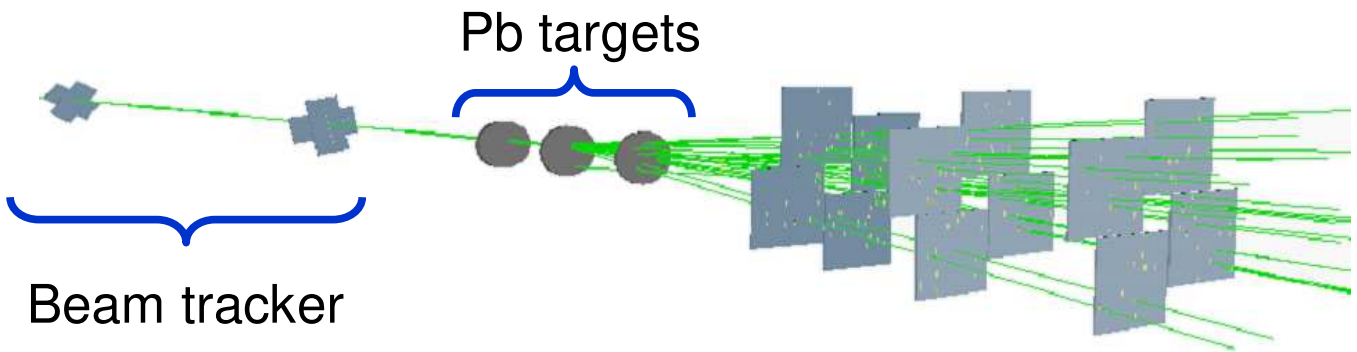
hybrid with assemblies

NA60 Low-energy Heavy Ion Run in Oct. 2002

- 20 and 30 GeV/nucleon Pb ions.
- 3 Pb-targets:
  1.5, 1.0 and 0.5 mm thick.
- Three 4-chip pixel detector planes at 2000 e threshold.
- Nearly no noisy pixels (« 0.5 %).
- Test columns efficiency problem in planes 2 found and fixed.



- Average vertex resolution: z: 200 μm transverse coordinates: ~ 20 μm

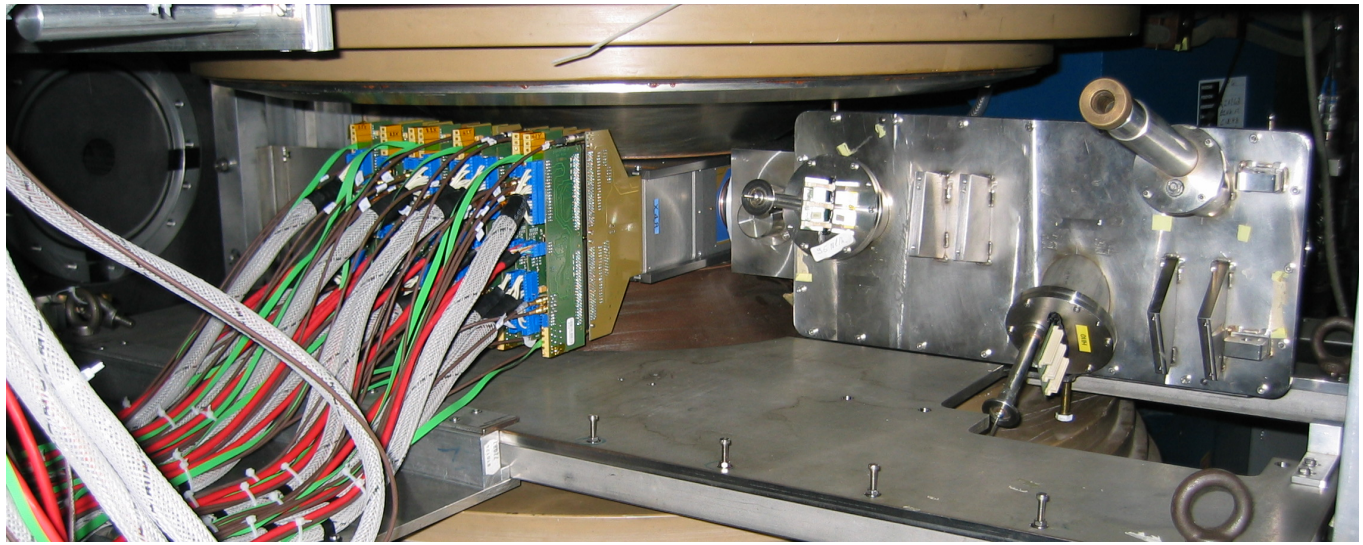


An average-multiplicity event with 36 reconstructed tracks.

Preparations for NA60 Heavy Ion Run, Oct. 2003

Proton test run September 2003:

- **7 small and 5 large planes were installed in the dipole magnet.**
- **All 12 pixel detector planes worked fine.**



- **Physics with In-In collisions at 158 GeV/nucleon, Oct. - Nov. 2003:**
- **The remaining 4 planes for the full 16-plane pixel telescope are ready and being added to the vertex spectrometer.**

J. Heuser et al., "The NA60 Experiment: Results and Perspectives, submitted for the proceedings of the Conference on the Intersections of Particle and Nuclear Physics, New York City, May 19-24, 2003.

Beyond LHC

- Requirements for future pixel vertex systems
- Electronics design considerations
- Addressing the problem of heat dissipation
- Suggestions for future research directions

Requirements for future pixel systems

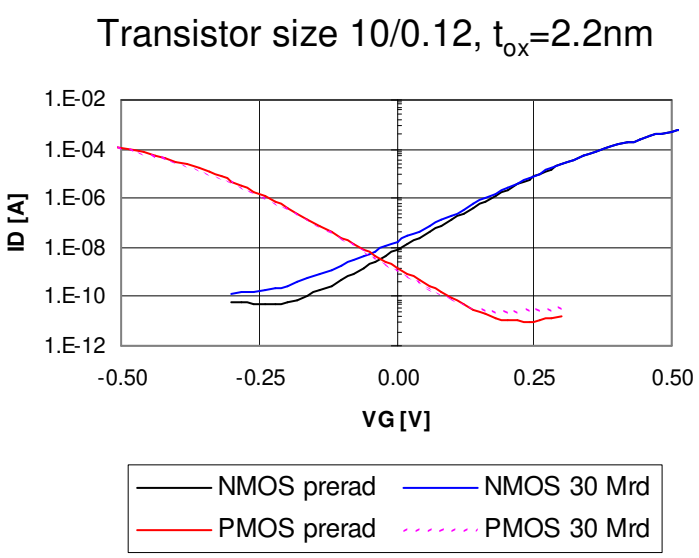
- **Even more radiation tolerance**
- **Maintain pattern recognition capabilities**
  - **High separation threshold/noise**
- **Better time precision**
- **Better spatial resolution**
  - **Less material**
- **Cheap!**

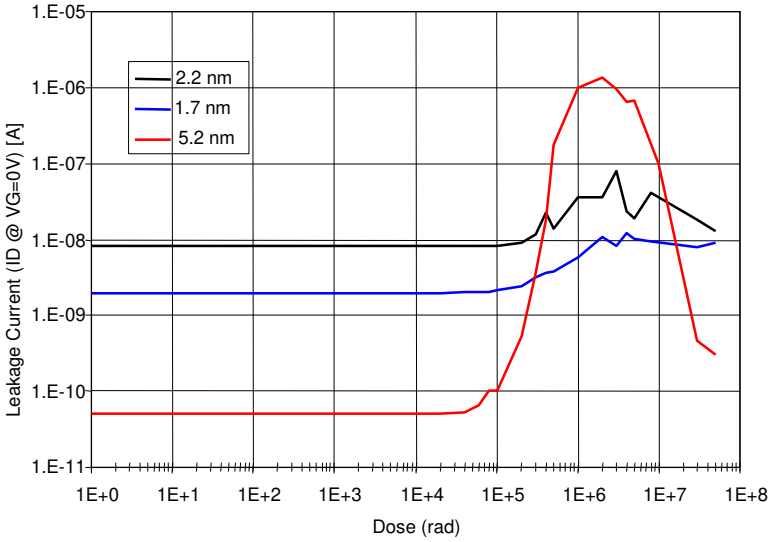
Radiation Hardness - 0.13μm Technology

- **Technology features**
  - 0.13μm generation CMOS technology
  - All copper technology, 4 – 8 metal levels
  - Core supply 1.2V & 1.5V
  - Triple gate oxide (1.7nm, 2.2nm, 5.2nm)
  - Non-epi p- substrate
- **Device options**
  - Standard, low Vt, high Vt NMOS and PMOS, ZeroVt NMOS
  - Ultra thin gate oxide NMOS and PMOS
  - Thick oxide NMOS, PMOS and ZeroVt NMOS
  - n+ diffusion and p+ polysilicon resistors
  - Metal-insulator-metal precision capacitors

Total Ionizing Dose - Wide Linear Devices

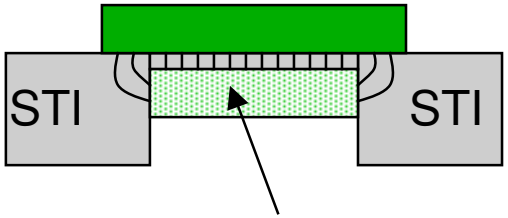
- t_{ox} 1.7nm&2.2nm: Negligible degradation for all transistors, for all parameters
- t_{ox} 5.2nm: variations on threshold voltage and leakage current
- all NMOS devices: small edge effect



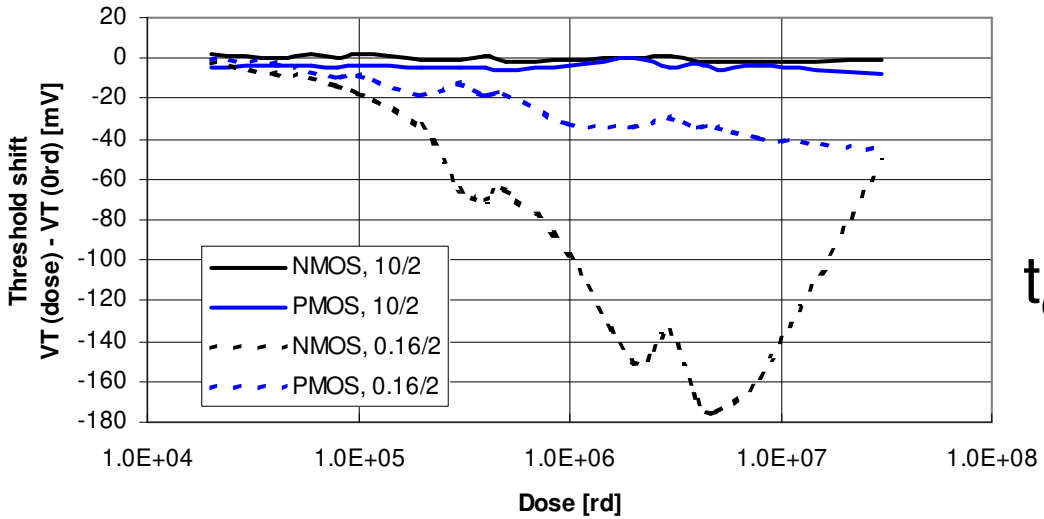


Total Ionizing Dose - Narrow Linear Devices

- Variations not negligible-especially for thick gate oxide (5.2nm)
- strong edge effect
- All transistors types affected



Depletion region

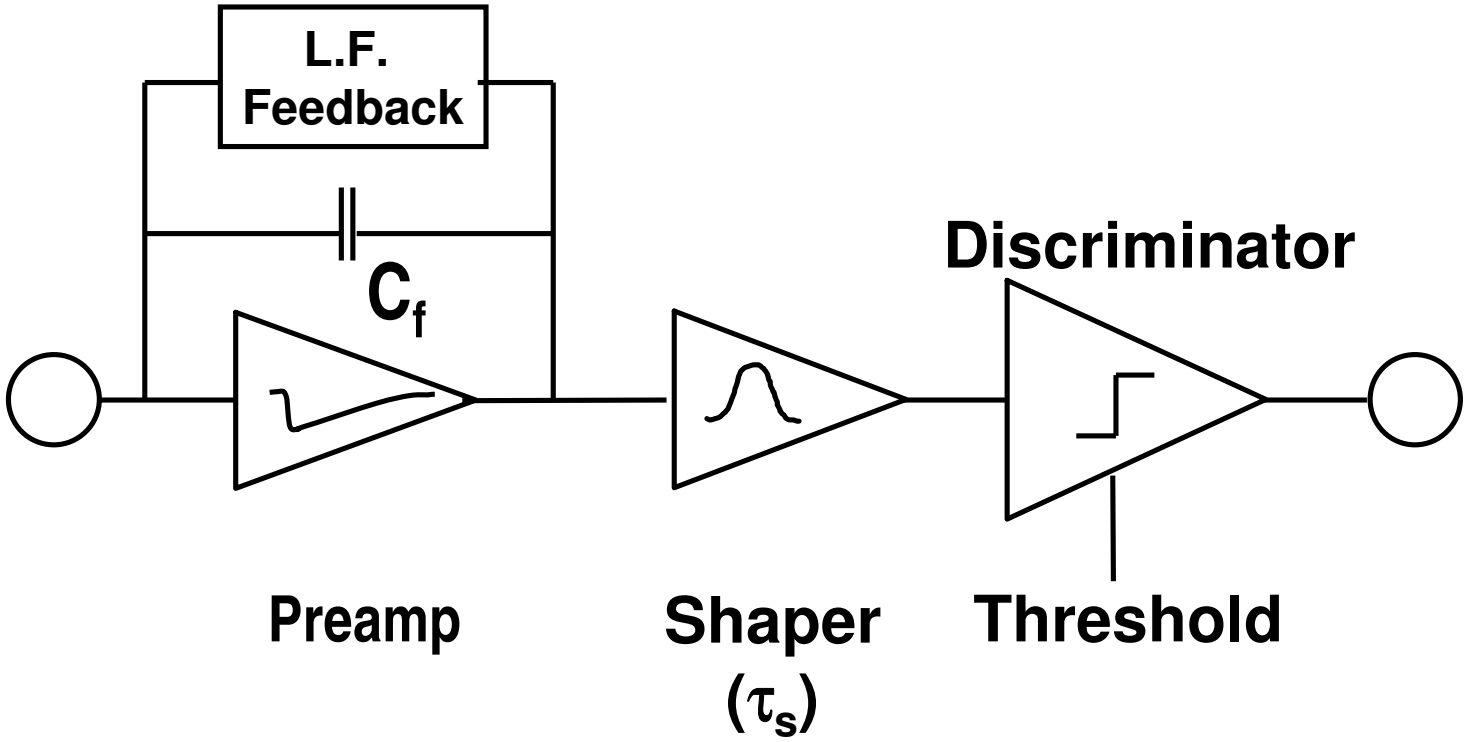


t_{ox} 2.2nm

0.13μm preliminary conclusions

- Seems to provide good radiation hardness even up to several 10's of MRad
- Narrow channel effect has been observed
- Promising for future applications

Typical Front-end for HEP Pixel



Preamp design

For a conventional Charge amplifier readout circuit 3 equations dominate the design:

rise time of preamp

$$t_r \propto \frac{C_t}{g_m}\frac{(C_L + C_f)}{C_f}$$

series noise

$$ENC_d^{\,2} \propto \frac{C_t^{\,2}}{g_m \tau_s}$$

parallel noise

$$ENC_o^{\,2} \propto I_o \tau_s$$

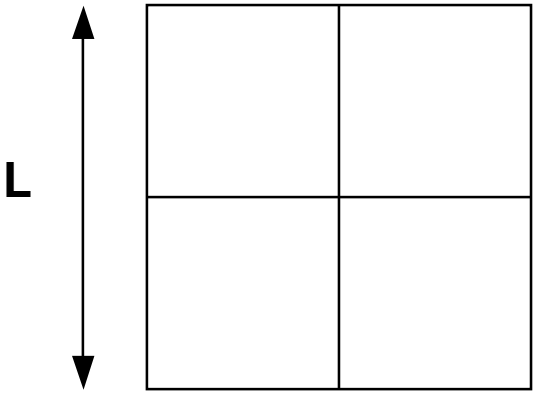
where C_t is the total input capacitance, C_L is the load capacitance of the preamp, C_f is the feedback capacitance, g_m is the transconductance of the input transistor and τ_s is the shaping time.

Scaling - an example

The rise time is proportional to C_t which is dominated by L.

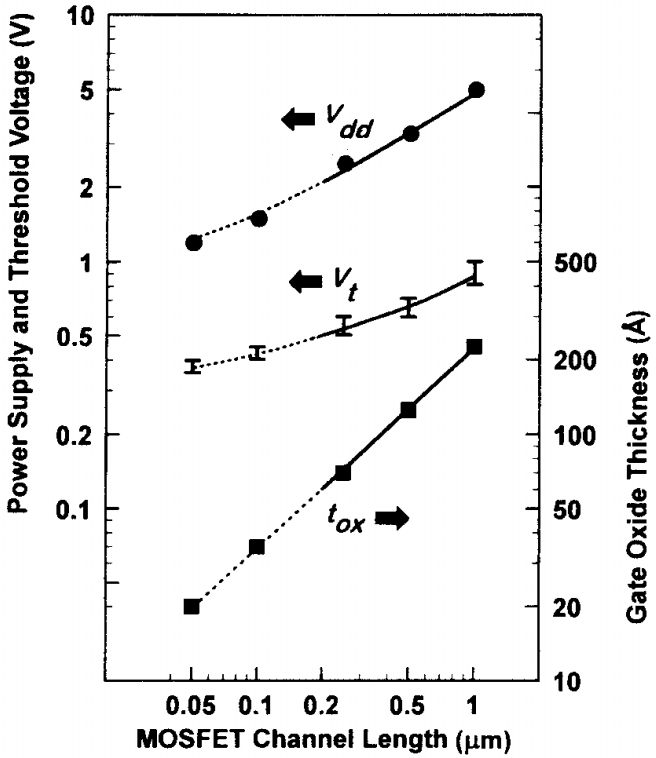
If the pixel is divided by 4, C_t (for all 4 pixels) increases by a factor 2.

Therefore I_d must also increase by factor 2. Power consumption increases even if not by a factor 2 (remember V_{dd} scaling.)



Power consumption increase implies more material for cooling. Therefore reduced spatial resolution.

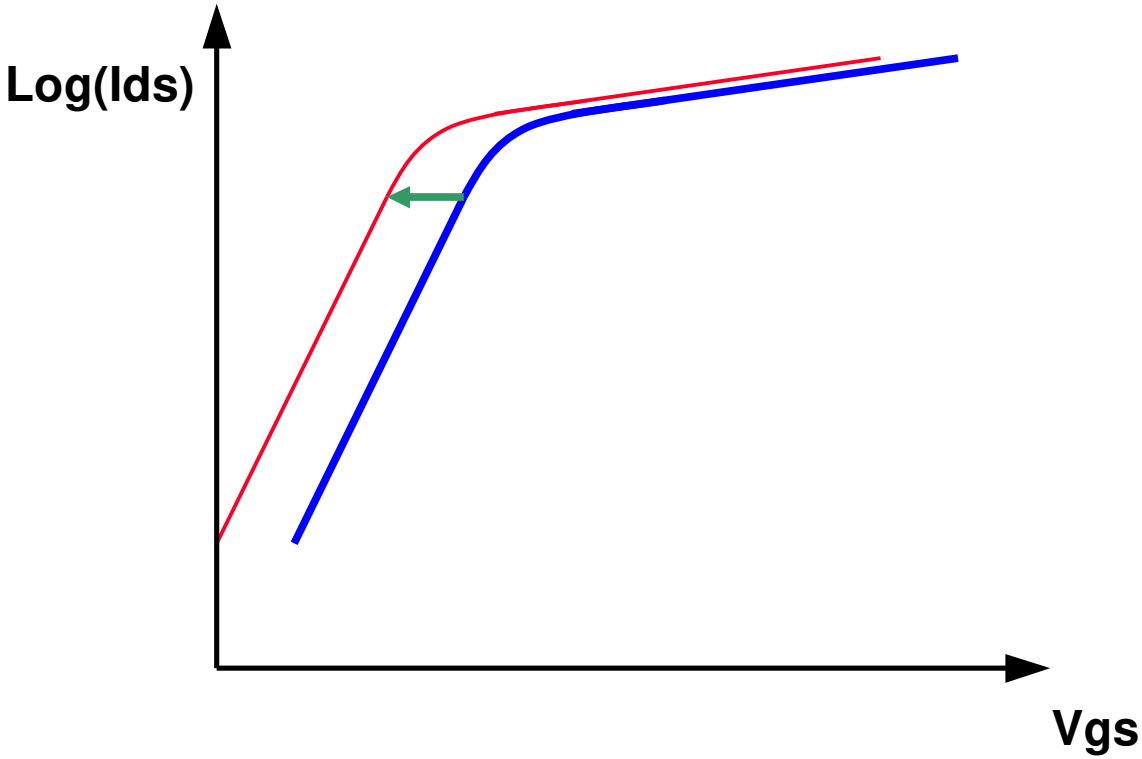
Power Supply Voltage and Transistor Threshold



Stacking of transistors in one branch becomes difficult

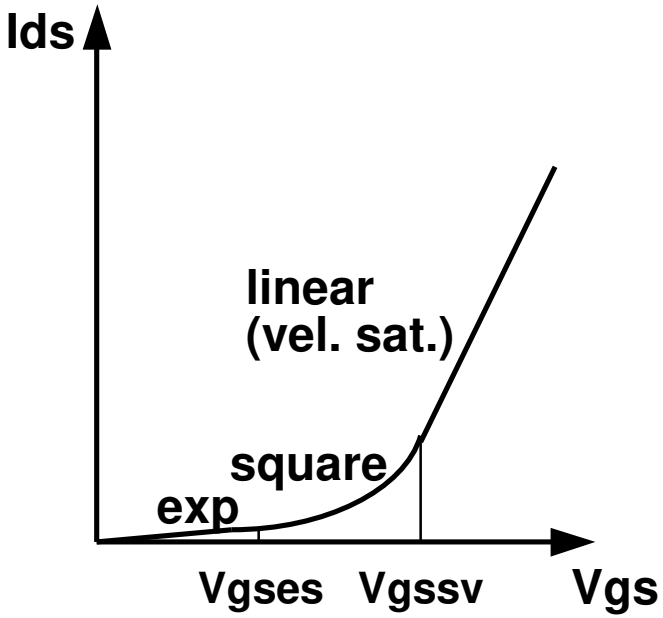
Y.Taur, D.A.Buchanan, W.Chen et al., "CMOS Scaling into the Nanometer Regime, Proceedings IEEE, Vol 85 no4, 1997, pp.486-504

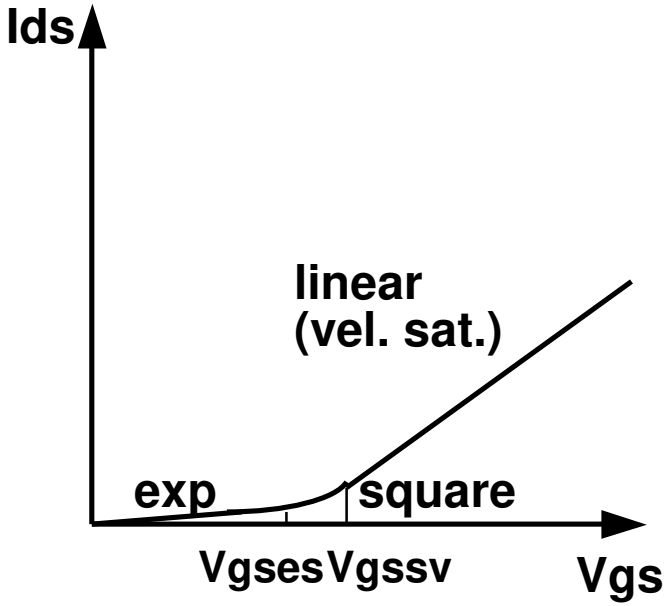
Design Implications of further scaling - Vt reduction



Vt goes down, but weak inversion slope is constant.
Dynamic range limited

Design Implications of further scaling- general - square law region disappears





$V_{gses} - V_t = 2nkT/q$

$V_{gssv} - V_t = 4nLv_{sat}/u$

Input devices will operate in Weak Inversion

$g_m = I_d/nU_T$

W.Sansen, "Low Voltage, low power analog CMOS design," Short Course on low voltage, low power analog CMOS IC design, June 21-25 1999, EPFL, Lausanne, Switzerland.

Design Implications of further scaling - positive aspects

1/f noise decreases

Matching improved for constant dimensions:

$$\sigma^2(V_{th}) \propto \frac{A_v^2}{WL}$$

A_v = 1mV per nm of gate thickness micron*

Many more digital transistors per unit area

*** H.Tuinhout, "Matching of NMOS Transistors," Short Course on Deep Submicron Modeling and Simulation, 12-15 Oct. 1998, EPFL, Lausanne, Switzerland**

CMOS scaling - remaining challenges

Front ends:
New front-end circuit topologies must be developed.
Can over sampling techniques deal with dynamic range limitations?

Digital circuits:
Automatic layout tools are needed for dense designs using radiation tolerant design techniques?
Single event resistant components.

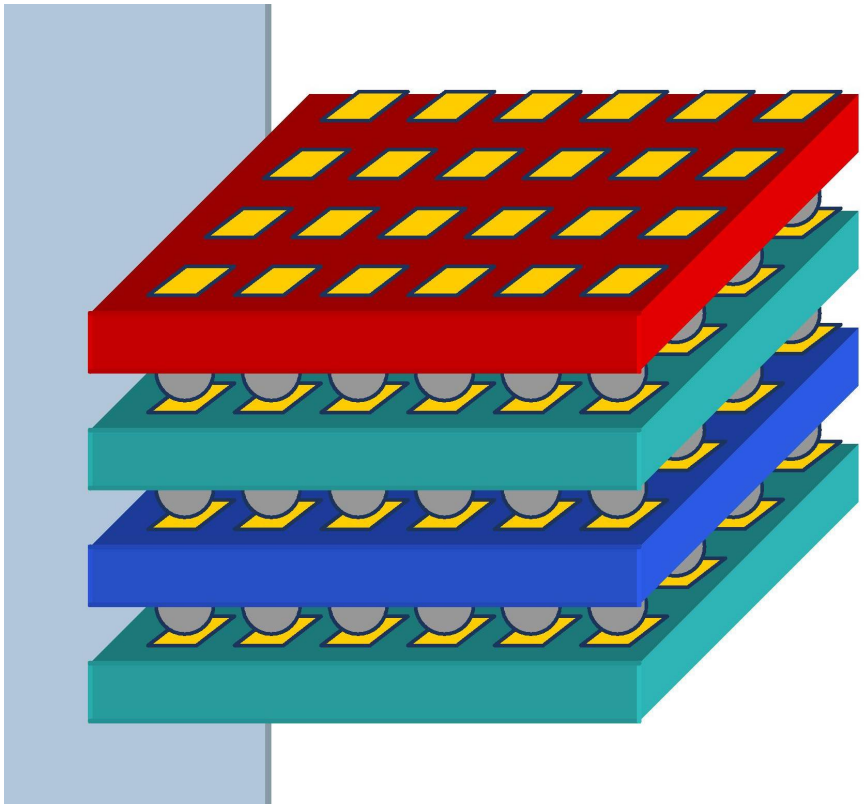
Technology:
How can we access the very best technologies at a reasonable price for prototyping?

CAE:
We have to keep up with the latest tools to use the technologies - automatic layout and wiring tools, verification software

Tiling in 2 dimensions

- 4-side buttable tiles should be developed
- Needs 3 dimensional interconnect!
- Similar technology to 3-D detectors
- Bring all IO and power supplies through the wafer
- Ladders no longer needed
- Already under development in packaging industry…

2-D Tiling concept



Sensor

Interposer

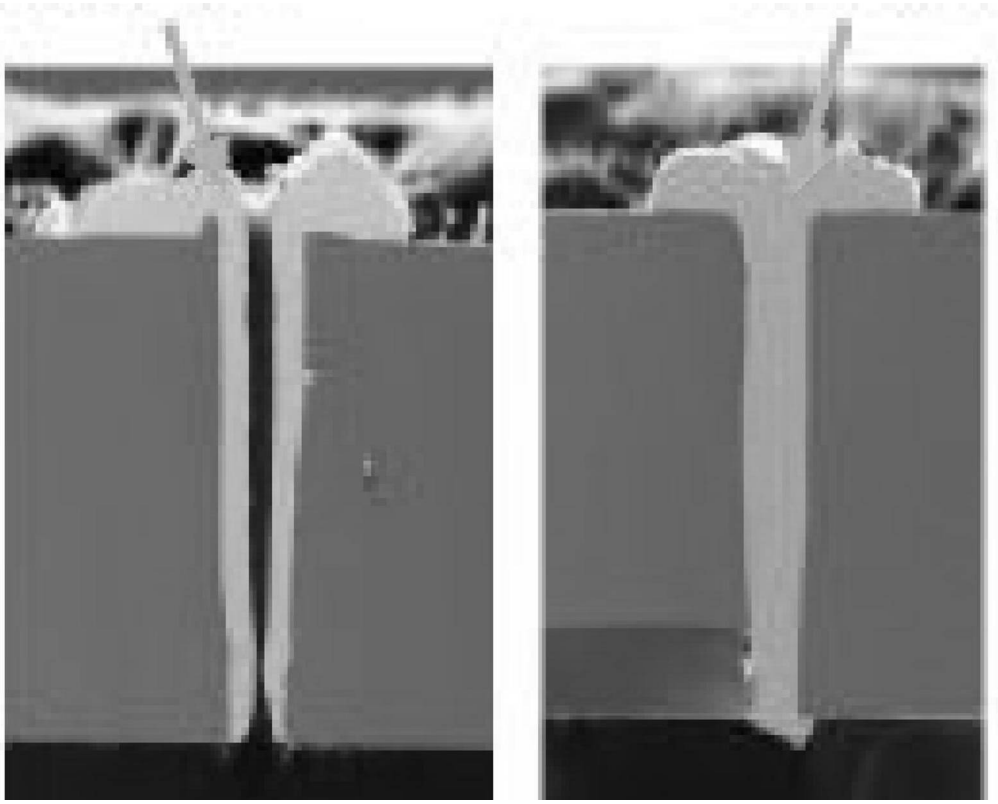
Readout

DSP

IMEC

[J. John, Proceedings of IWorid meeting, Sept. 2003 Riga (next 2 slides)]

Through wafer hole plating

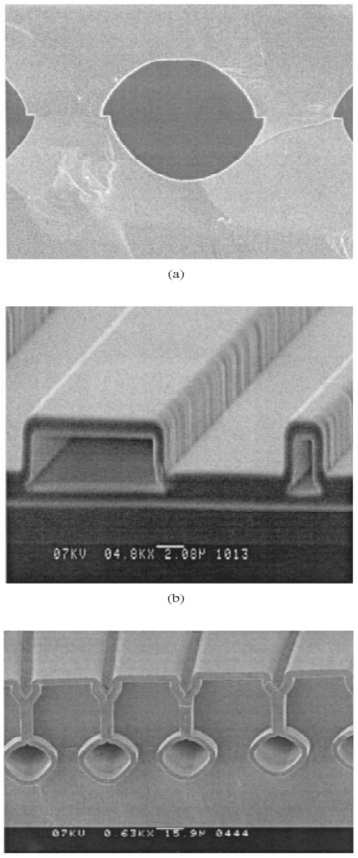


IMEC

W plugs in Si wafer
NB Post processed wafer T_{max} 400 C

Novel cooling techniques

- 3 examples of micro cooling channels
- Must look for solutions which can be used post processing (<400 C)
- Interconnection of channels between chips remains a challenge



[J. Meint et al, Journal of Microelectromechanical Systems, Vol. 9 (1), March 2000]

The way ahead…

- Following the evolution of CMOS is unavoidable
- Cost of prototyping becomes a major issue
- Manpower required for major chip designs in significant (experiments sharing chips???)
- Radiation hardness is still ok (at least for 0.13μm CMOS) but caution is needed in the choice of circuit topologies
- Low mass tiling needs to be developed
- There are promising developments in cooling which may be adopted
- A significant R and D effort is needed to develop a low-mass DSM tile if requirements beyond LHC are to be addressed

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