Status of the CALICE ECAL

CALICE collaboration

http://polywww.in2p3.fr/flc/calice.html

- Introduction
- The proposed calorimeter
- The ECAL prototype
- R&D for next generation
- Schedule

- Silicon wafer
- PCB
- VFE Chip
- Gluing
- DAQ
- First measurements

- New chip
- Thermal studies
- AC coupling (silicon)
- PCB

It is not R&D in the back yard !!

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Start from physics

See what design/technique could fit

List the R&D to do to validate the choice

Study potential performance with simul.

Optimise EFLOW performances lead to optimize close showers separability so, like digital camera

➔ number of pixel !!!!

The proposed calorimeter

Ultra granular/segmented – stable – compact

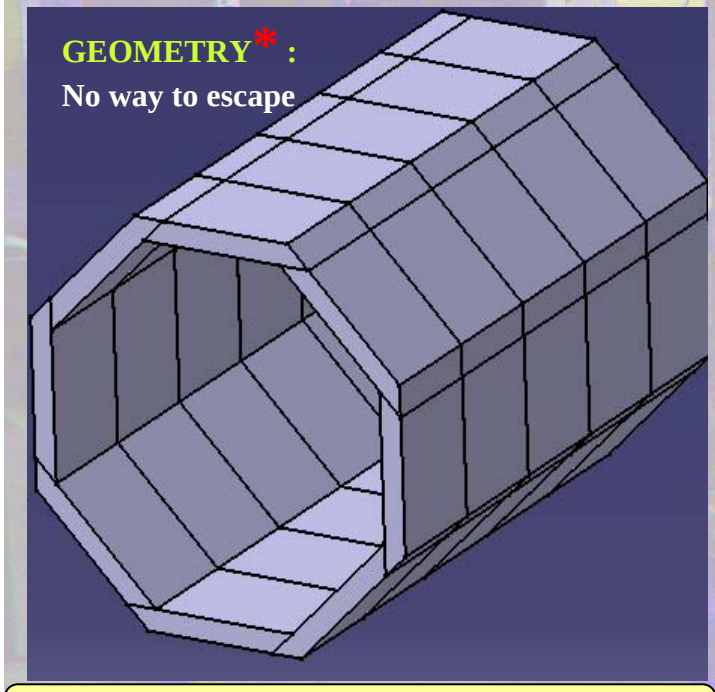
example ECAL , a sampling tungsten – silicon

example HCAL , a sampling Fe – RPC's, gem, scint. tiles

Well adapted for the physics programme at TeV LC

i.e. to fully reconstruct multi-jets events

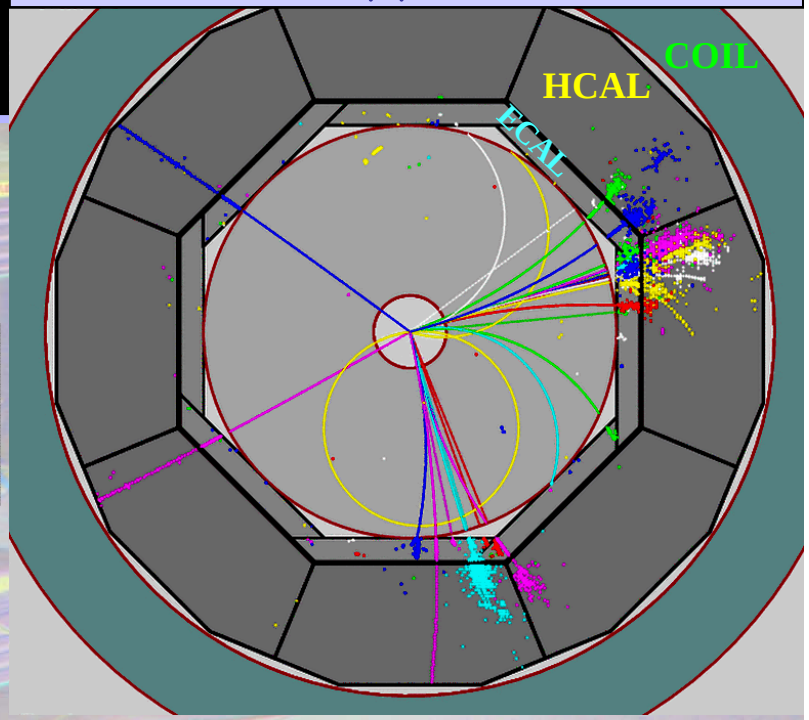
to have a good channel id. in the τ decays



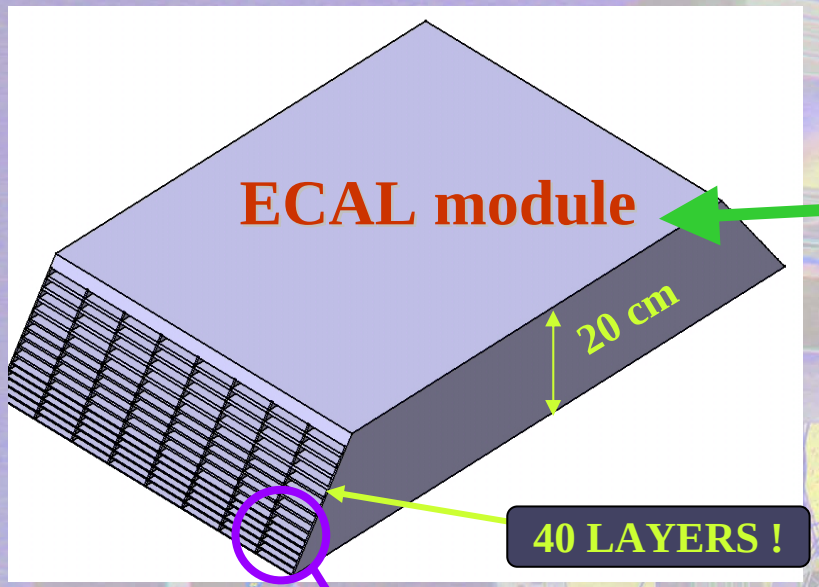
Perspective view of the ECAL

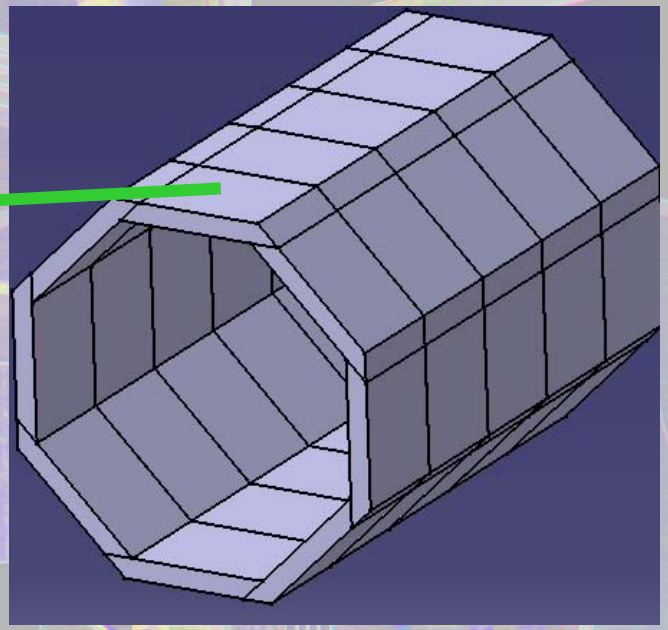
- 40 layers
- pads 1x1 cm^2
- 32 M channels

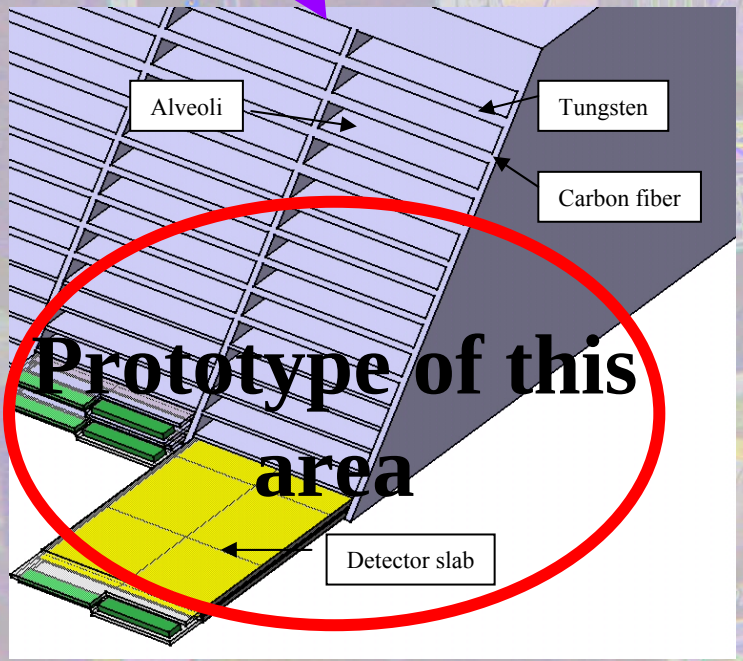
$e^+e^- \rightarrow ZH$, $Z \rightarrow \mu\mu$ at $\sqrt{s}$=500 GeV



[*] The calorimeter 8-fold way of Henri Videau







- No large dead zone
- All modules are identical
- Detector slab tested before mounting

Based on mechanical study ,

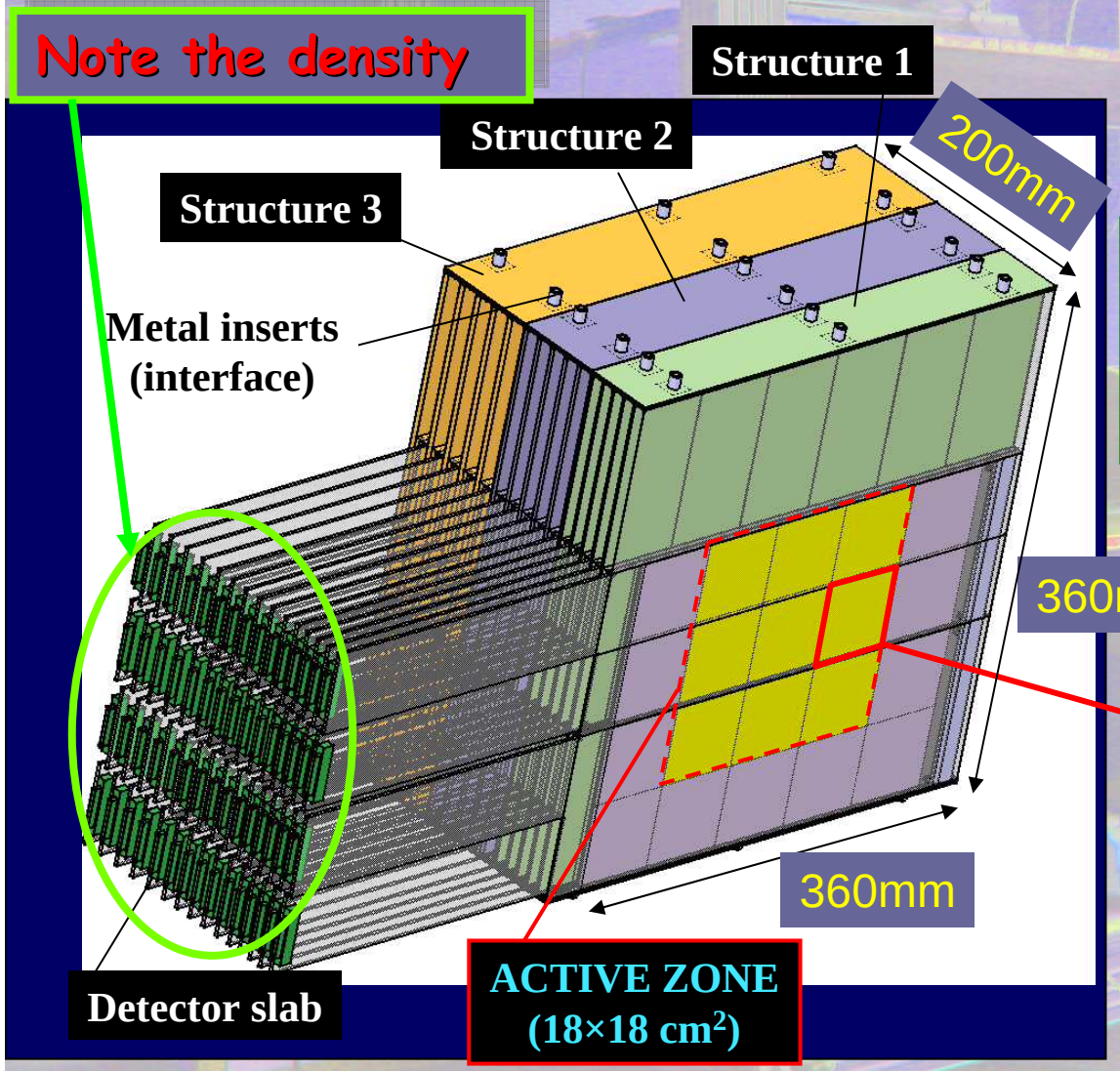
The full scale detector can be realised with the same pattern:

"Tungsten wrapped in CFi"

The ECAL prototype

CALICE ECAL

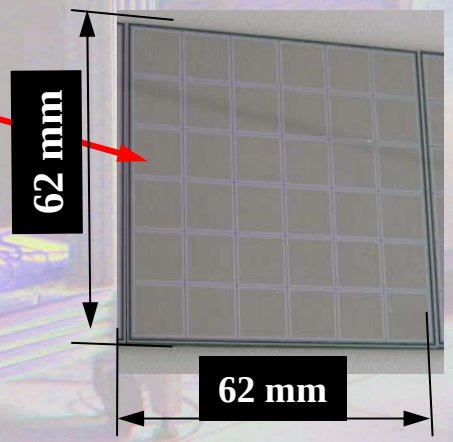
- LAL,LLR,LPC,PICM
- Imperial College, UCL, Cambridge, Birmingham, Manchester, RAL
- ITEP,IHEP,MSU
- Prague (IOP-ASCR)
- SNU,KNU



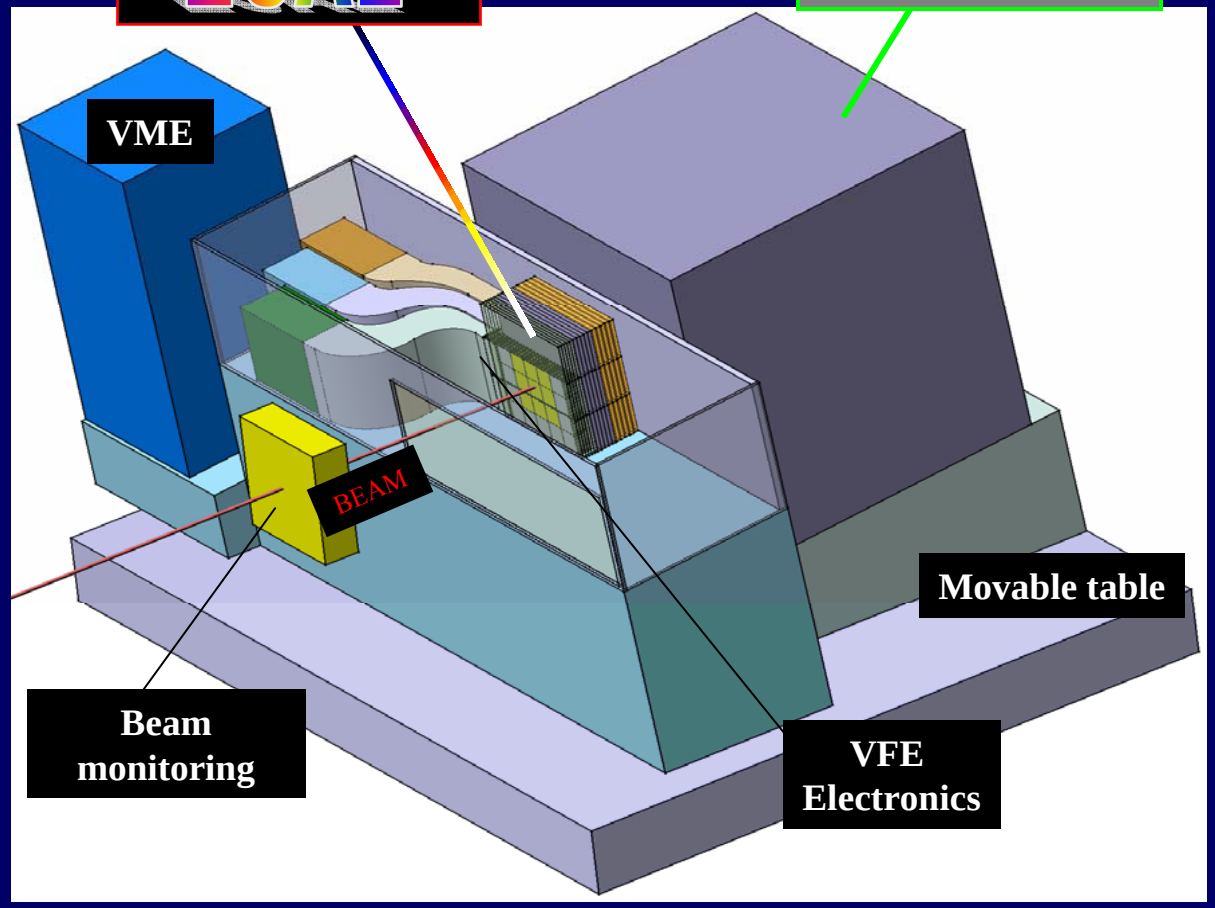
- 3 structures W-CFi (1,2,3 x1.4mm)
- 15 « detector slabs »
- Dimension 200x360x360 mm

➔ **9720 channels in the proto.**

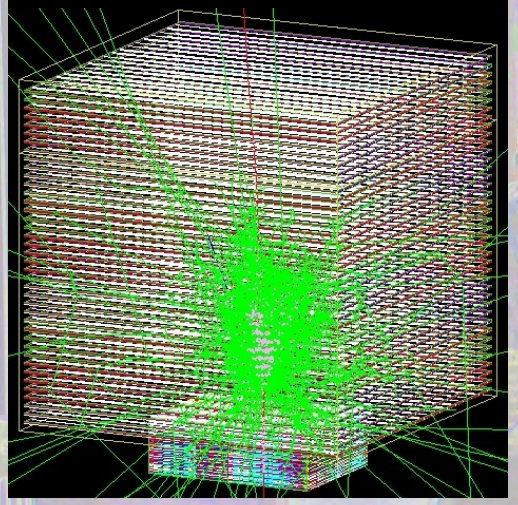
Silicon wafers with 6×6 pads (10×10 mm²)



Prototypes for the test beam

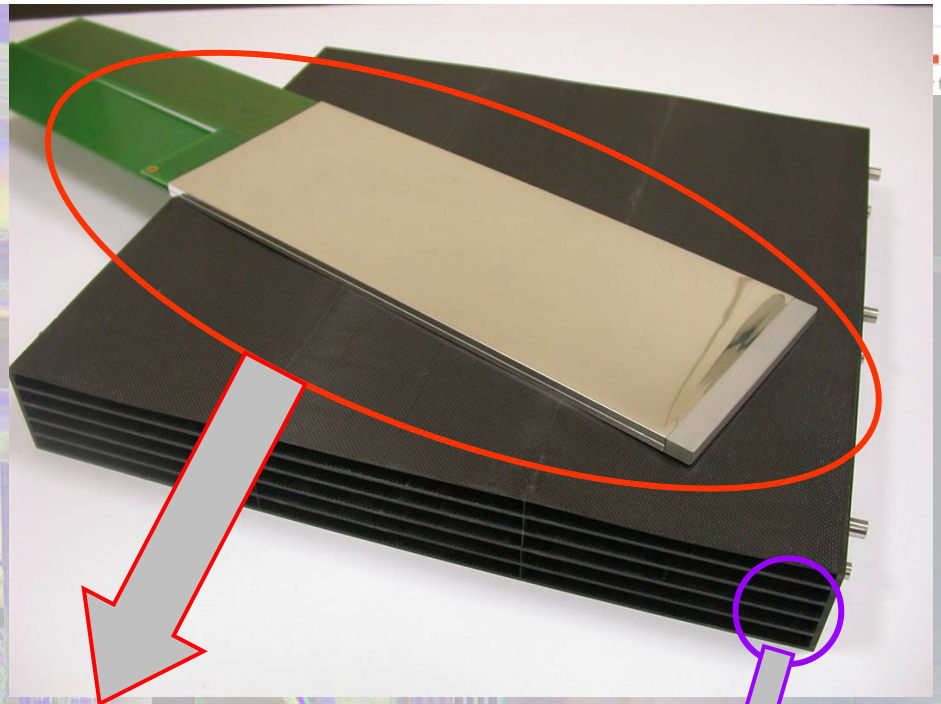


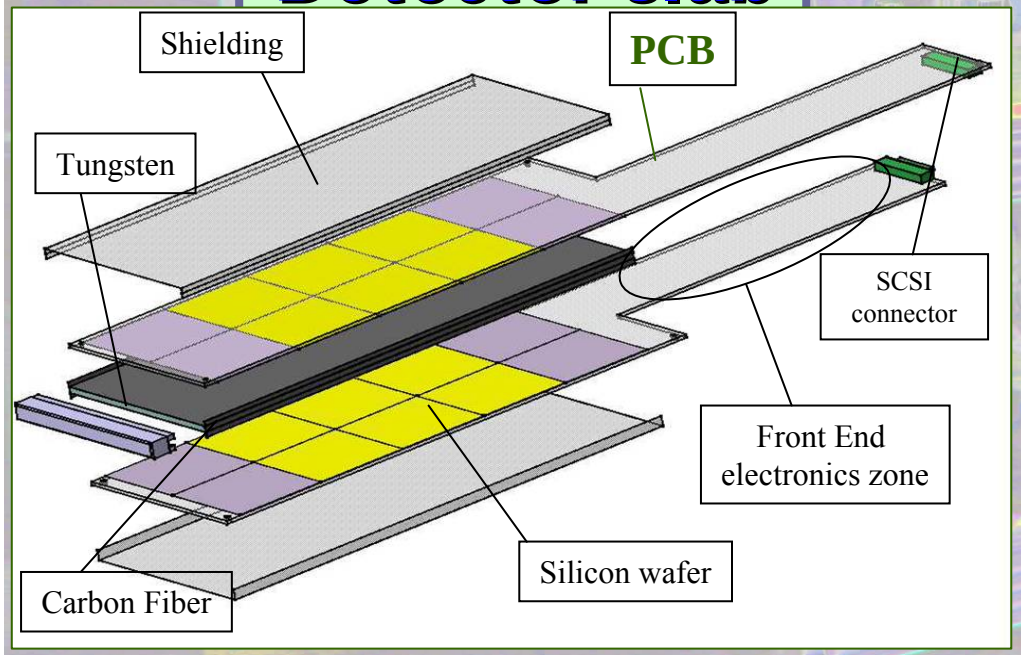
Simulation GEANT4

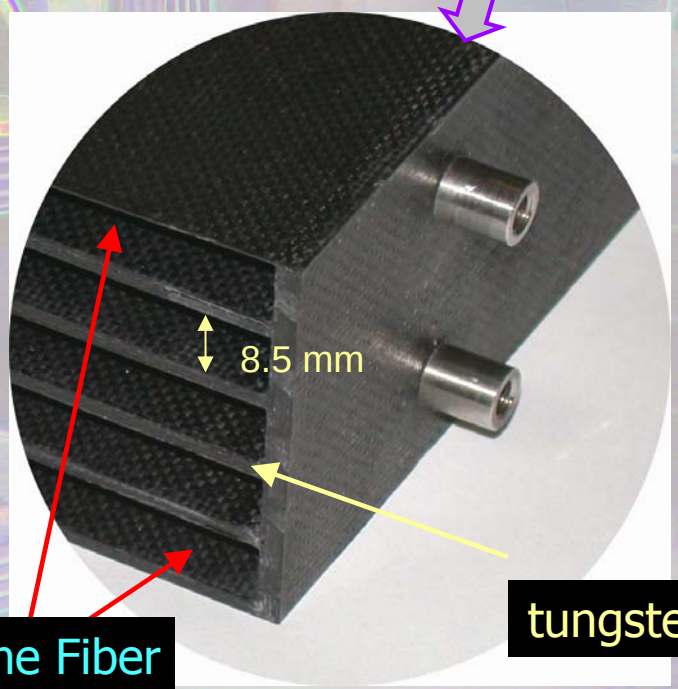


10 GeV pion

Detector slab







Silicon Wafers for the prototype

4″ High resistive wafer : 5 KΩcm

Thickness : 525 microns ± 3 %

Tile side : 62.0 + 0.0

- 0.1 mm

Guard ring

In Silicone ~80 e-h pairs / micron ⇒ 42000 e^- /MiP

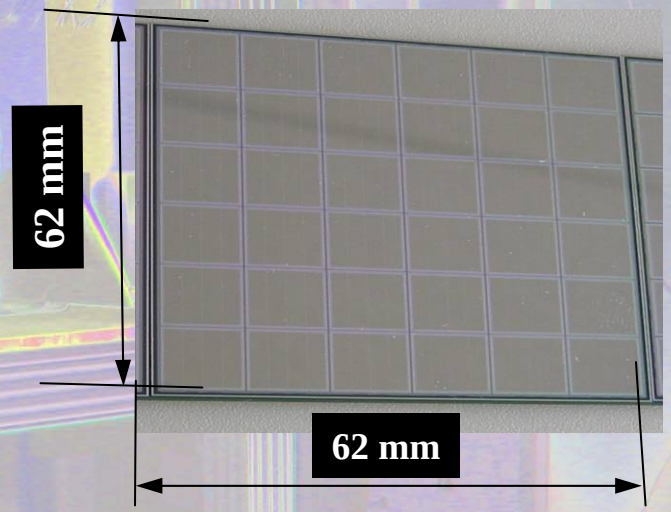
Capacitance : ~21 pF

Leakage current : 5 – 15 nA

Full depletion bias : ~150 V

Nominal operating bias : 200 V

Si Wafer :
6×6 pads of detection
(10×10 mm²)



One wafer is a Matrix of 6 x 6 pixel of 1 cm².
Important point : manufacturing must be as simple as possible to be near of what could be the real production for full scale detector in order to :

- Keep lower price (a minimum of step during processing)
- Low rate of rejected processed wafer
- good reliability and large robustness

Silicon Wafers for the prototype

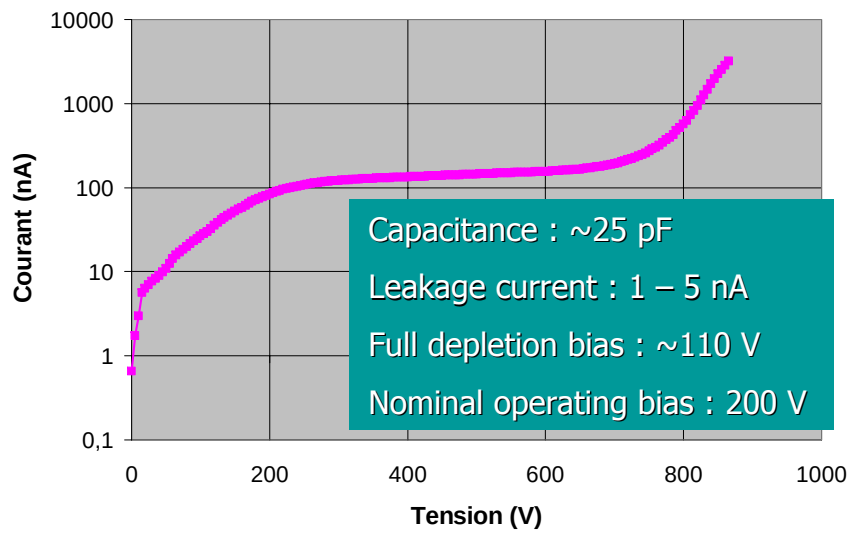
Number of active Wafer needed for the physic prototype : **270**.

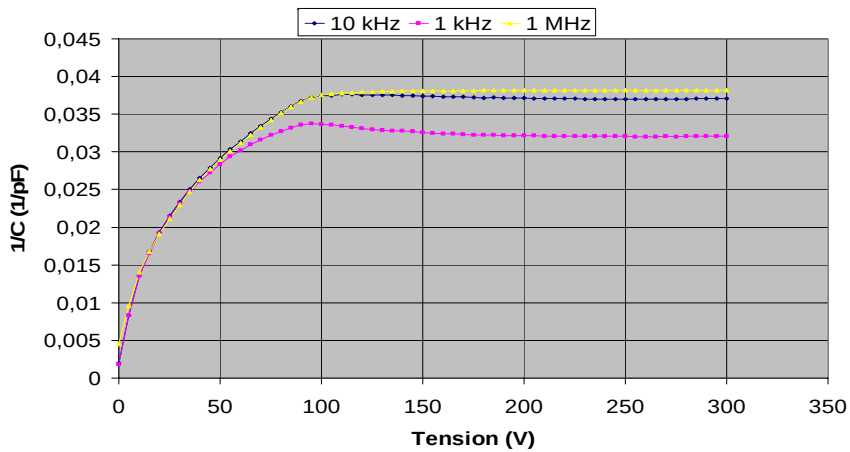
- 150 produce by Institute of Nuclear Physics - Moscow State University (M. Merkin, A. Savin , A. Voronin)
  - First test production : February 2003
  - Today : **~130 matrices**

- 150 produce by Institute of Physics, Academy of Sciences of the Czech Republic – Prague (V .Vrba)
  - ***First test production : March 2004*** (6 good wafers)
  - Full prod for end of May.

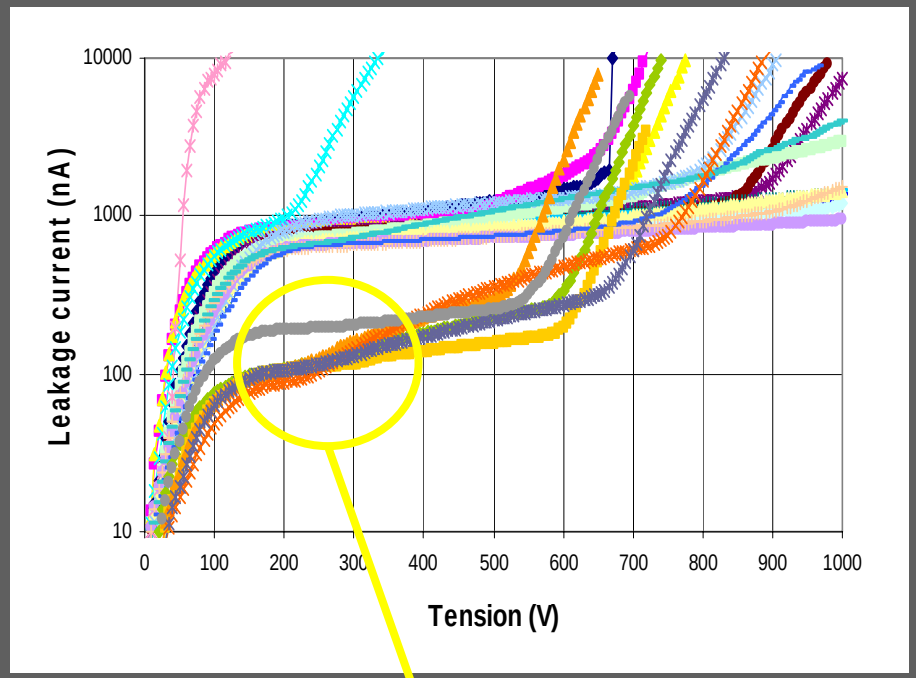
Silicon Wafers for the prototype

Institute of Nuclear Physics Moscow State University





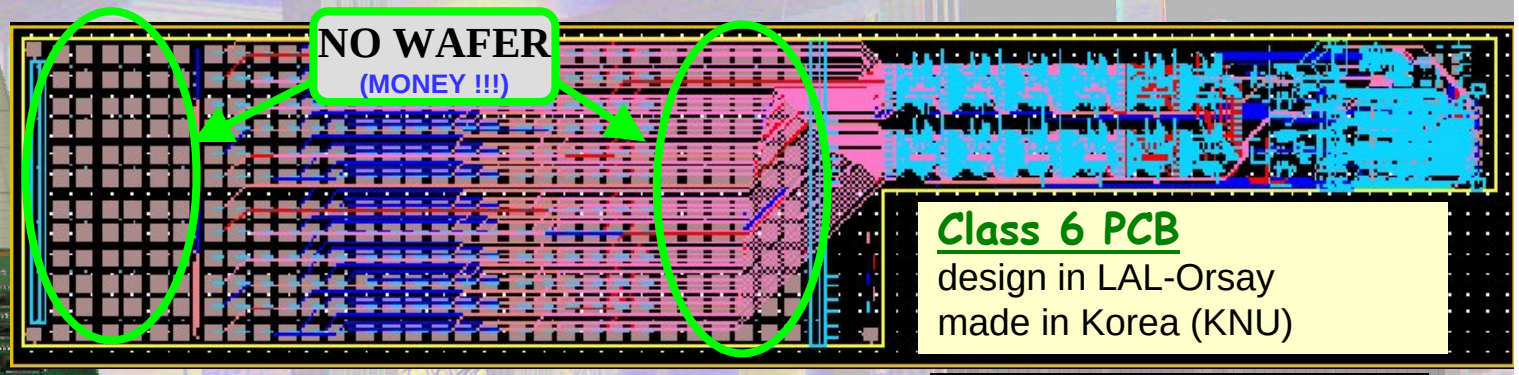
Institute of Physics, Academy of Sciences of the Czech Republic



One process gives results which fit the spec.

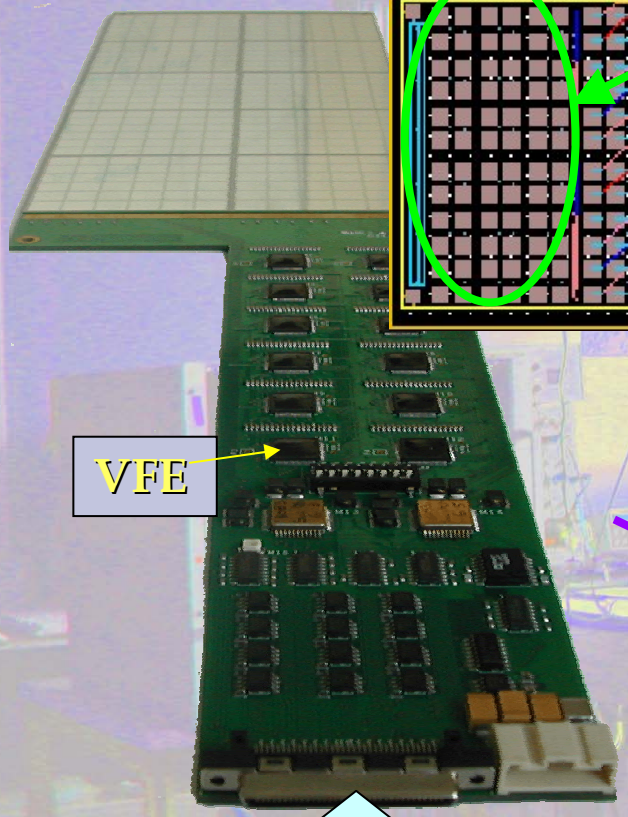
PCB for the prototype

Silicon matrix



Class 6 PCB
design in LAL-Orsay
made in Korea (KNU)

PCB 14 layers, 2 mm



DAQ

VME/PCI

Prototype : 60 PCB → middle of July

FLC-PHY3

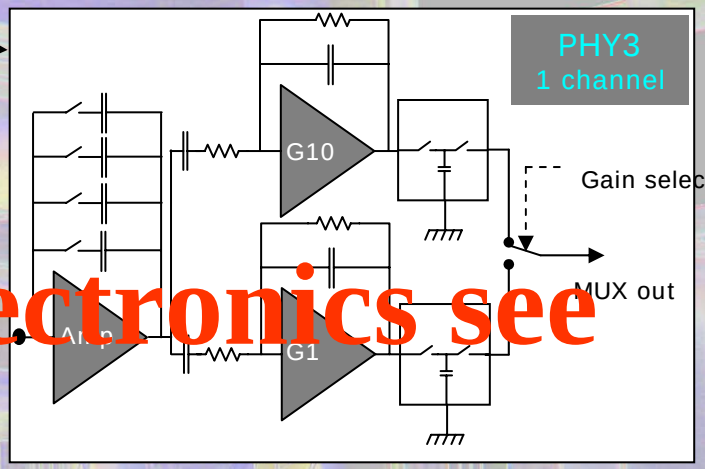
Chip VFE

Processed channels 18 (two possible gains)

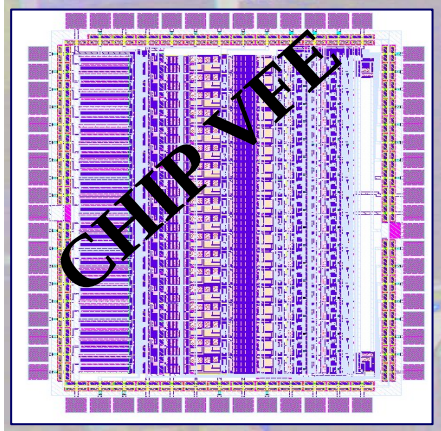
Noise ENC=3300 + 30 e-/pF

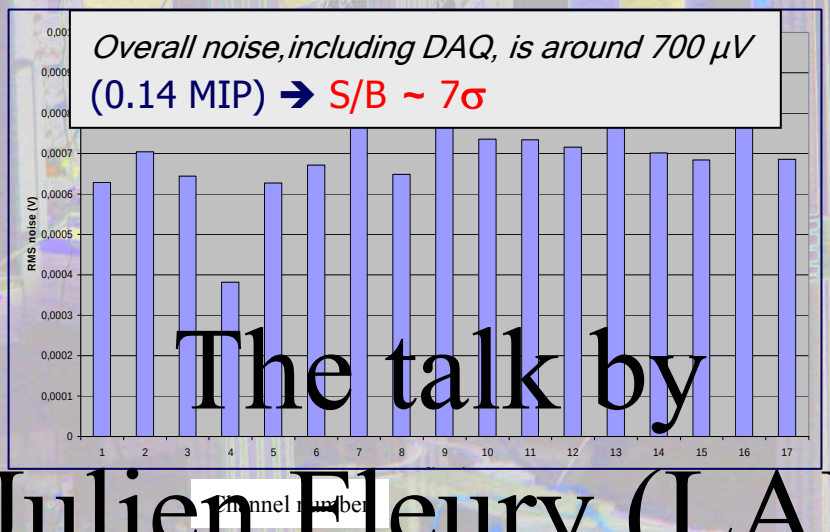
Linearity ± 0.2 %

Dynamic 600 MIPS @ Cf = 1.6 pF



VFE electronics see





Overall noise, including DAQ, is around 700 µV
(0.14 MIP) ➔ S/B ~ 7σ

The talk by Julien Fleury (LAL)

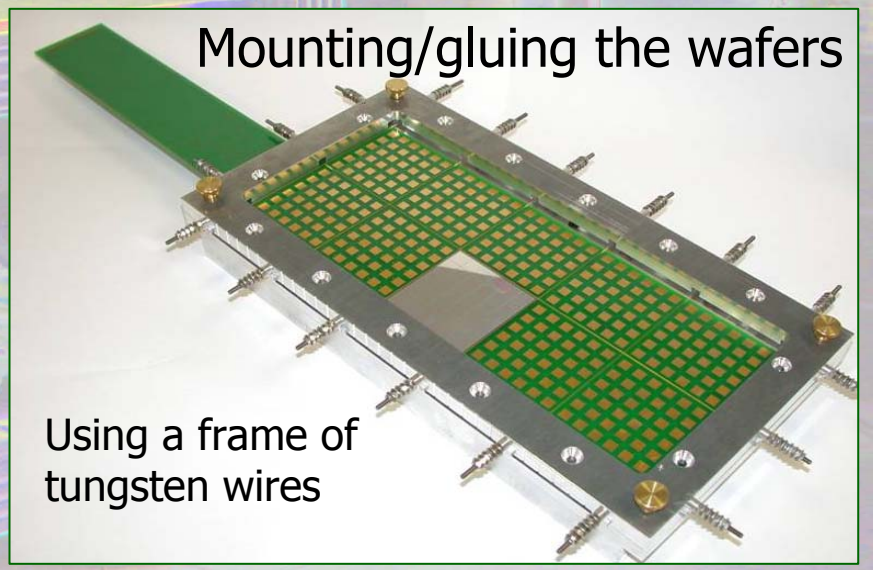
Mounting/Gluing the wafers

A automatic device is use to deposit the conductive glue :
EPO-TEK® EE129-4

X-Y-Z table (400×400×150 mm^3) with glue dispensing tool (conductive glue)

Gluing and placement (± 0.1 mm) of **270** wafers with 6×6 pads

About **10 000** points of glue.



ADC - DAQ system

DAQ for Prototype

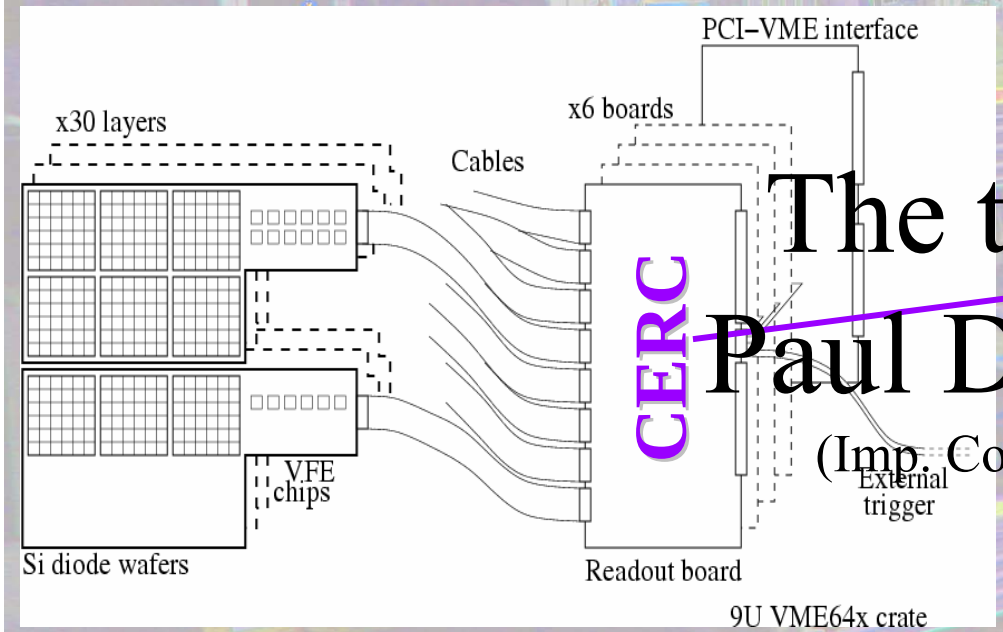
- **F**ull **P**rototype **D**AQ (FPD)

  based on **VME 9U** board developed for CMS modified by UK groups

  no zero supress, 96 VFE/board, 16 bits ADC's, 20 Kbytes/s possible for Test Beam

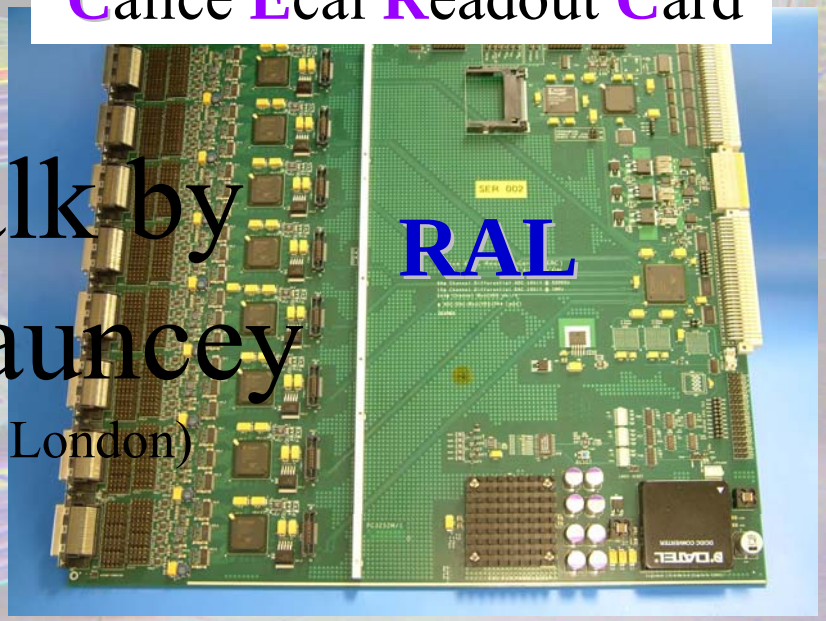
  First test on April 2004 validate the full chain from wafer to DAQ and "tape"

See



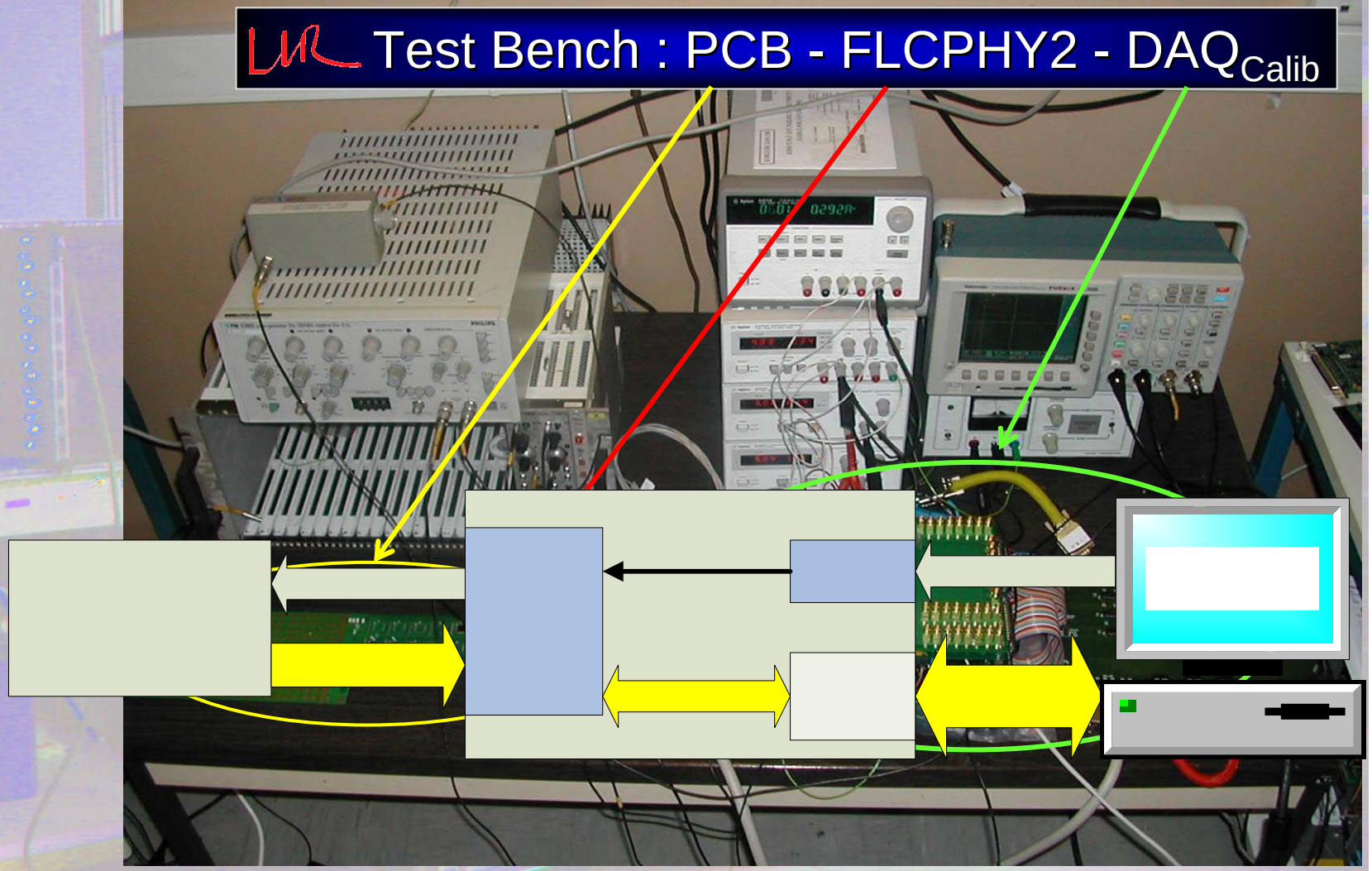
The talk by Paul Dauncey (Imp. Coll. London)

Calice **E**cal **R**eadout **C**ard

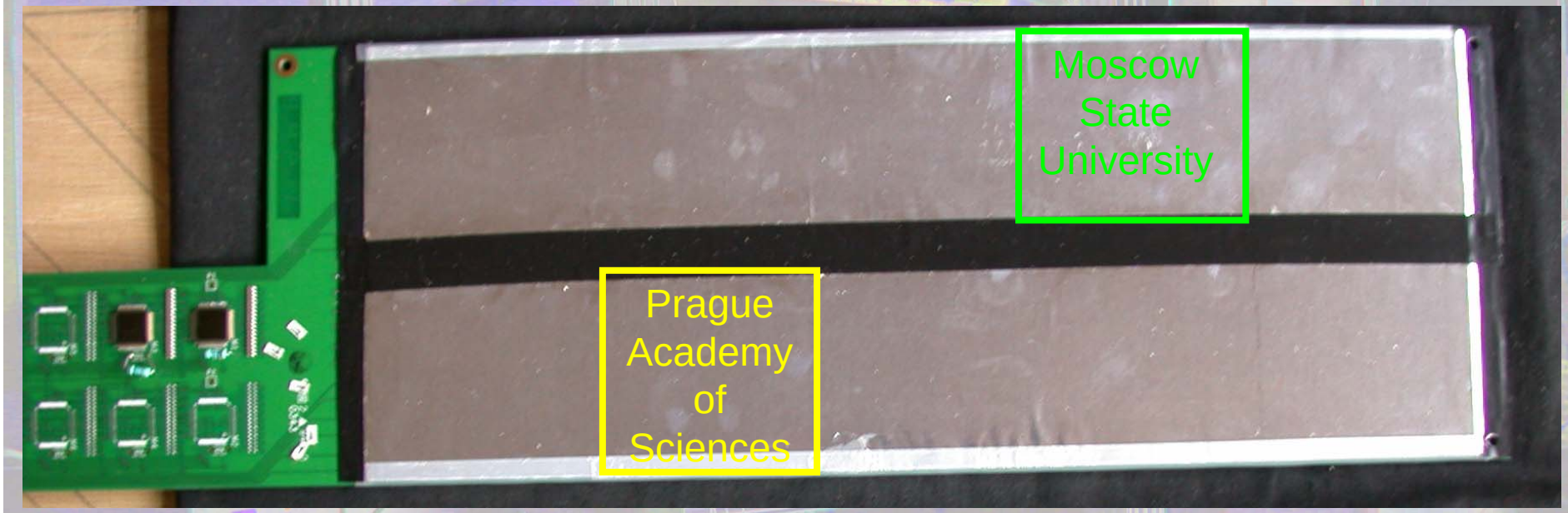


ADC - DAQ system

- **Single Slab DAQ (SSD)**
  - for calibration and test on Cosmic Test bench
  - work only for a single detector slab
    (24 VFE chips/ 432 silicon pad channels)
  - based on NI board (on-shell)



First test with a complete detector slab



First test with a complete detector slab

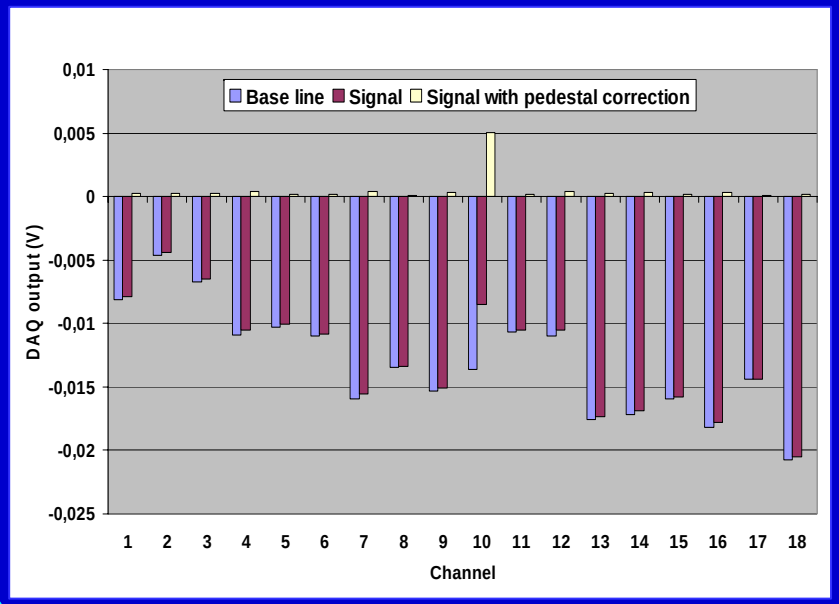
LLR : S.Chollet, F.Gastaldi, A.Karar, J-Ch. Vanel
LAL : J.Fleury

Si wafer - glue - PCB - VFE – DAQ (Single Slab DAQ)
and ground with Al. EMC shield

"internal" signal

1 MIP injected in channel 10 with CALIB chip and measurement made on 100 points

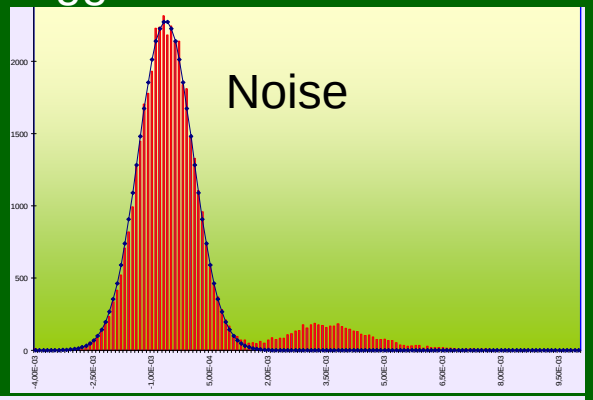
-Theoretic result : 4.97mV
(C_f=1.35pF)
-Measured : 5.05mV

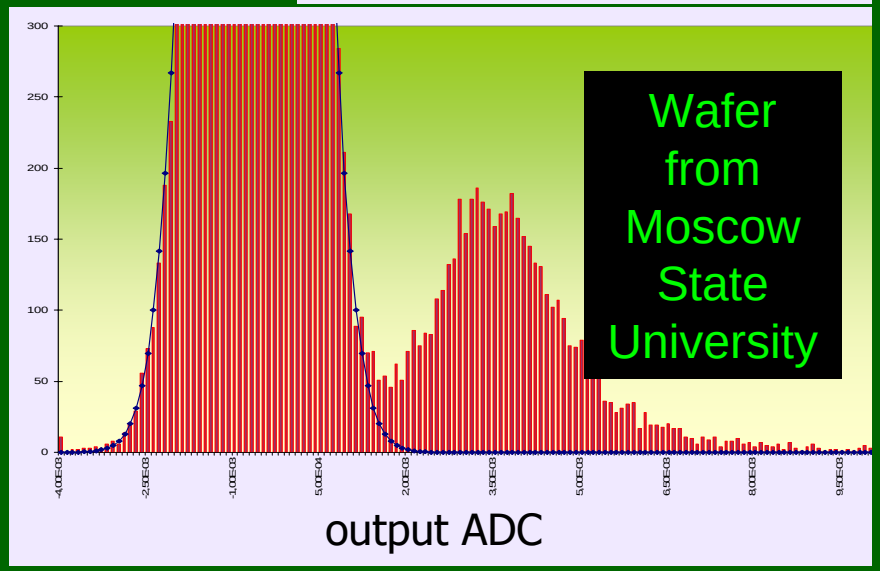


"external" signal

Sr^{90} source ➔ trigger ➔ read 6 channels
Only ONE with signal

$$\frac{MIP}{Noise} \approx 7.5$$



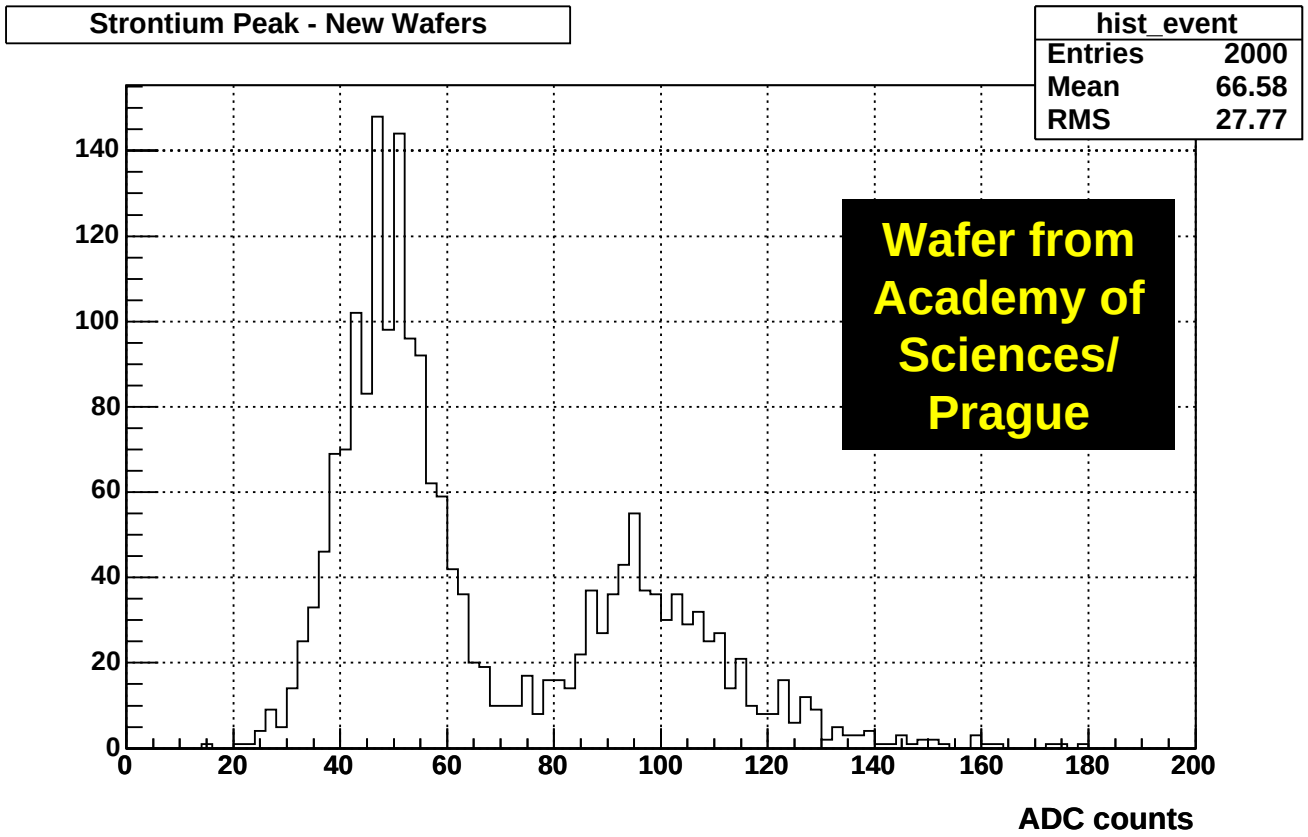


First test with a complete detector slab

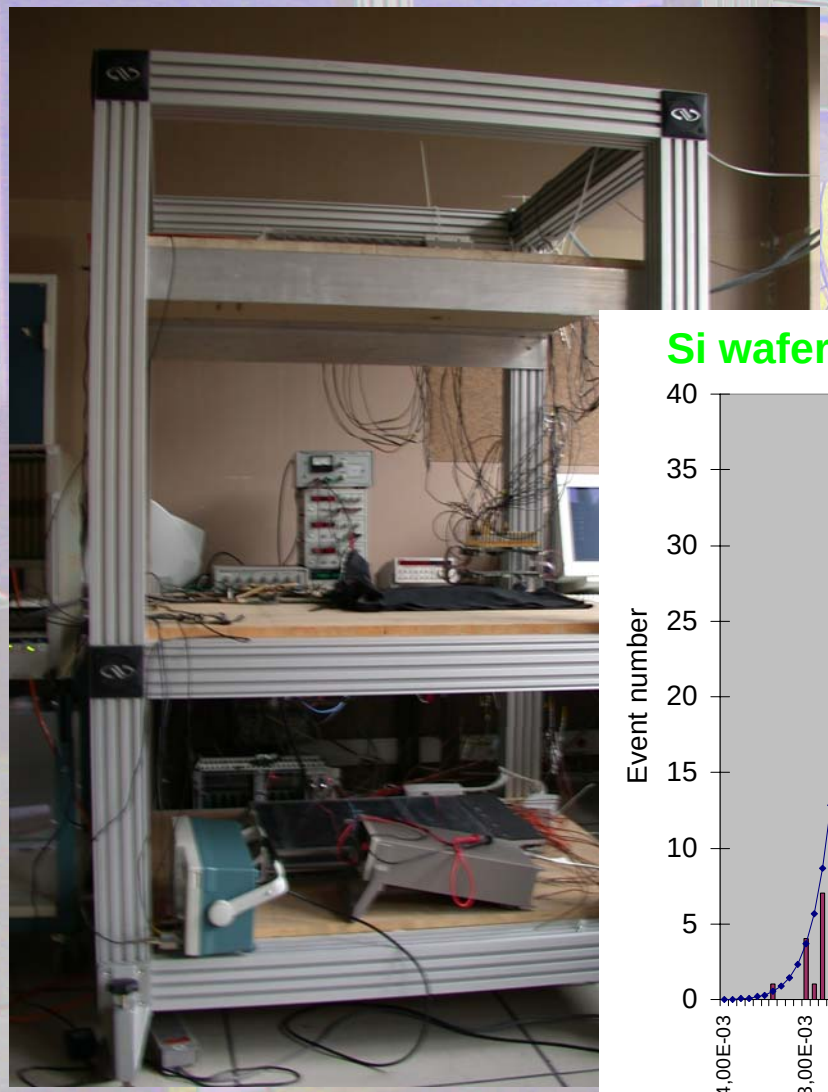
Si wafer - glue - PCB - VFE – DAQ (Full proto DAQ)
and ground with Al. EMC shield

LLR : S.Chollet, F.Gastaldi, A.Karar, J-Ch. Vanel
LAL : J.Fleury
Imp. Col. : P. Dauncey, D. Bowerman, C. Fry

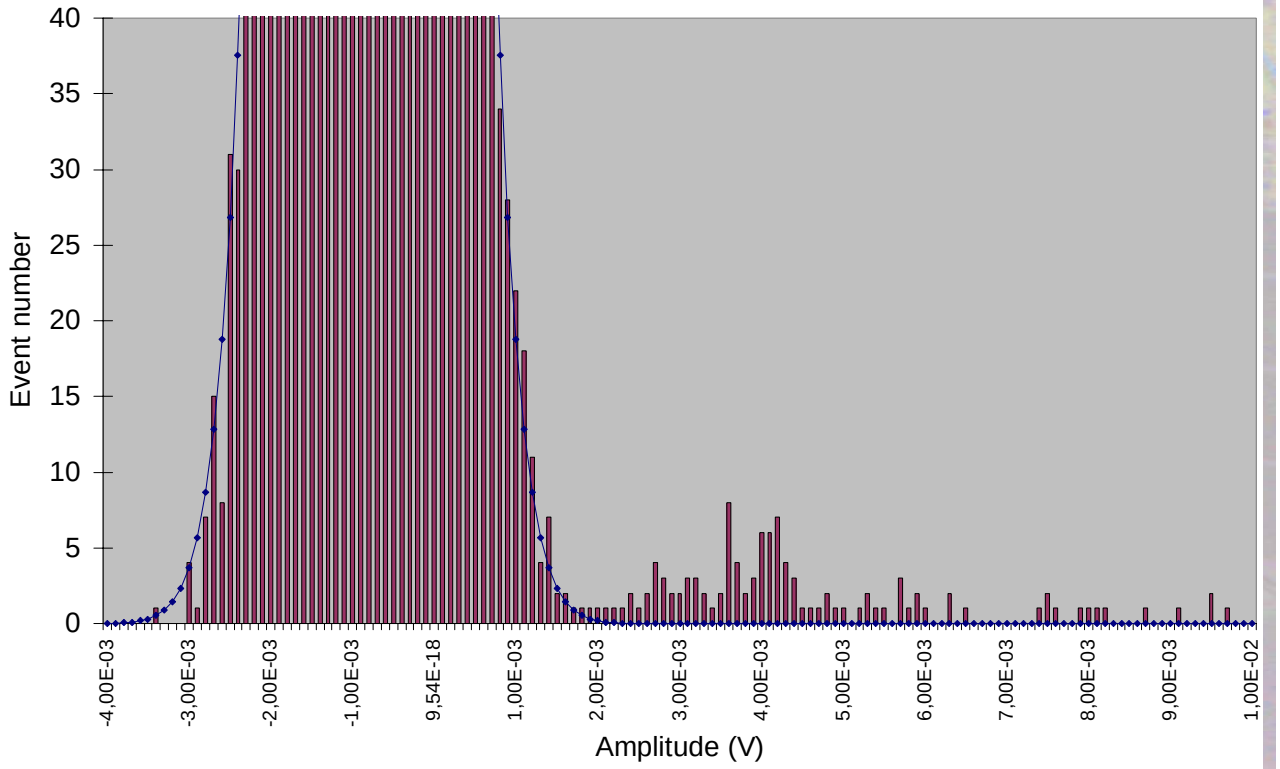
Sr^{90} source ➔ trigger ➔ read 1 channel



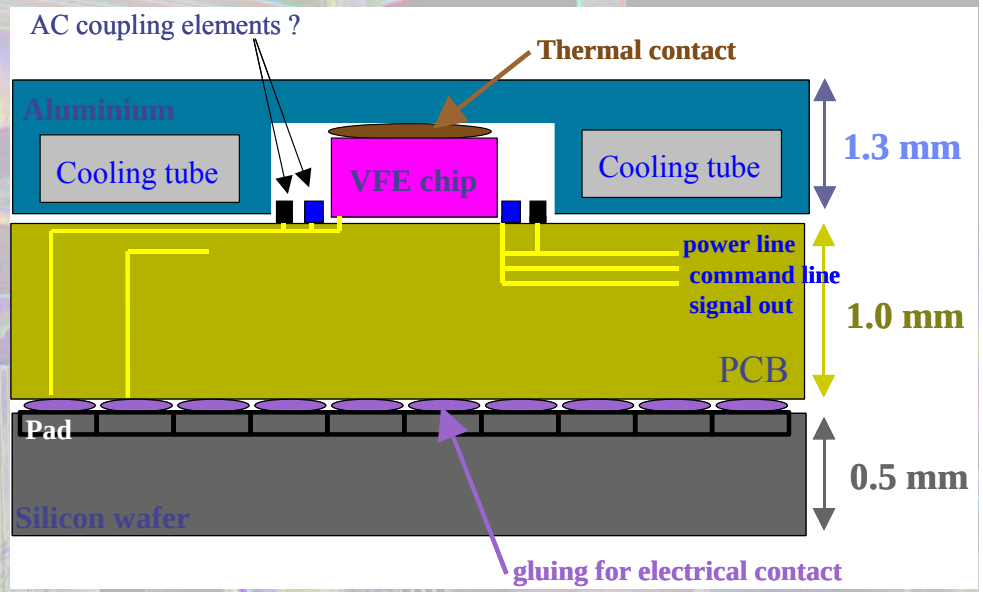
Cosmic test bench



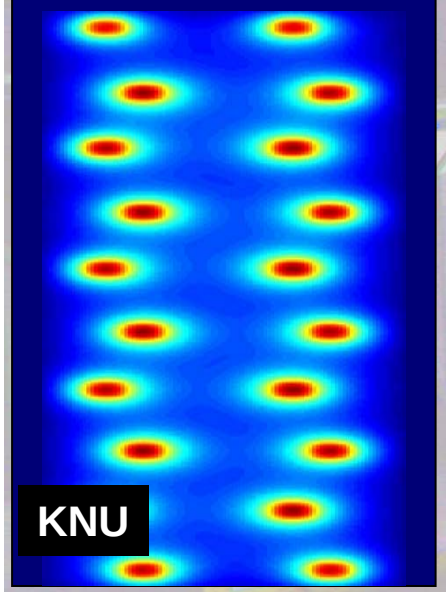
Si wafer - glue - PCB - VFE - PCB – DAQ (Single Slab DAQ)



R&D



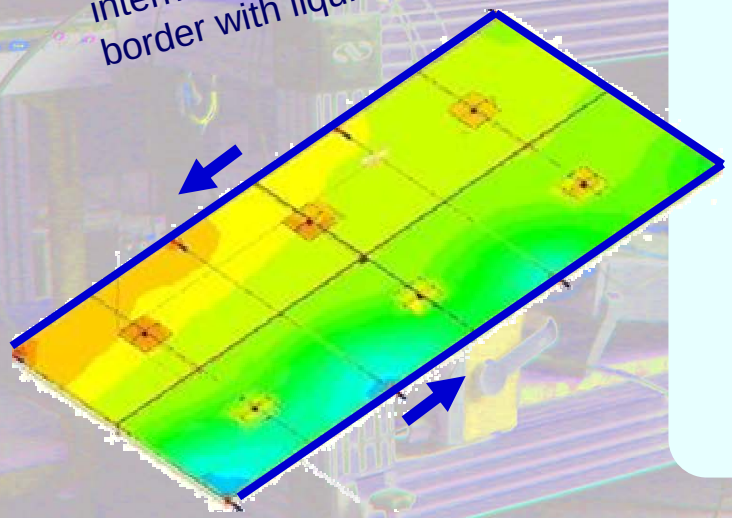
First test with/without cooling (top Al. plate) and VFE inside



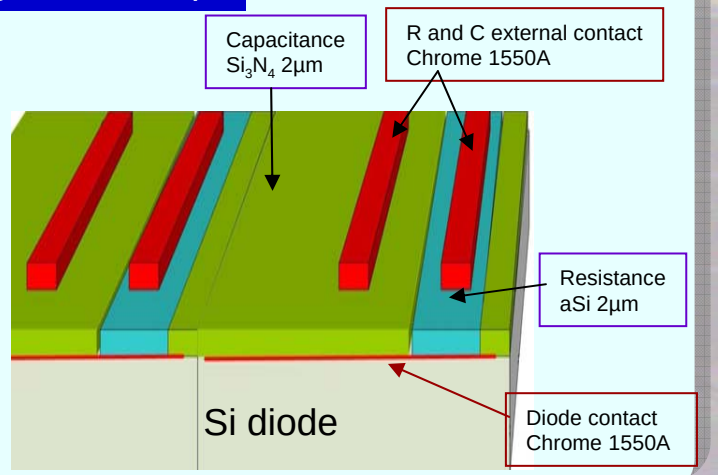
LLR

SAMCEF Simulation

Thermal dissipation with internal cooling at the border with liquid flow



R and C for AC coupling using thin film technique



The ECAL prototype schedule

March – November 2004

Assembling and testing on a cosmic test bench

Intercalibration of the 10K channels and overall debug !

~December 2004 at DESY (Low energy electrons E<6 GeV)

First test beam

2005-2006 at FNAL/IHEP/SLAC ? (electrons/pions/protons up to ~80 GeV)

test beam with HCAL ...

R&D in ECAL-CALICE

2004-2007

¶ VFE inside detector

Study of the new geometry ¶ with the impact of HE e.m. shower in the chip

- Optimisation of the interaction VFE-chip / cooling
- ADC-DAQ board with low consumption, small dimension, >100 channels/board

CALICE