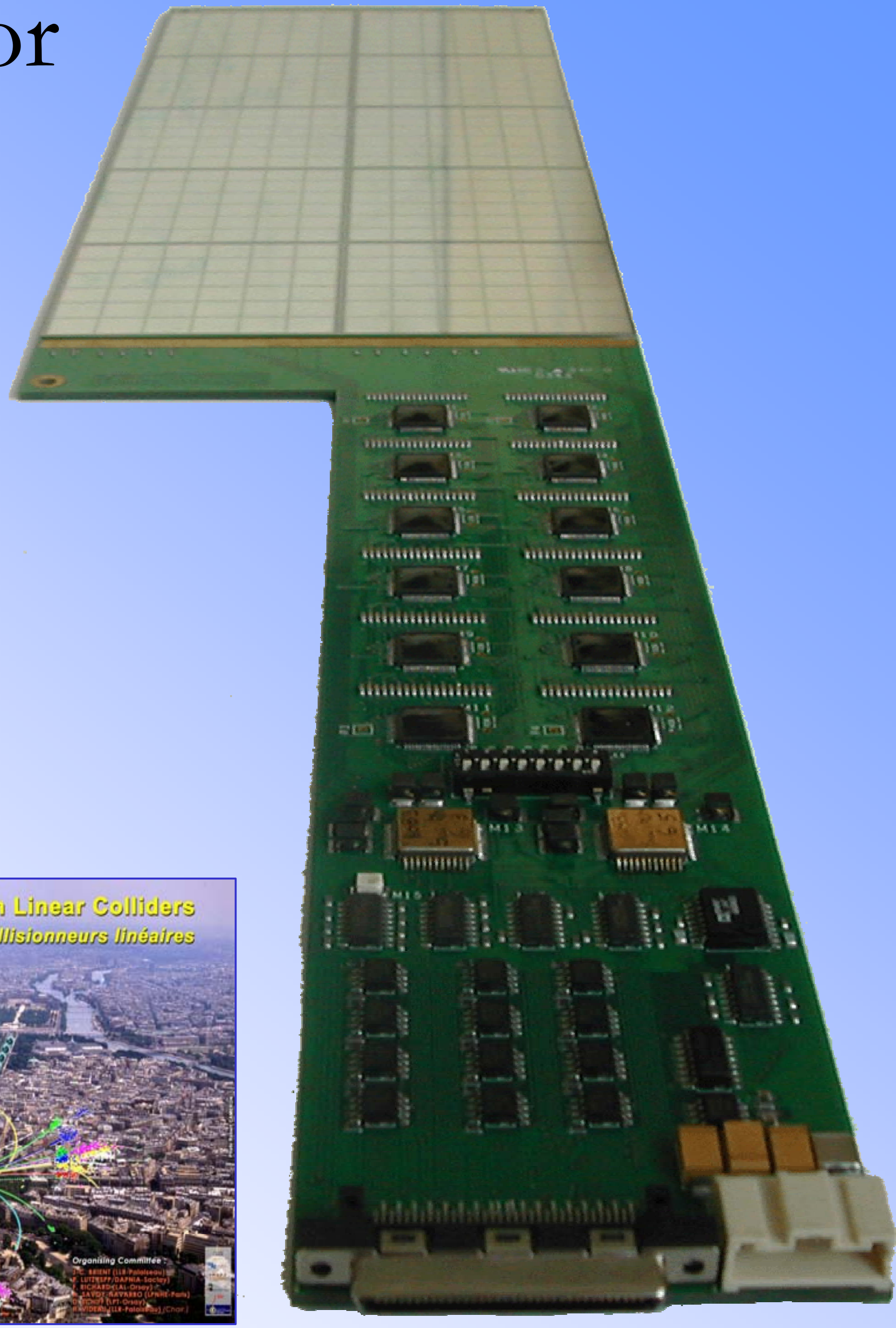
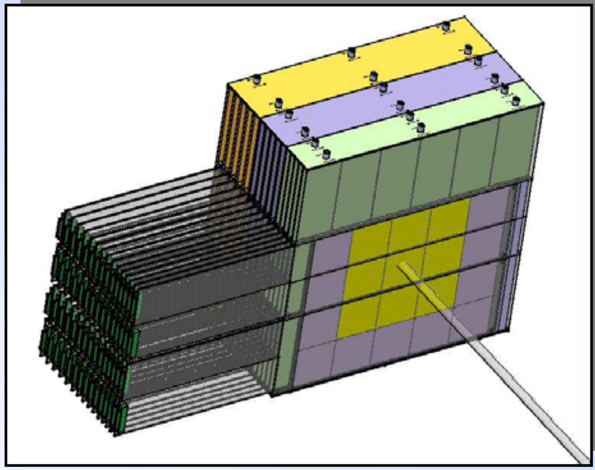
Front-end electronic for Si-W calorimeter

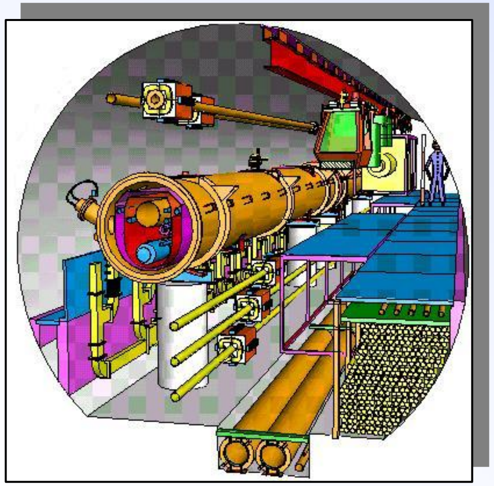


Sylvie Bondil
Julien Fleury
Christophe de La Taille
Gisèle Martin
Ludovic Raux

Plan

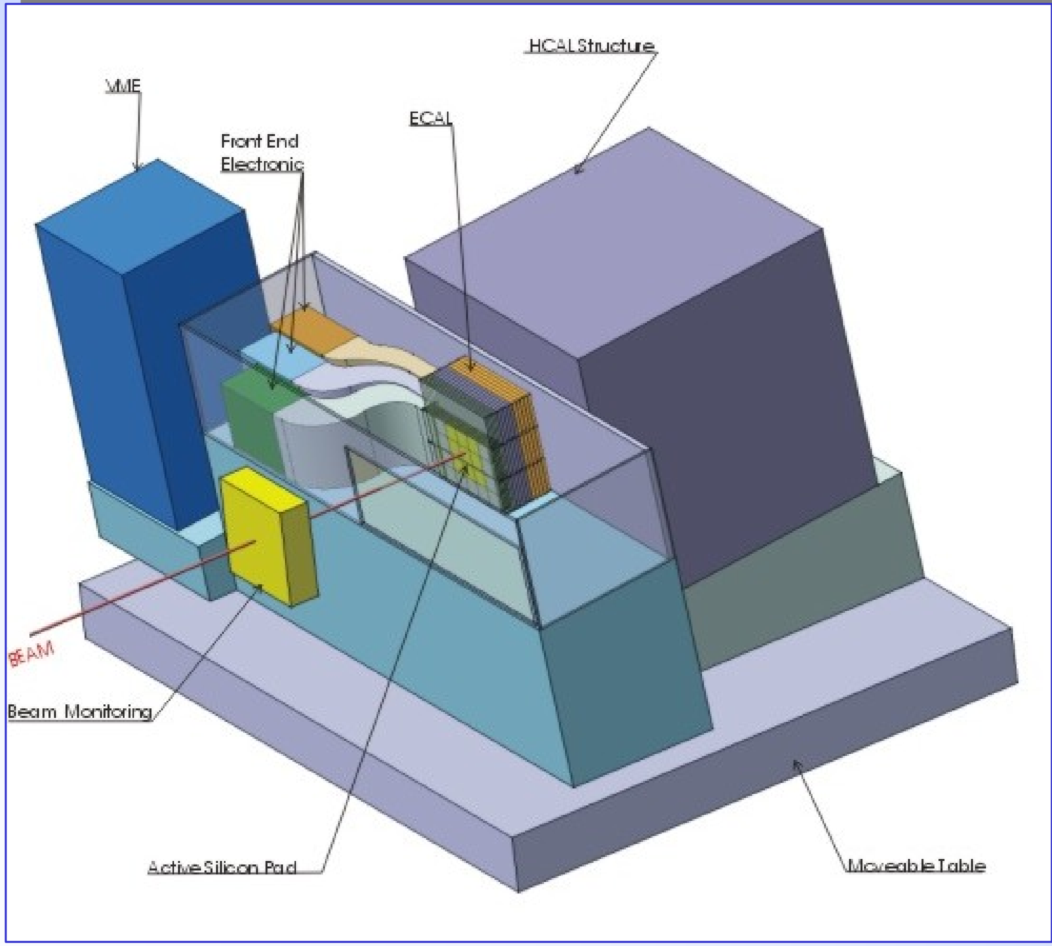


Electronic for a physics prototype



Electronic for a technologic prototype

Front-end Electronic for Physic Prototype



Presentation of the front-end electronic

6 active wafers

Made of 36 silicon PIN diodes

→ 216 channels per board

Each diode is a 1cm² square

2 calibration switches chips

6 calibration channels per chip

18 diodes per calibration channel

12 FLC_PHY3 front-end chip

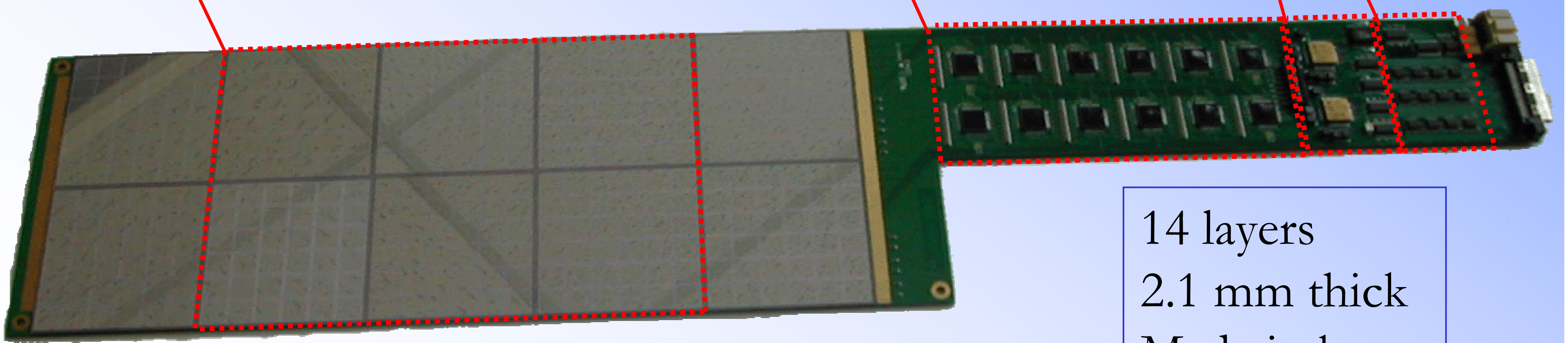
18 channels per chip

13 bit dynamic range

Line buffers

To DAQ part

Differential



14 layers

2.1 mm thick

Made in korea

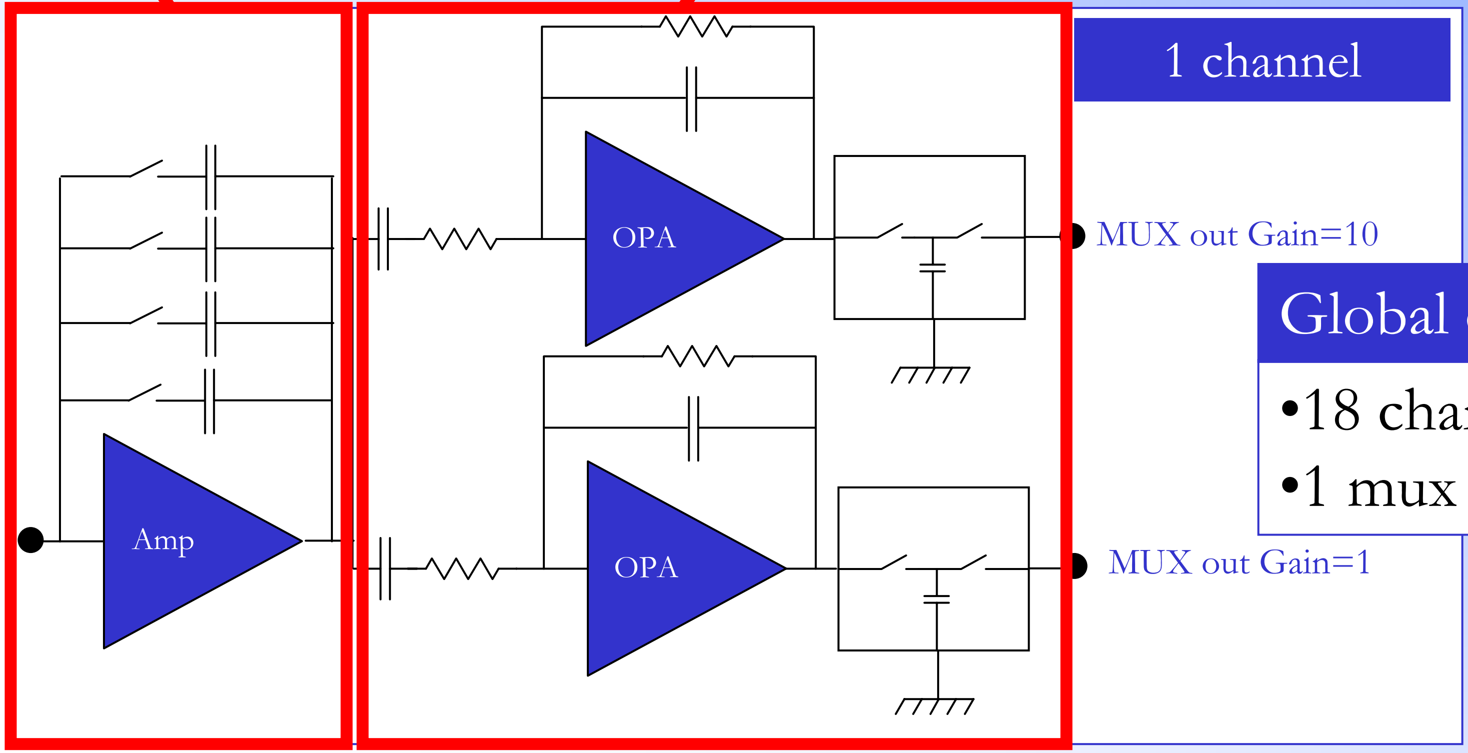
FLC_PHY3 overview

Multi-gain charge preamp

- 4 bits for gain selection
- Gain from 0.3 to 5 V/pC
- Gain selected offline

Dual shaper & track and hold

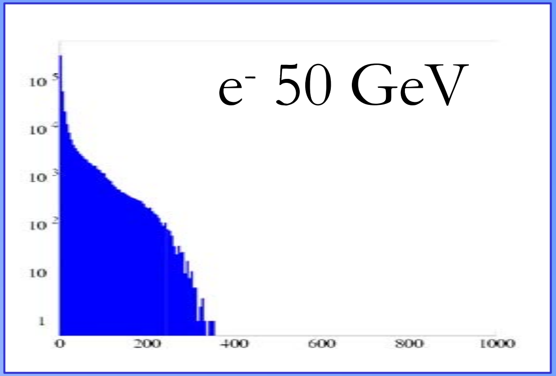
- Gain 1 and gain 10
- Work in parallel to select gain *a posteriori*



Global characteristcs

- 18 channel input
- 1 mux output

FLC_PHY3 meas. Results - Linearity



Measured input charge swing

Within ‰ linearity :

$Q_{IN\ MAX}$= 6.04 pC (900 MIP) @Cf=3pF

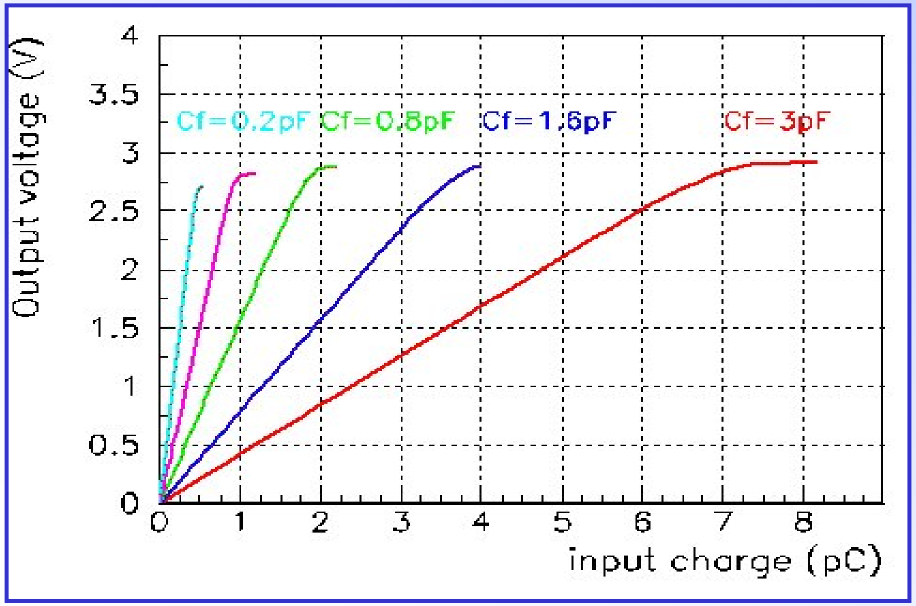
$Q_{IN\ MAX}$= 3.27 pC (500 MIP) @Cf=1.6pF

$Q_{IN\ MAX}$= 0.41 pC (60 MIP) @Cf=0.2pF

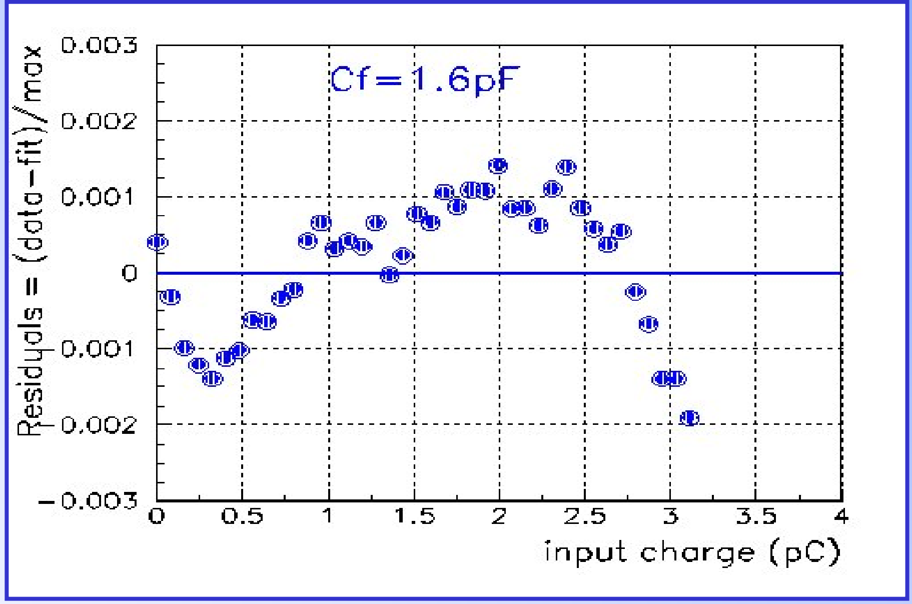
Measured Linearity

A few ‰ on every gain

Linearity curves (sweeping Cf / G1)



Residuals (Cf=1.6pF / G1)



FLC_PHY3 meas. Results - Transient

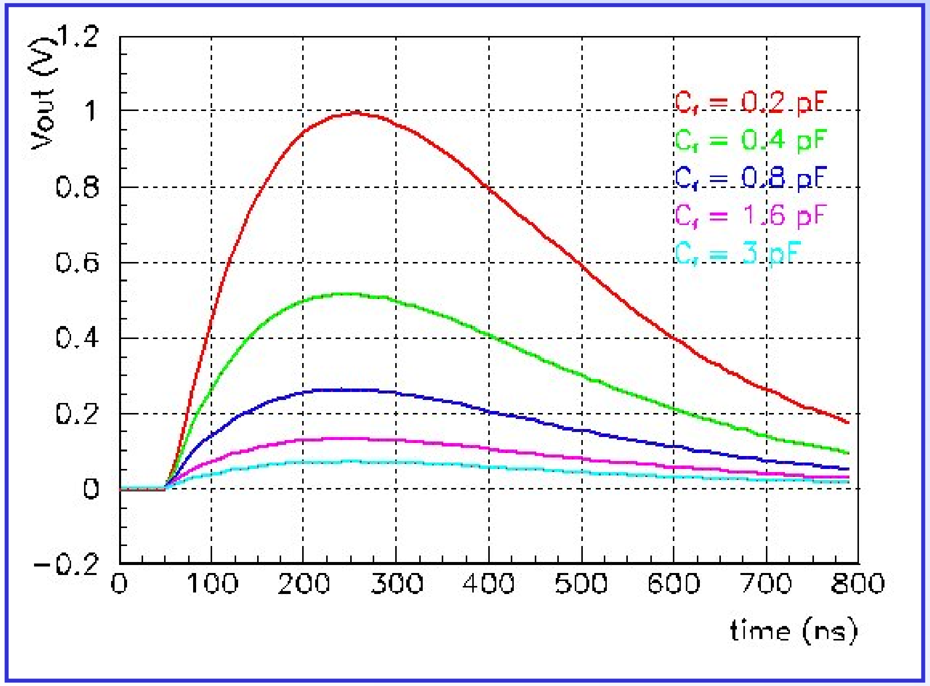
Peaking time uniformity

189ns ± 1% RMS @G1
174ns ± 1% RMS @G10

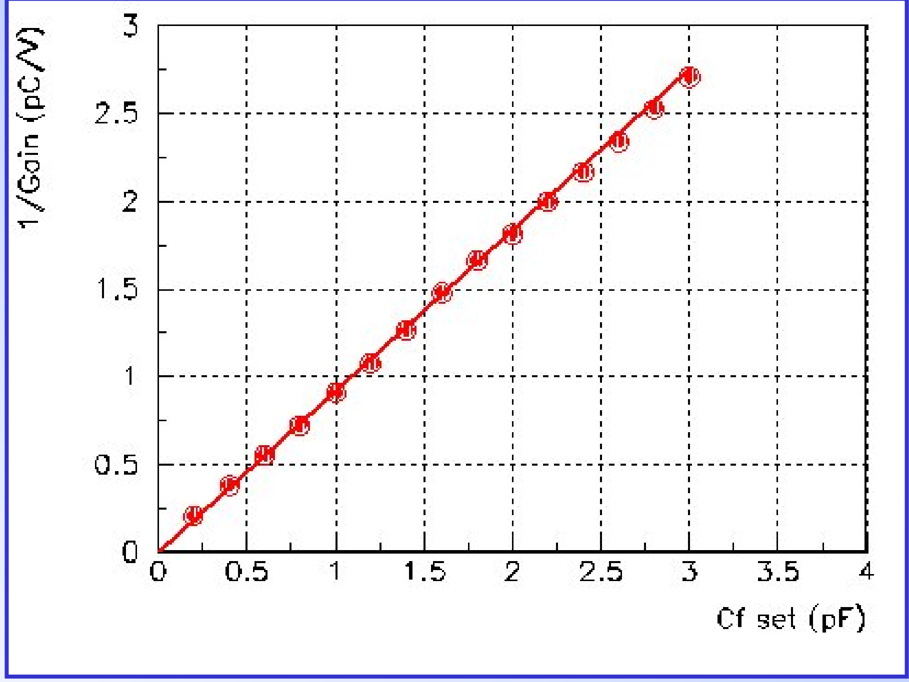
Gain uniformity @ Cf=1.6pF

696 mV± 2.5% RMS @G1
6.29 V ± 2.9% RMS@G10

Transient Output vs Gain (G1)



Gain vs feedback capacitance setting



FLC_PHY3 meas. Results - Noise

Noise

- Series : e_n = 1.6nV/√Hz
- Detector + line capacitance on physic proto : 70 pF

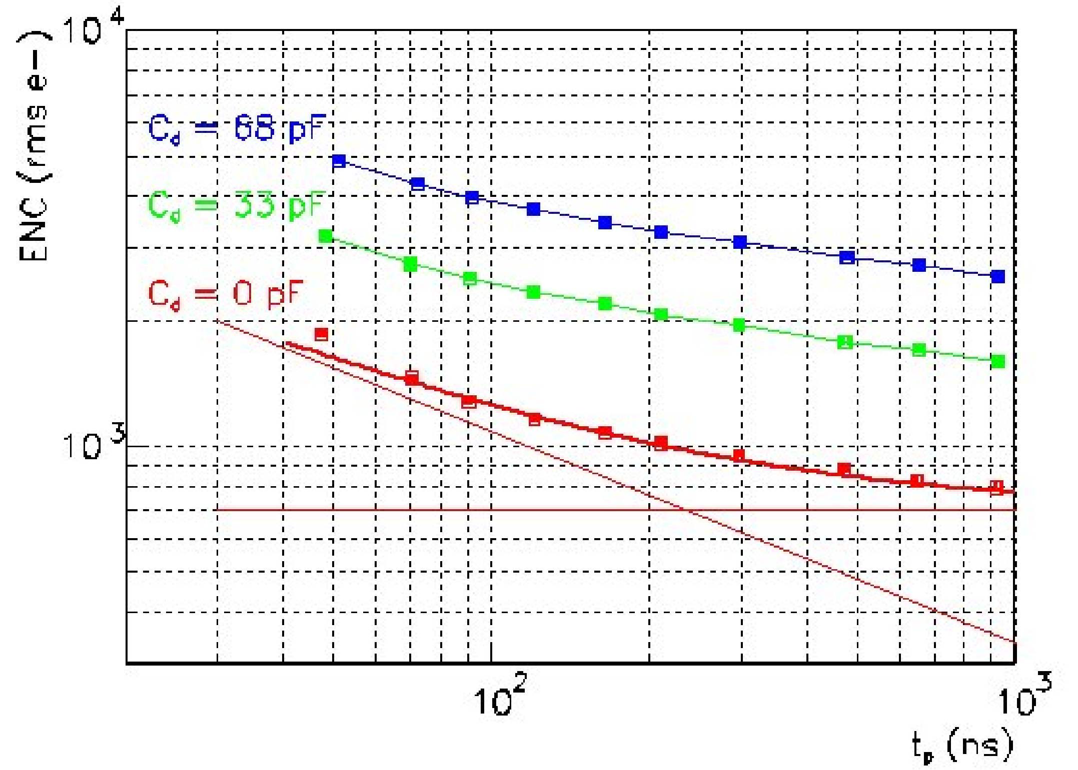
➔ ENC : 4000 e^- (1/10 MIP)

➔ Ouput noise : 500 µV RMS

Crosstalk

- Below 1 ‰ with gain 1 shaping
- Below 2 ‰ with gain 10 shaping

ENC measurement and fit (Cf=1.6pF)



Physic prototype front-end status

Status of front-end chip FLC_PHY

PRODUCTION DONE

-1840 chips are being packaged

-Automated Test Equipement for testing is ready

-Production will be ready for application in May

-Many spares lying around for other applications

Status of front-end PCB

READY FOR PRODUCTION

-Prototype has been debugged

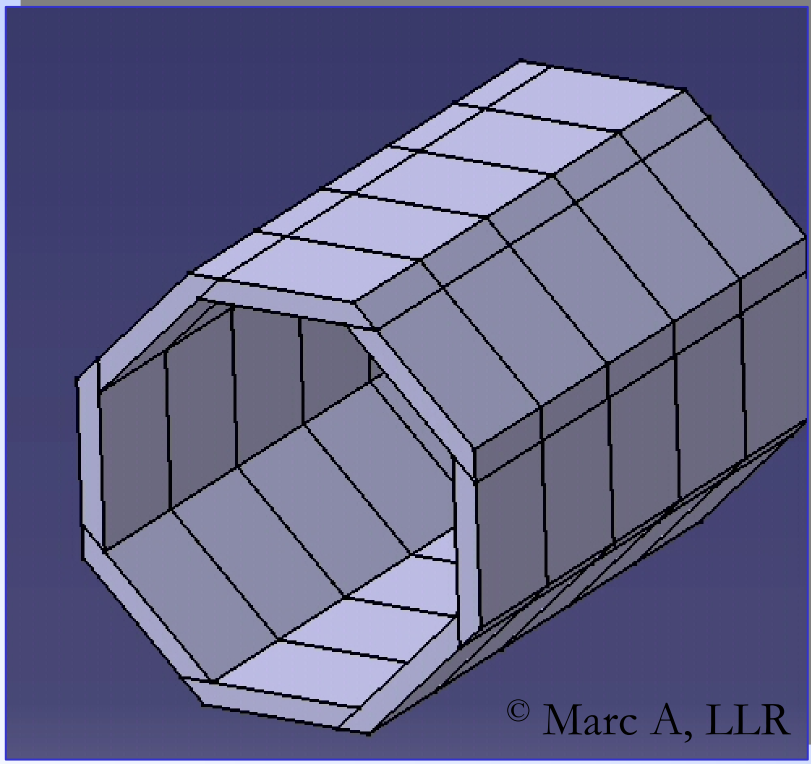
-Functionalities has been checked :

- -With Cosmic bench DAQ (for cross-calibration)
- -With test beam DAQ

-Pre-production has been sent in beginning April

-65 boards will be produced by the end of June

Front-end electronic for Technologic prototype



Technology choice

Our expectations

-Perennity :
No way the technology we choose dies before the production … in 20xx…
-Good digital performance :
It sounds clear that electronic for FLC will be mixed
-Good analog performance :
It still sounds clear that electronic for FLC will be mixed
-And of course, as cheap as possible

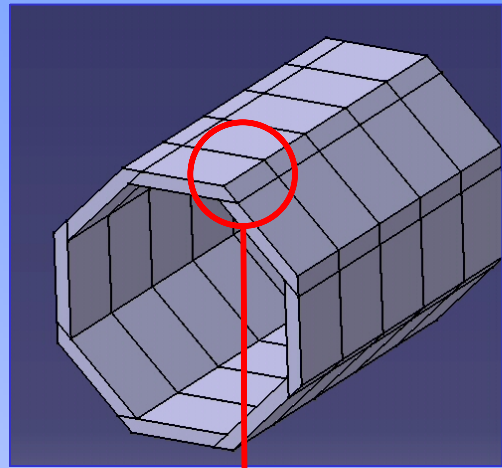
Our choice : AMS 0.35um CMOS (C35b4) and AMS 0.35 SiGe BiCMOS (S35b4)

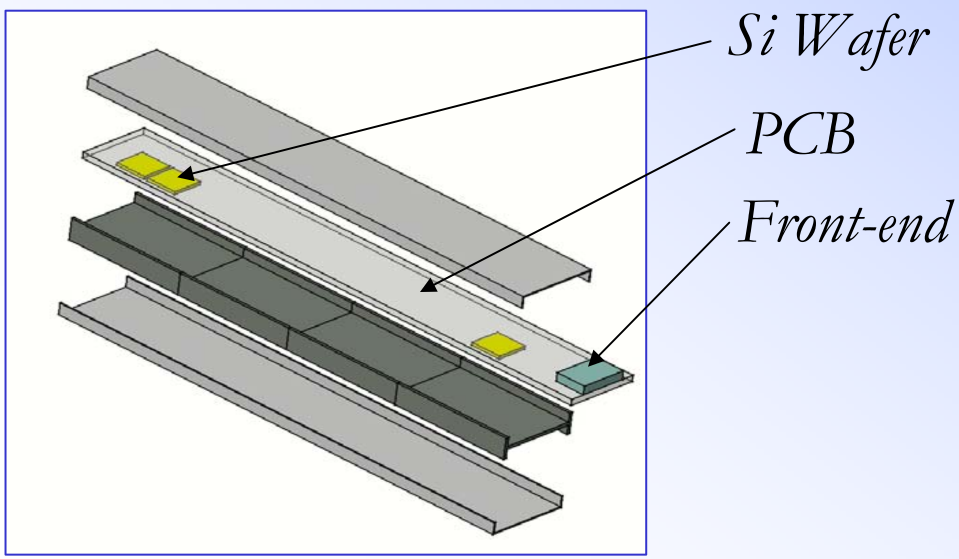
-Perennity :
used by car industry and RF industry who need « normal » voltage supply (3.3V)
-Good digital performance :
Transistors are small enough to go as fast as we need
-Good analog performance :
Transitors are big enough to allow a 3.3V supply and let room for analog voltage swing
-And of course, as cheap as possible
Big volume → cheap due to huge industrial customer

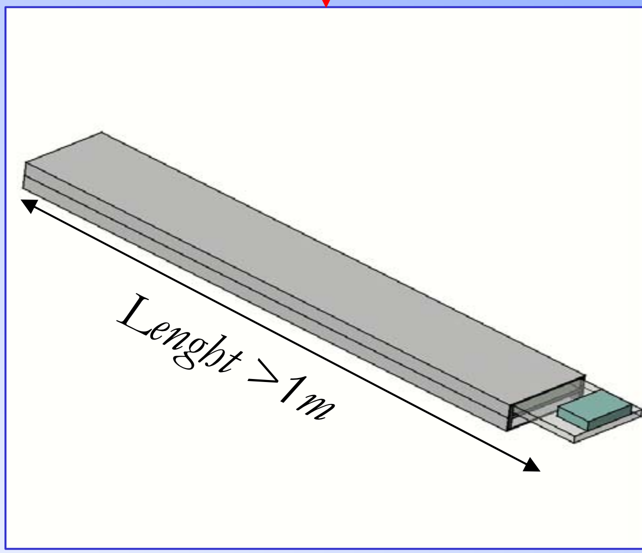
Electronic for a technologic prototype

What is in the TDR :

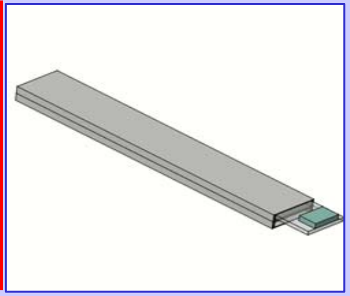
- Charge preamp, tri-gain shaper
- Auto-trigger + Analog memory
- Output : Channel ID, BCID, Energy
- Chips at calorimeter end, 128 channels/chip, 1 W







Alternative solution for electronic

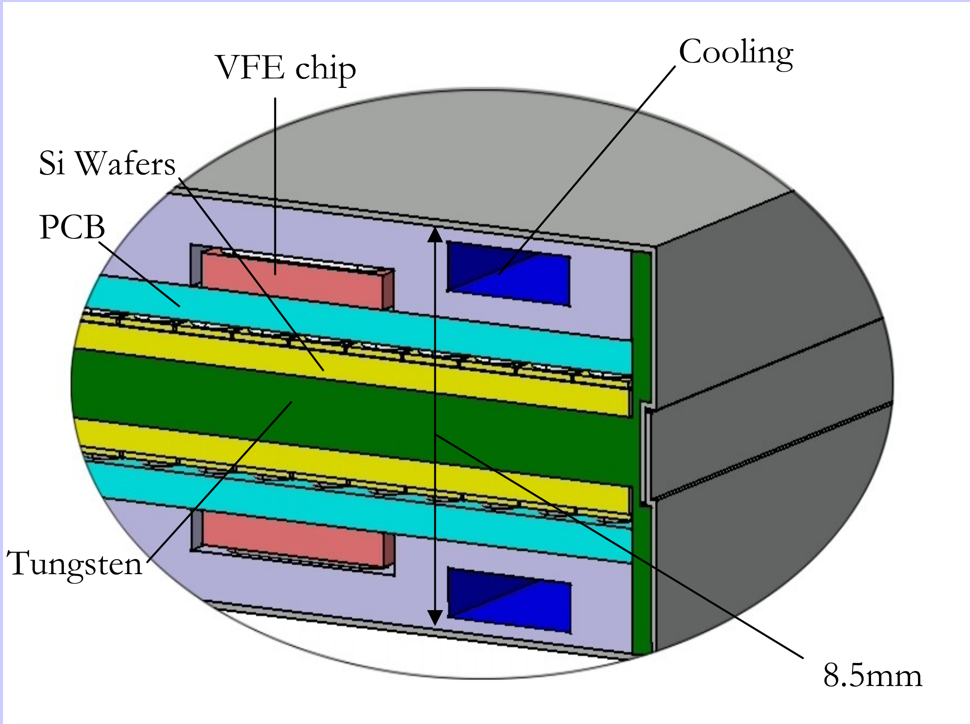


TESLA TDR solution

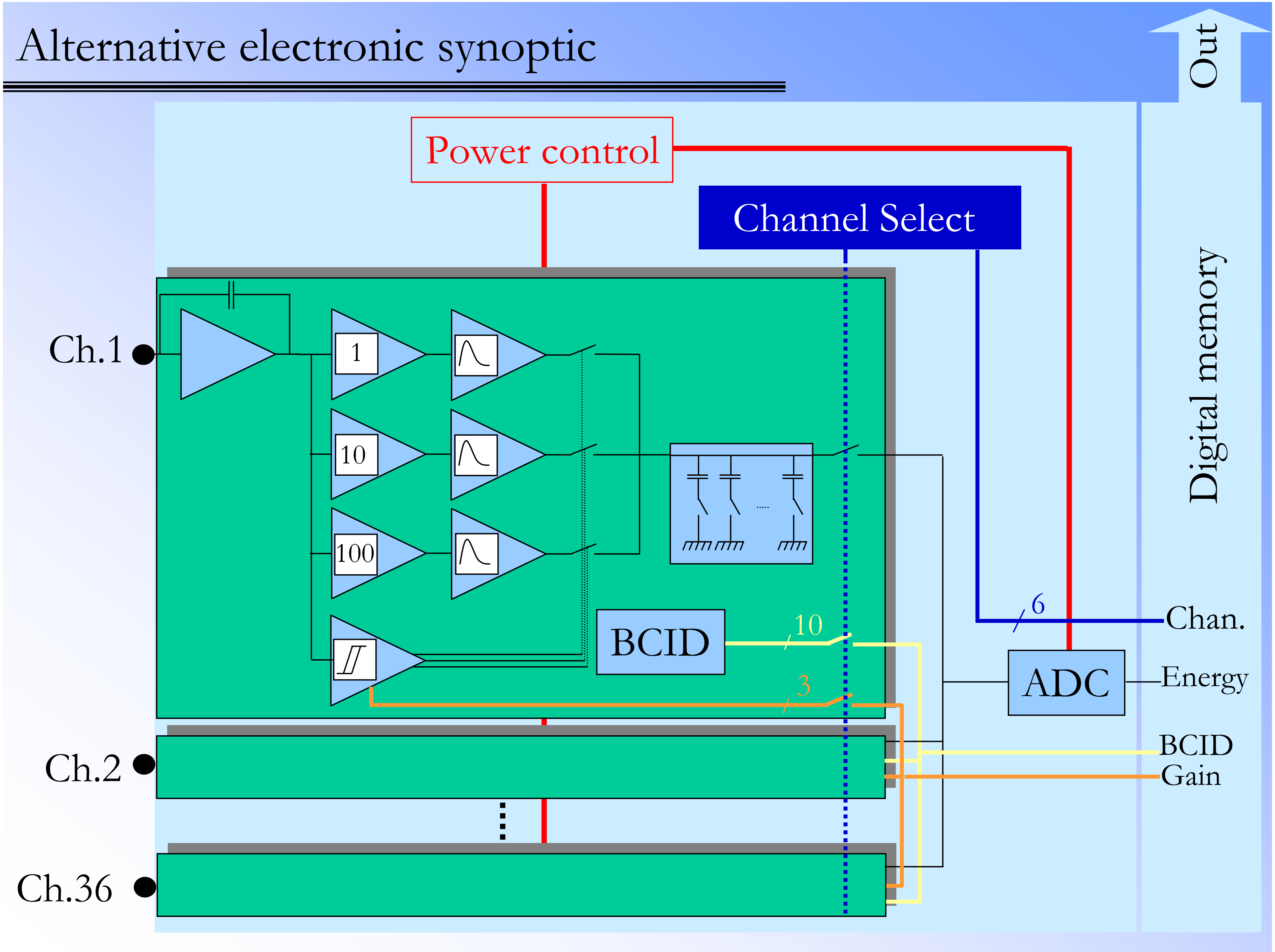
-Industry cannot build 1m PCB and tendance is *going smaller*
-High line capacitance → very noisy
-Big number of lines →crosstalk issue and many PCB layers

Alternative solution

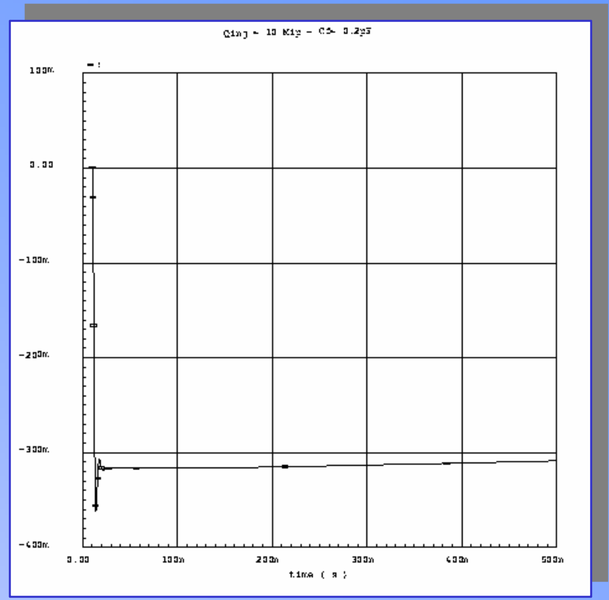
-Chip embedded in detector
-1 chip per wafer (36-channel chip)
-low power issue
-Cooling issues
-temperature distribution in module?
-Fake signal due to e.m. showers in chip ?



Alternative electronic synoptic



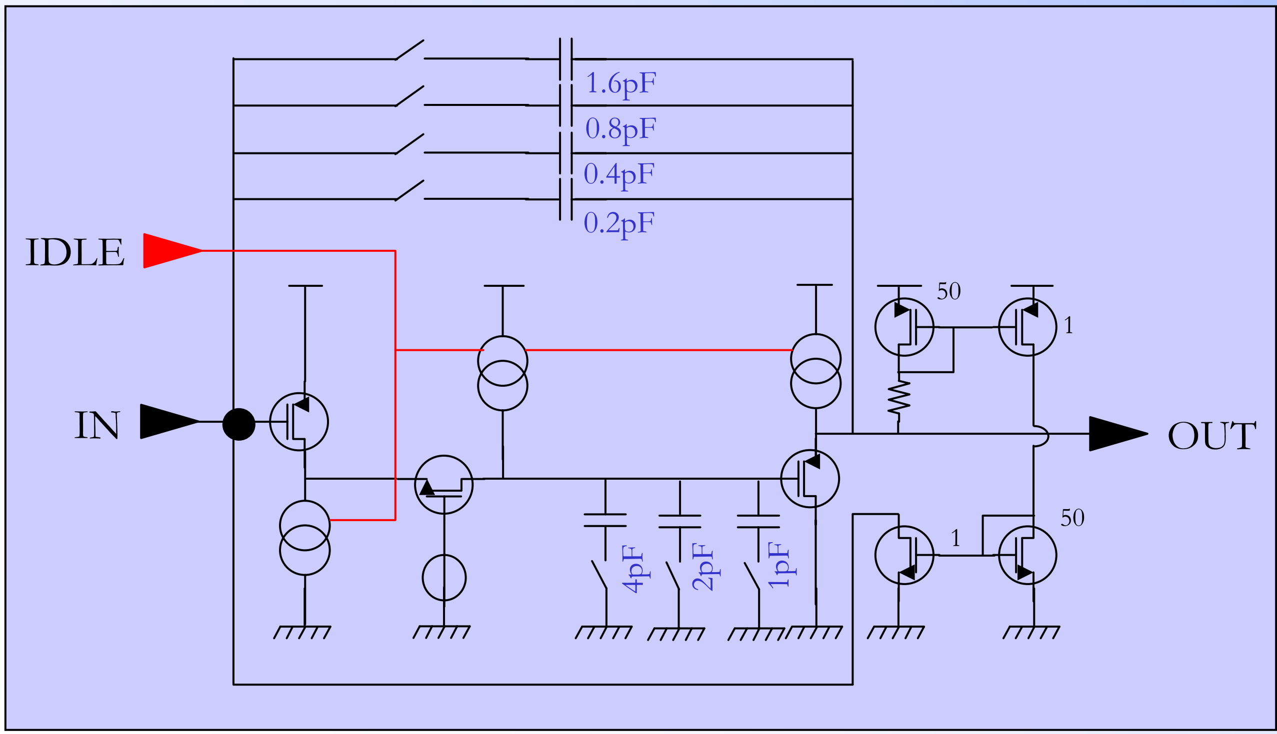
Charge preamp. for a techno prototype



Expectations :

- -Low noise : ~1nV/sqrt(Hz)
- -Low power : below 1mW
- -Settling time : around 2us

Technology	AMS 0.35 CMOS
Submission	April, 19th 2004



Shapers for a techno prototype

Op. amp. shaper

-Conservative version
-Peaking time : 200ns
-Low power : below 400uW
-Gain 1 & 10

Capacom shaper

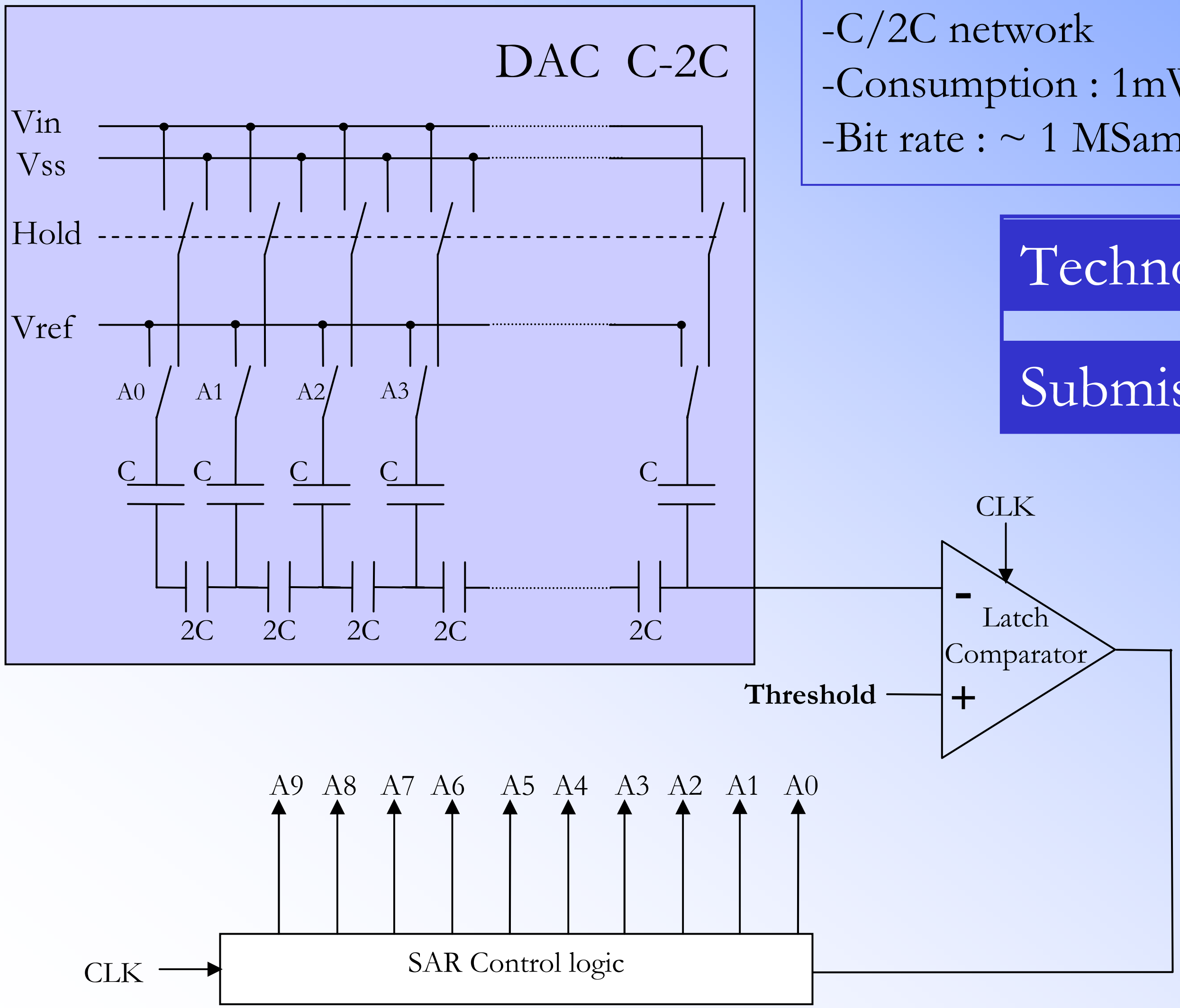
-Peaking time : variable from 100ns to 1us
-Low power : below 400uW
-Variable gain : from 1 to 15
-Auto-hold capability

Current feedback Op. amp. shaper

-Peaking time : 200ns
-Low power : below 400uW
-Gain 1 & 10
-High Gain-Bandwidth Product (>2GHz)

Technology	AMS 0.35 CMOS
Submission	April, 19th 2004

ADC for a techno prototype



SAR (successive approximation) ADC

- -10 bits
- -C/2C network
- -Consumption : 1mW
- -Bit rate : ~ 1 MSamples/s

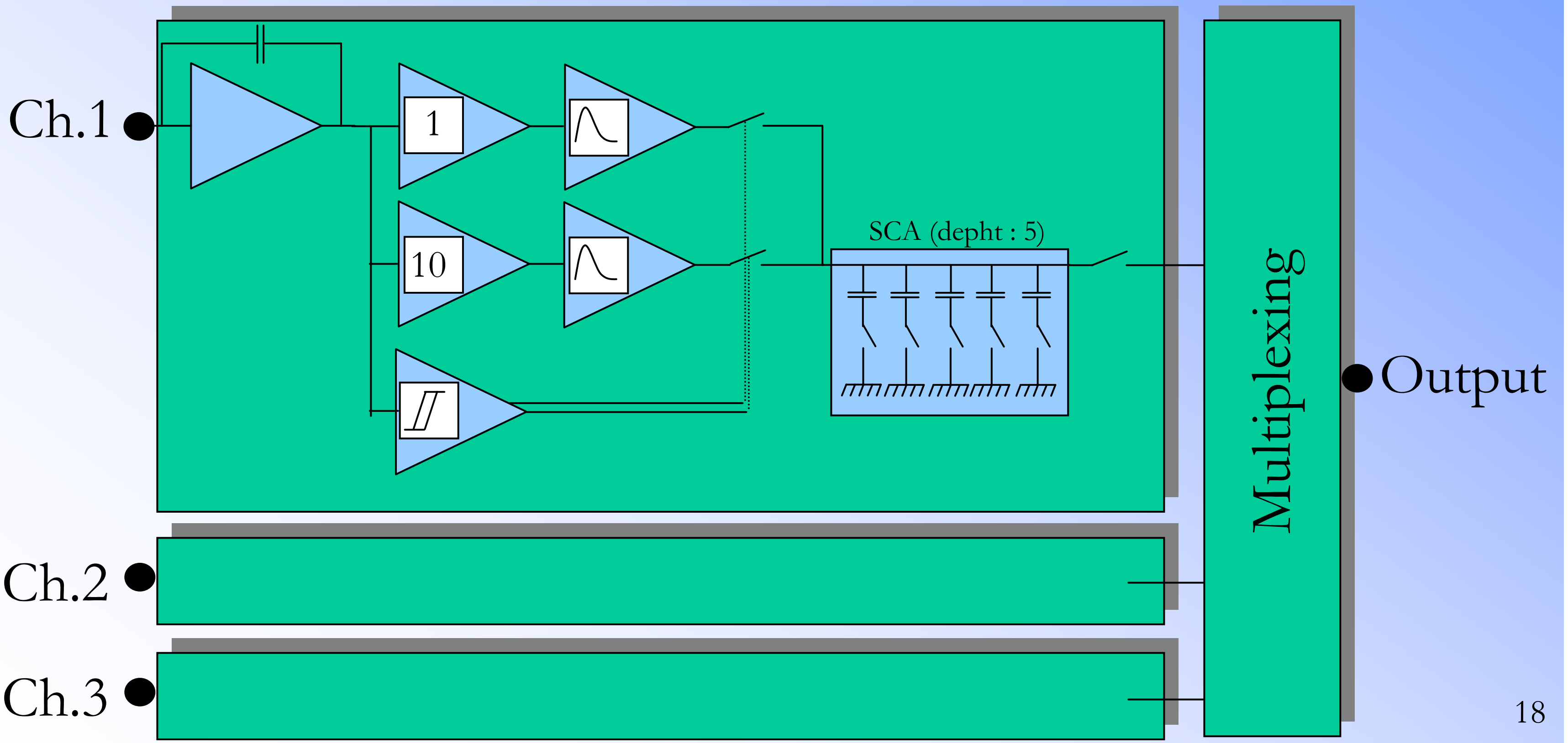
Technology	AMS 0.35 CMOS
Submission	April, 19th 2004

FLC_TECH : a first iteration

FLC_TECH description

- -3 channels
- -Multi-gain charge preamplifier
- -2 shaping : gain 1 and gain 10
- -5-depht SCA
- -Multiplexed output, auto-trigger and Idle mode

Technology	AMS 0.35 CMOS
Submission	April, 19th 2004



LPC contribution to techno prototype

10 bits low power high speed pipeline ADC

LPC Clermond-Ferrand, Fr

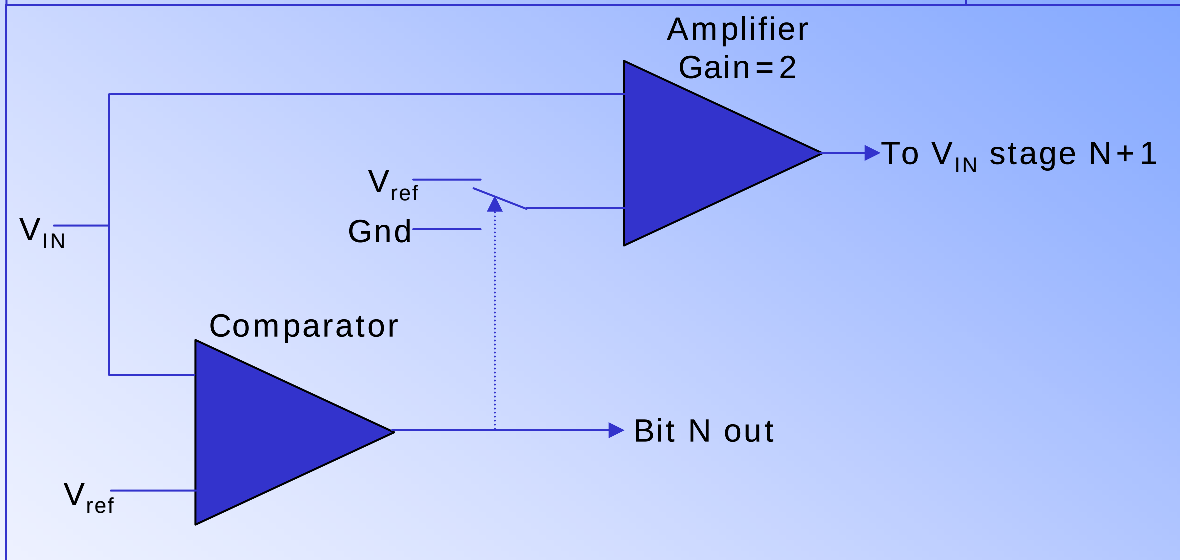
-Gerard Bohner
-Pascal Gay
-Jacques Lecoq
-Samuel Manen

Performance

-10 bit
-up to 5MS/s (Clk @ 50 MHz)
-Consumption around 10mW

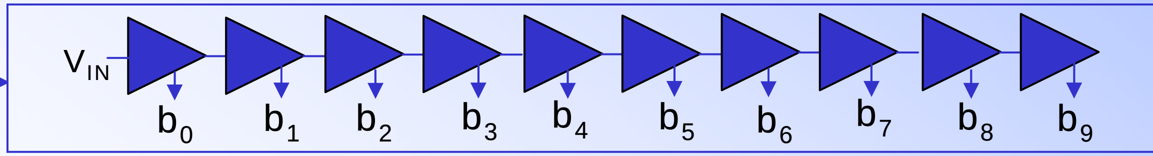
Status

-First iteration (AMS 0.8 CMOS) is working well
-New iteration (AMS 0.35 CMOS) submitted in April, 19th



Stage N of pipeline ADC block schema

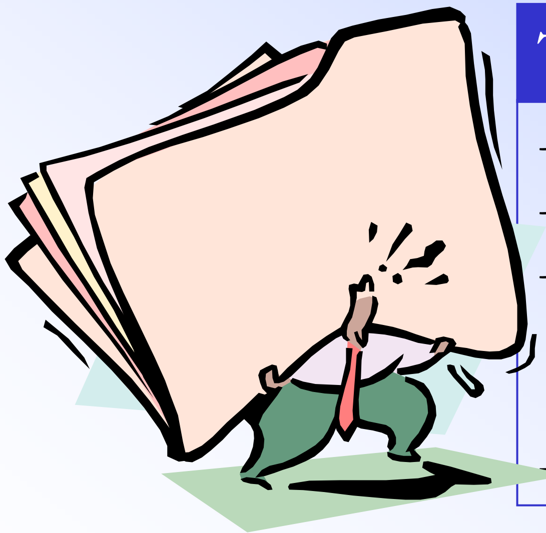
10 bit ADC
→10 stages



Conclusion

Physic prototype

-Beginning of production
-On time, so far
-Ready for test beam in dec. 2004
-Good start point for techno proto



Technologic prototype

-Working on *embedded chip* solution
-Many blocks in design
-Focus on low power issue
    -Pulsed supply
    -Low power design
-Big work to do on ADC

Questions