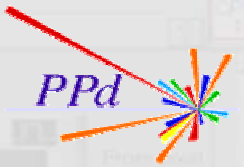


LCFI Collaboration Status Report

LCWS 2004

Paris

Joel Goldstein

for the LCFI Collaboration

Bristol, Lancaster, Liverpool, Oxford, RAL

LCFI Research Programme

R&D for a vertex detector at NLC or TESLA

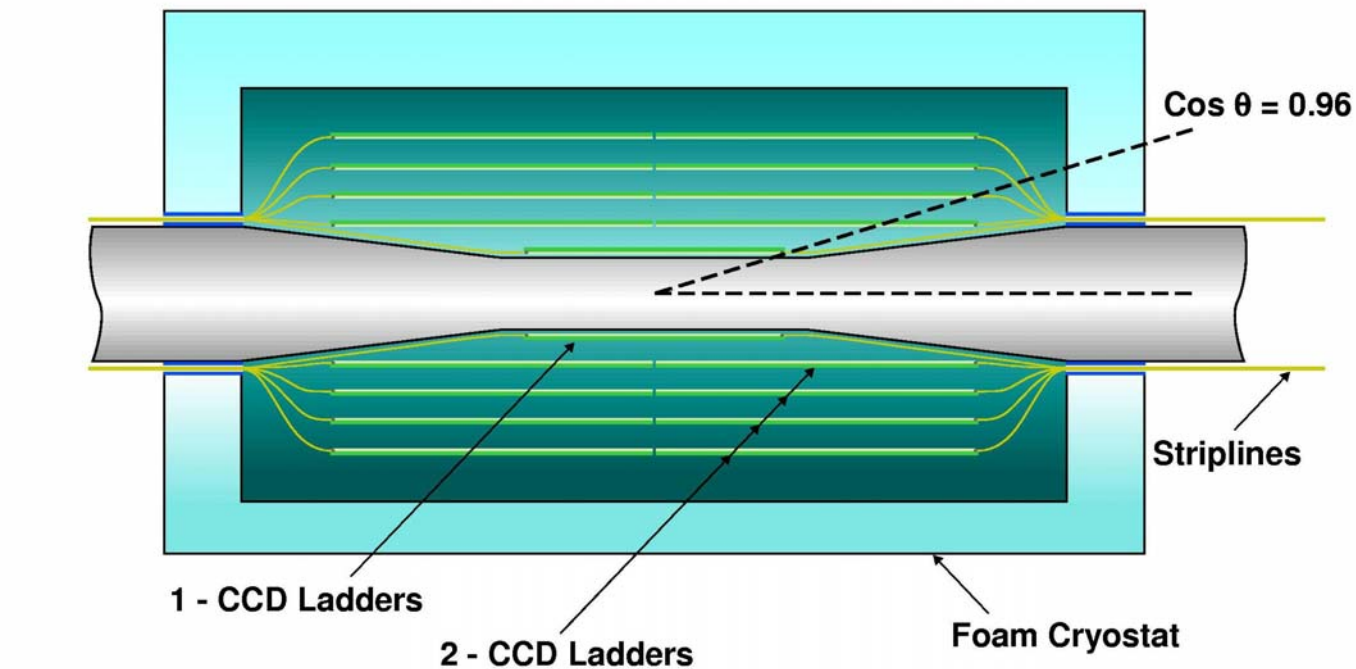
1. **Physics Studies**

   (See Sonja Hillert's talk in Simulation session)

2. **Mechanical Development**
   - **Ultra low-mass ladders**
   - **FEA/physical models**

3. **Detector Development**
   - **Fast CCD technology** (50 MHz for TESLA)
   - **Custom CMOS readout chips**

LC Vertex Detector



- **800 Mchannels of 20×20 μm pixels in 5 layers**
- **Optimisation:**
  - **Inner radius (1.5 cm?)**
  - **Readout time (50 μs?)**
  - **Ladder thickness (0.1% X_0?)**

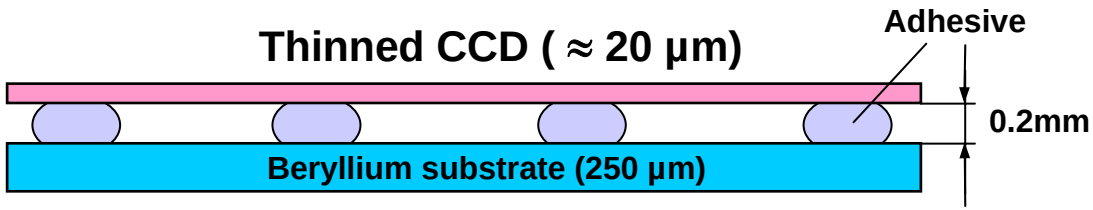
Mechanical Options

Target of 0.1% X_0 per layer

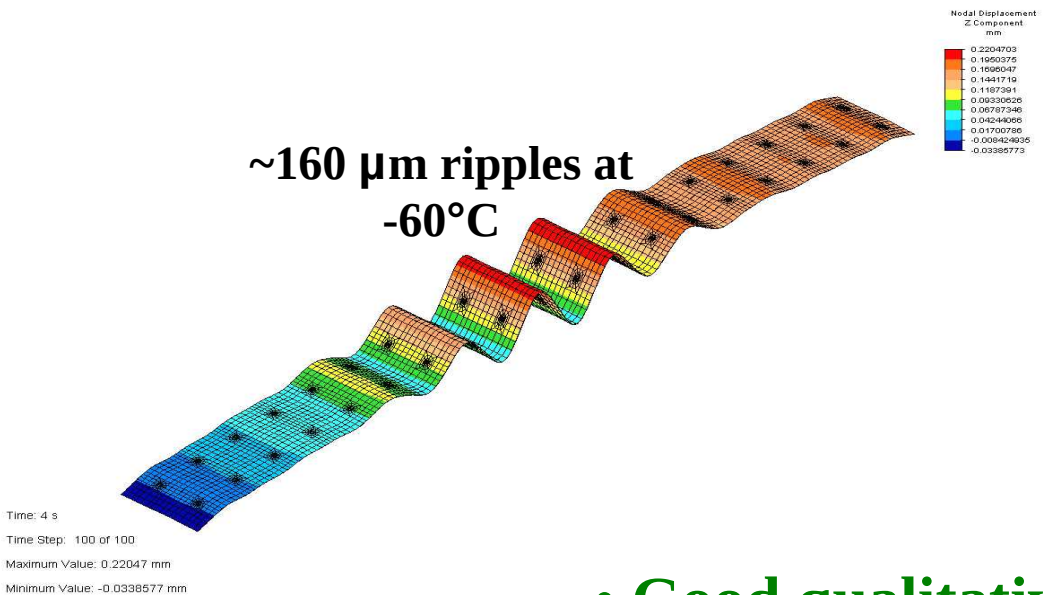
(100μm silicon equivalent)

1. **Unsupported Silicon**
   - Longitudinal tensioning provides stiffness
   - No lateral stability
   - Not believed to be promising
2. **Semi-supported Ultra-thin Silicon**
   - Detector thinned to epitaxial layer (20μm)
   - Silicon glued to low mass substrate for lateral stability
   - Beryllium has best specific stiffness
   - Composites, ceramics, foams...
3. **Novel Structures**

Mechanical Studies of Be-Si

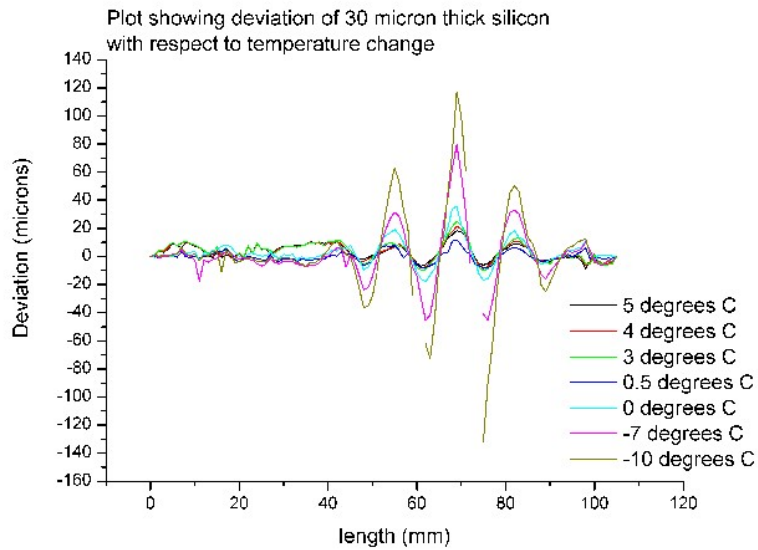


FEA Simulations



Physical Prototyping

- **Laser survey system**



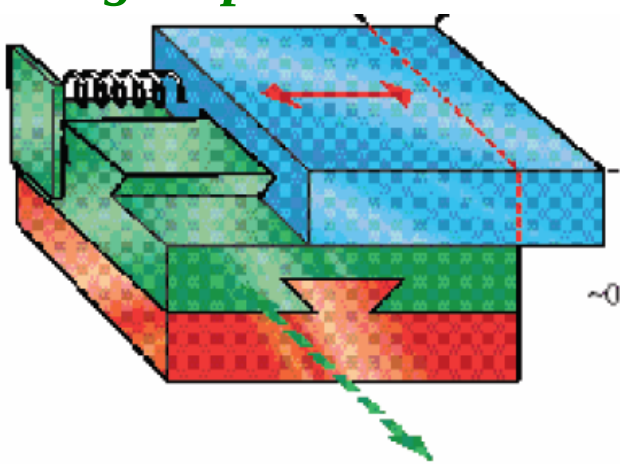
- **Good qualitative agreement**

New Approaches

- **Be-Si unstable when cooled due to CTE mismatch**
- **Choose substrate with closer CTE match**
  - **100 µm carbon fibre**
  - **ceramic foam**
- **Micromechanical techniques....**

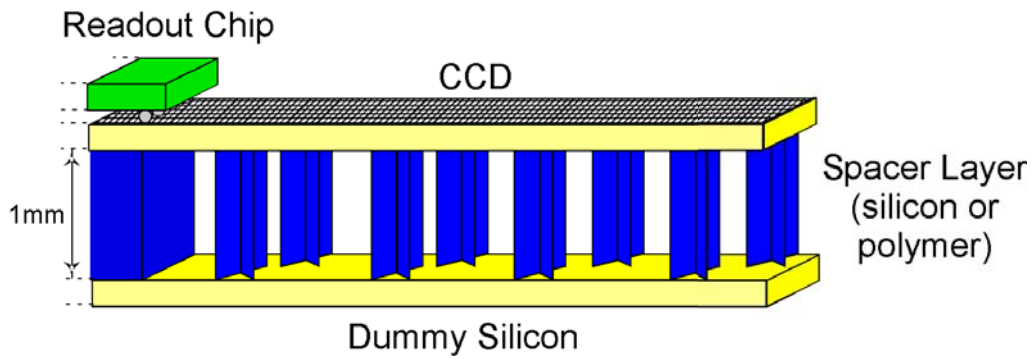
Microstages

replace glue pillars



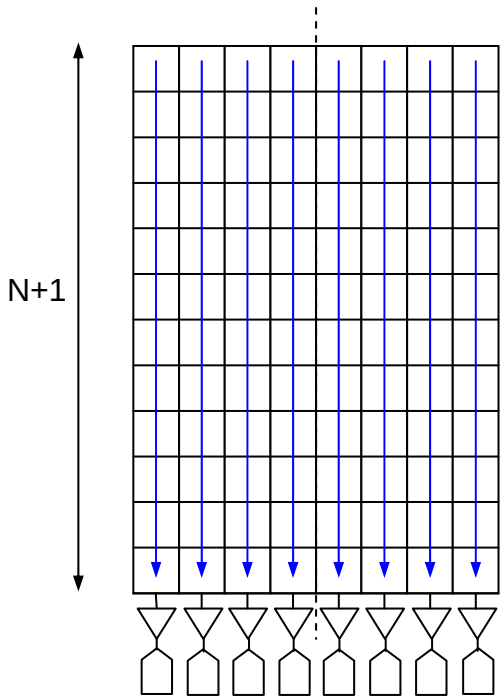
Sandwich

UV lithography on dummy

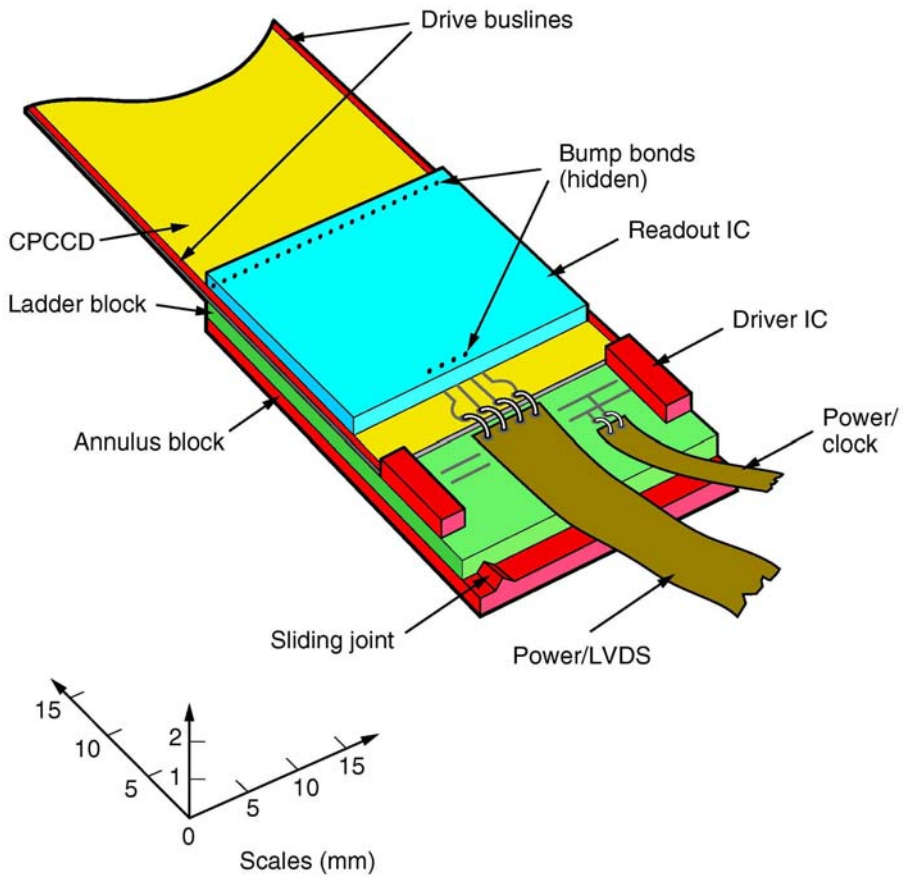


Column Parallel CCD

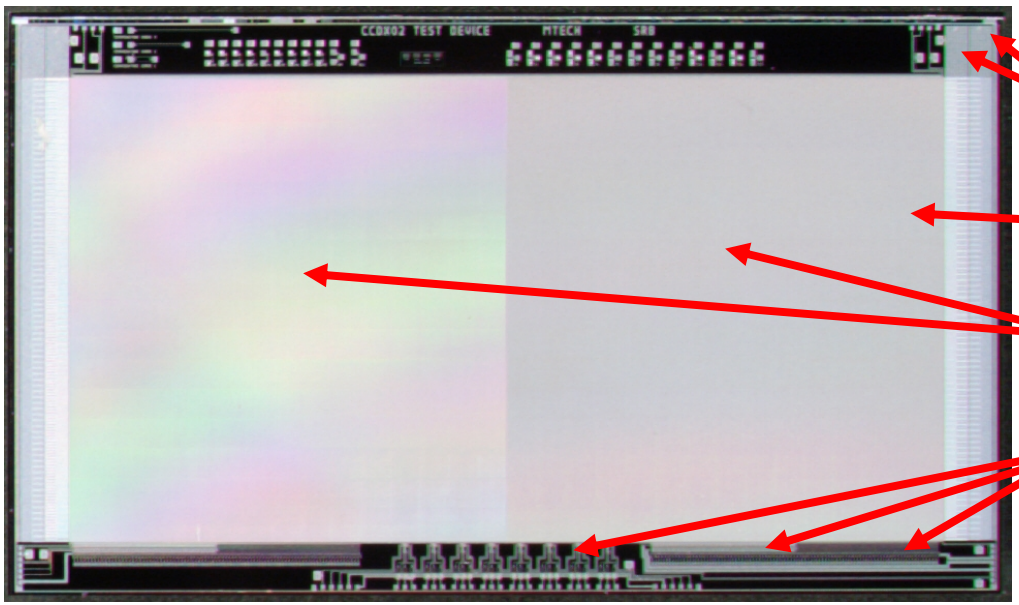
- **Separate amplifier and readout for each column**



Column Parallel CCD
Readout time = $(N+1)/F_{out}$



Prototype CP CCD



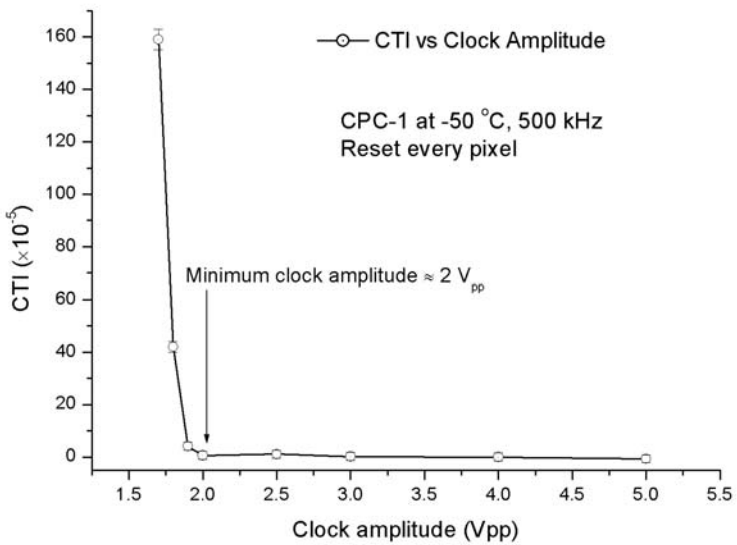
CPC1 produced by E2V

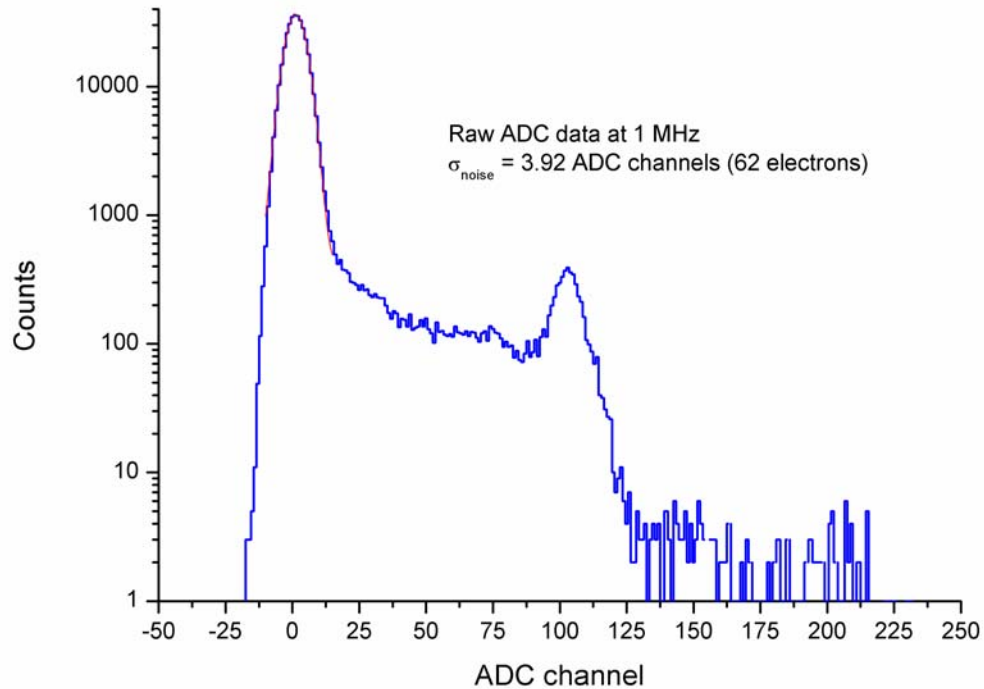
- Two phase operation
- Metal strapping for clock
- 2 different gate shapes
- 3 different types of output
- 2 different implant levels

➢ *Clock with highest frequency at lowest voltage*

CPC1 Results

- **Noise ~ 100 electrons (60 after filter)**
- **Minimum clock ~1.9 V**



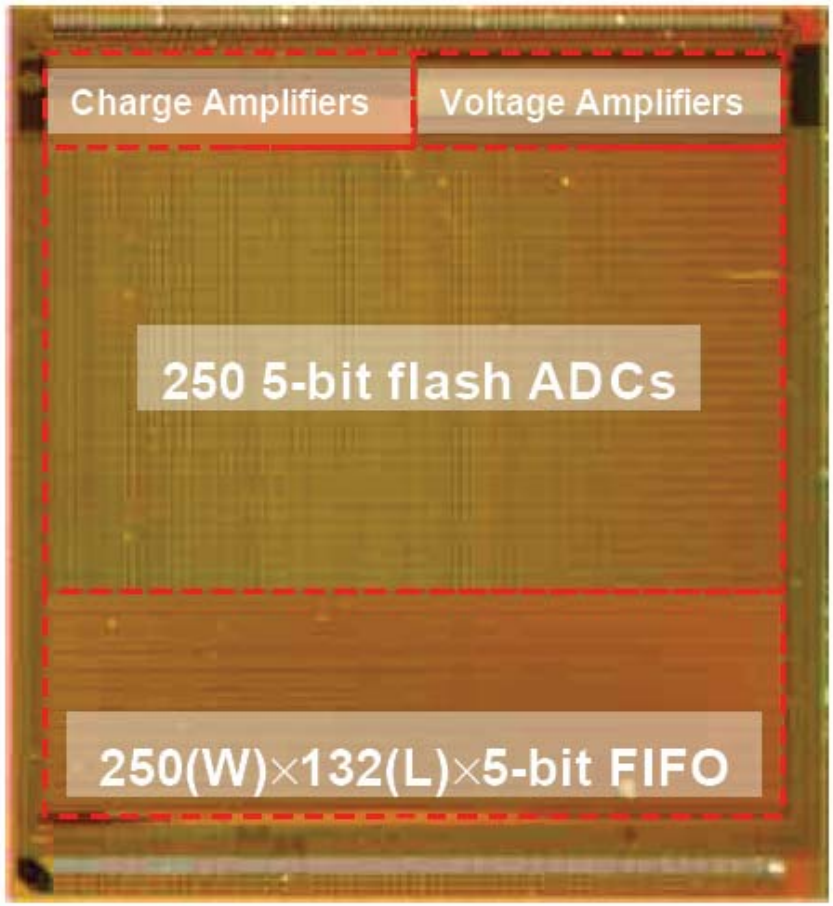


- **Maximum frequency > 25 MHz**
  - **inherent clock asymmetry**

CP Readout ASIC

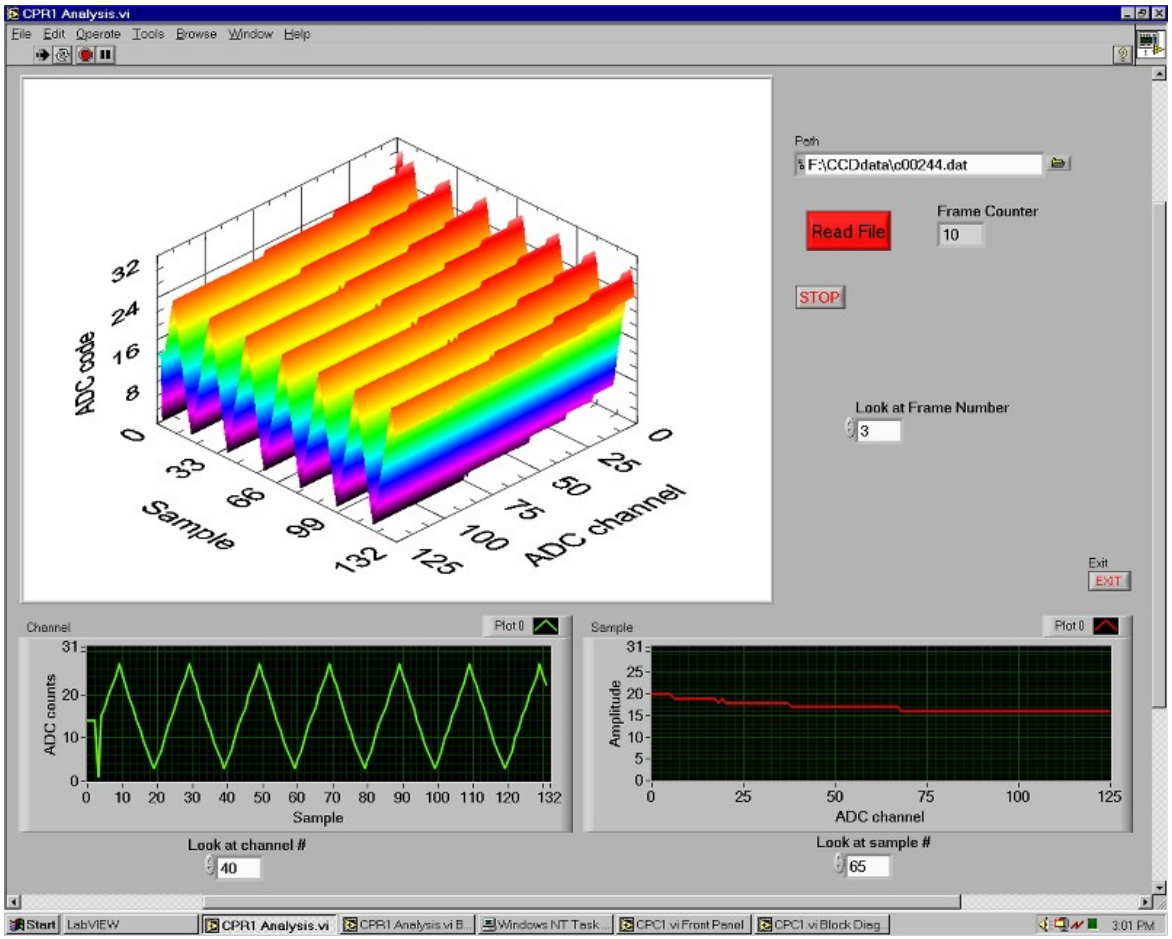
CPR1 designed by RAL ME Group

- **IBM 0.25 µm process**
- **250 parallel channels with 20µm pitch**
- **Designed for 50 MHz**
- **Data multiplexed out through 2 pads**



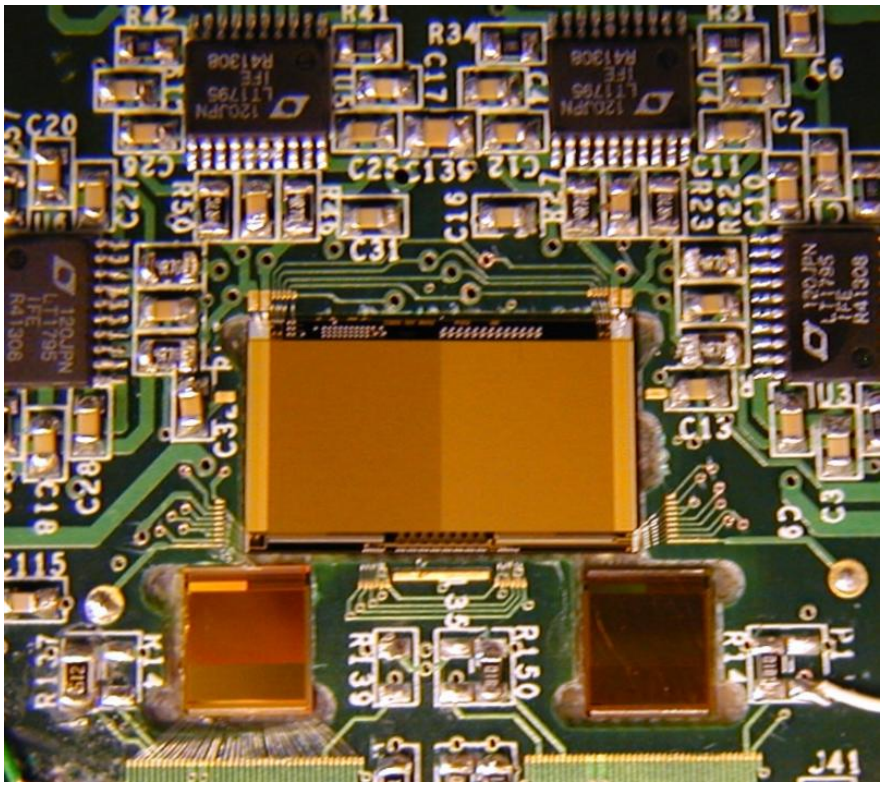
CPR1 Testing

Voltage injection into ADC

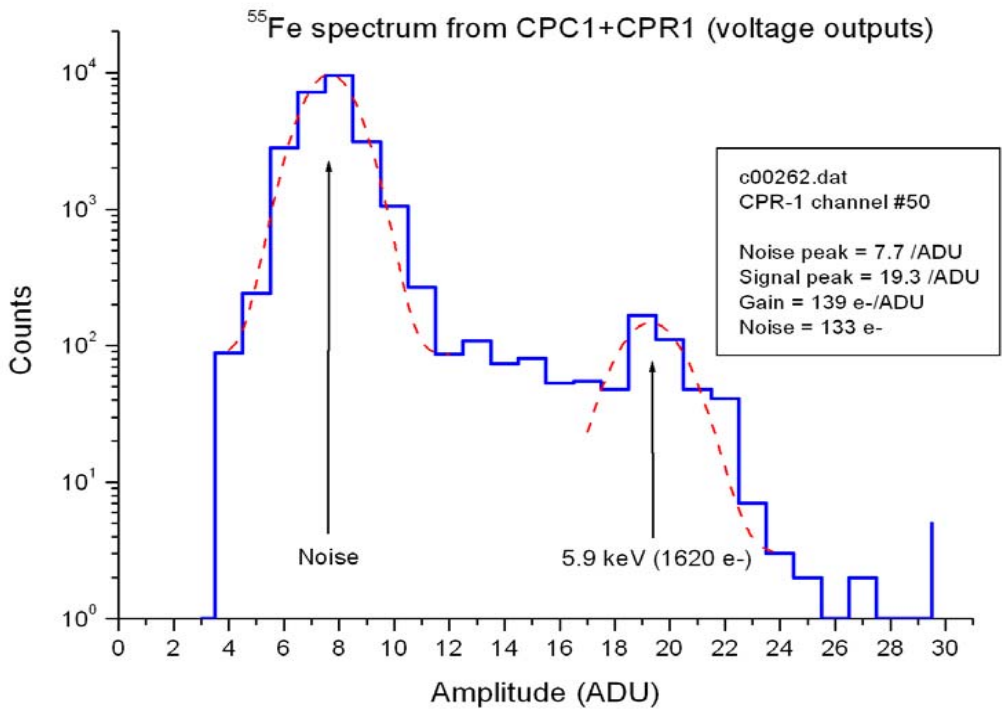


- **Flash ADCs tested**
- **Voltage and charge amplifiers tested**
- **Voltage gain ~40**
- **Very sensitive to timing and bias values**
- **Outstanding digital problems**
- **Charge amplifiers not fully understood**

Wirebonded Assembly



- **Total noise ~130 electrons**
- **Noise from preamps negligible**



Bump bonding underway at VTT

Future Detector Work

- **Test Programme**
  - **Bump bonded assemblies expected early May**
  - **Radiation effects on fast CCDs**
  - **High frequency clocking**
- **Next Generation CCDs and ASIC**
  - **Detector scale CCDs**
  - **Cluster finding logic**
  - **Design underway; production later in year**
- **In-situ Storage Devices**
  - **Resistant to RF interference**
  - **Reduced clocking requirements**

(See Chris Damerell's talk on Thursday)

Summary

- **Excellent progress over past two years**
  - **Mechanical options studied in detail**
  - **CCD+ASIC operation achieved**
  - **New ideas being discussed**
- **CP CCDs are viable technology for linear collider**
- **Next generation will be full-scale prototype CCDs**

➢ ***Accelerator technology choice will determine path***