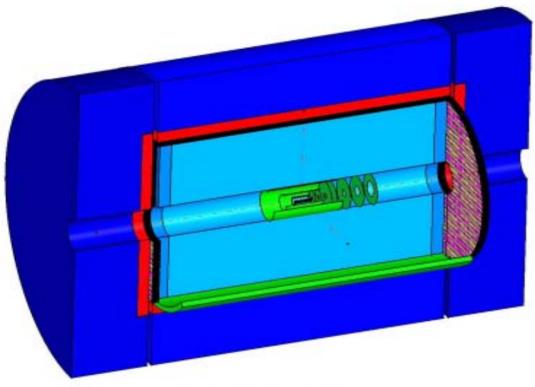
SiLC Progress Report

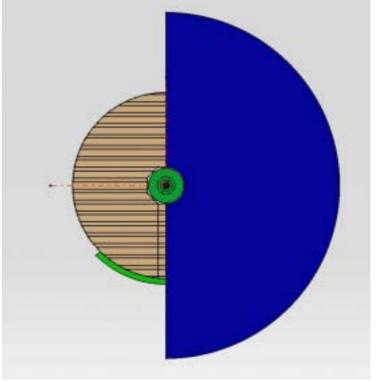


Capture of PIBD, CADIED, CatalaCVESLAVESLA CVTProduct - 15/04/0004 13:25:44

LCWS '04, Tracking session, Paris, April 19th to 23rd 2004,

Latest on:

- •R&D on sensors
- Results on Lab test bench
- R&D on F.E.E & readout
- R&D on Mechanics
- Integration & calibration
- Simulations



SiLC Collaboration

<u>USA:</u>

BNL Wayne St.U.

U. Of Michigan

SLAC UCSanta Cruz -SCIPP

Proposition DOE(04-06): UCSC+SLAC+LPNHE

<u>Europe:</u>

Helsinki U. (Fin)
Obninsk St. U.(Ru)
IEKP Karlsruhe(Ge)
Charles U. Prague (CZ)
Ac. Sciences.Wien(Au)
LPNHE-Paris(F)
U. de Genève (CH)
Torino U. (I)
INFN-Pisa (I)
La Sapienza-Rome (I)
CNM-Barcelona (Es)

<u>Asia:</u>

Korean Institutes

Tokyo U. HAMAMATSU

EU contract btw. several Inst.

Cantabria U. (Es)

PRC Proposal on May 7th 2003 (PRC-DESY-03-02) + Addendum on Oct. 31st 2003: Roadmap: mid 2003 to end 2006 → test beam on full prototype, by fall 2006

R&D applies to both: all-Si-tracking system or to Si-Envelop (Si-tracking+TPC)

SiLC gathers worldwide expertise on Si-tracking detectors technology Based on LEP, B-factories, Tevatron, LHC(ATLAS, CMS, ALICE), AMS et GLAST LEITMOTIVs: HIGH PERFORMANCES, TRANSPARENCE & EASY to BUILD

R&D on sensors

The Right St. Life Square St. Squ

Kapton with serpentine design → 28, 56,112 & 224 cm µstrip length

<u>Underway</u>: Fabrication of a 2nd proto Made of 10 new Hamamatsu sensors. Each sensor will be tested in Vienna CMS test bench, no serpentine.

ASN, SiLC Progress Report, LCWS04

Long ladder prototype (Geneva +ETHZ + Paris), read out with VA64hdr (AMS-IDEAS)

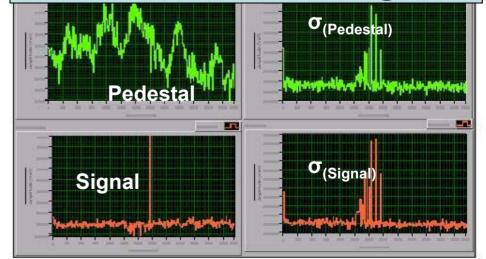
Lab test bench, Labview based (Paris)

Test with LD1060nm on 224 cm long patrip

Latest results after redesign of the kapton



Prelim: S/B ~10 looks achievable @ 224cm

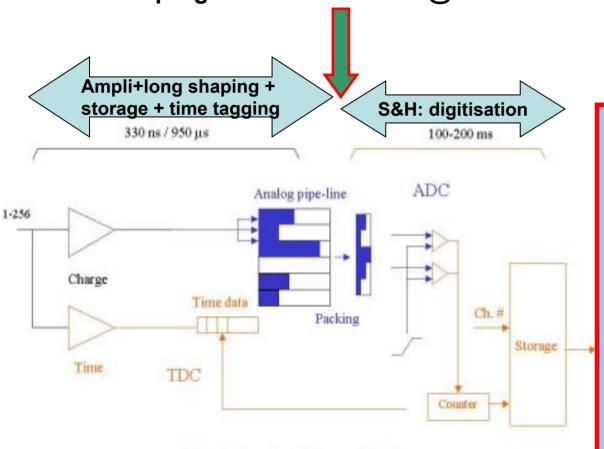


And work in progress on sensor R&D especially in Korea (Park's talk) & foreseen with others (ST-M or CNM, for instance)

R&D on F.E.E & readout for long ladders

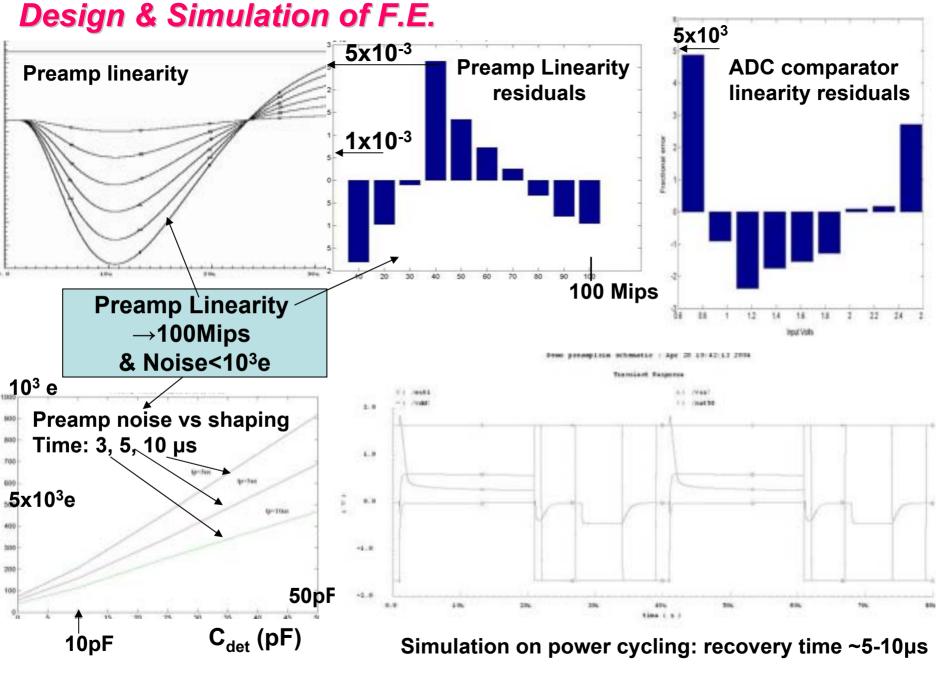
- Work in progress on new F.E.E @ SCIPP-UCSC (B Schumm's talk)
- New V.A. IDEAS chip adapted to LC Si-tracking (IDEAS + Vienna + Karlsruhe)

Work in progress on new F.E.E. @ LPNHE



Goals:

Low noise preamp
Long shaping time
Very low power dissipation
Shared ADC/TDC
Digitisation @ sparsification
Power cycling
Compact and transparent
Choice of DSµE



ASN, SiLC Progress Report, LCWS04

Summary of SiLC FE & Readout status (04/21/04) (@ LPNHE

Item Features Status

Very Front end:

Preamp Gain: 3,5 mV/MIP Simulated

Noise: 480 e- (690e-)

@50pF, 10 (5)µs shaping time

Dynamic range: 100 MIPs

Power: 82.5 μW

Shaper Peaking time: Gain 4

3-5 µs

Sample and Hold:

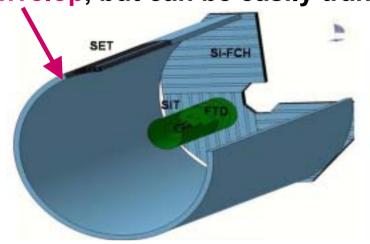
ADC 10 bit 4µs Comparator simulated

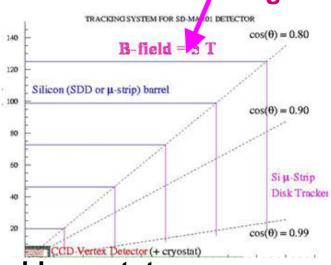
Power: 40 µW

Multi-channel prototype in UMC, 0.18 μm sent to foundry by July 04
Expected to be fully tested at Lab test bench by end 04
Estimated total power dissipation per channel all included ≤ 200μW
Thus for 2x10⁶ channels → 400 Watts without power cycling

R&D on Mechanics

CAD design of the architecture of the various elements of the Si-Envelop, but can be easily translated to the all-Si tracking case

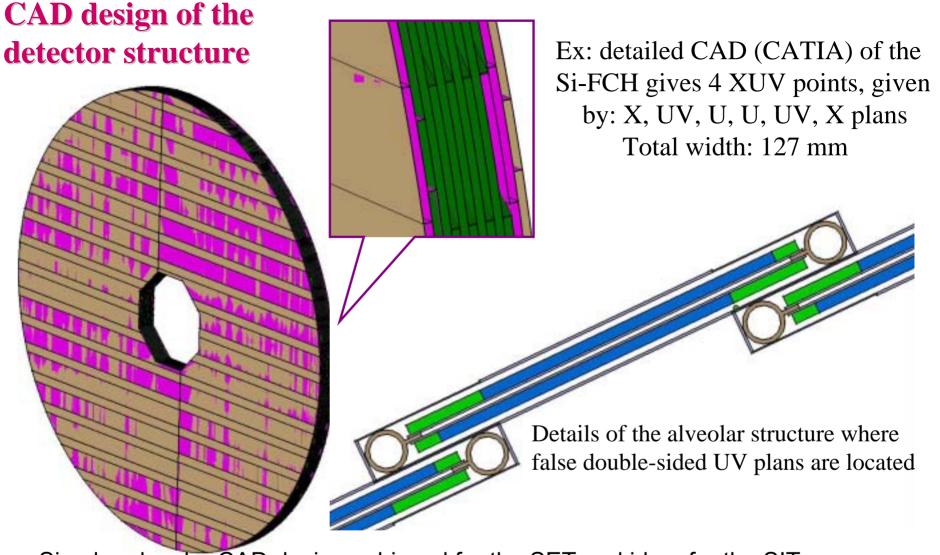




- Design and construction of a long ladder prototype
- Thermal mechanical studies
- Alignment techniques are under development at U. of Michigan and starting at U. of Cantabria (based on interferometer & LHC expertise)

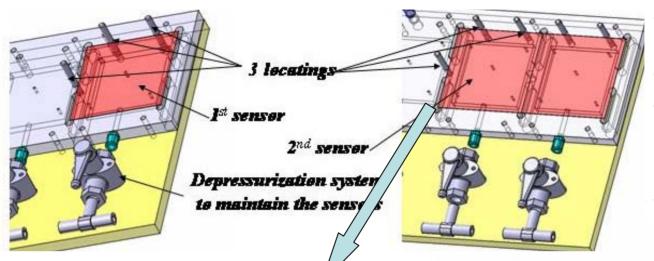
Main R&D aims:

Transparency, high precision, simplicity, and easy to build



Simular alveolar CAD design achieved for the SET and idem for the SIT Next step: collaboration with Industry to check feasibility vs cost of designed structure and fabrication of a mechanical prototype for further mechanical studies

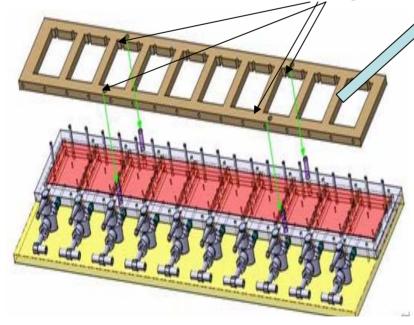
Long ladder construction:

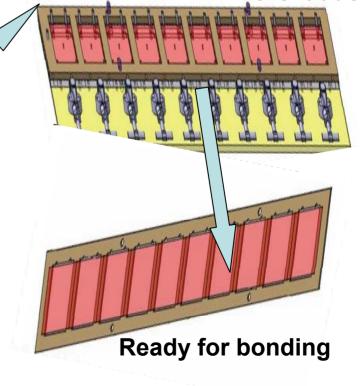


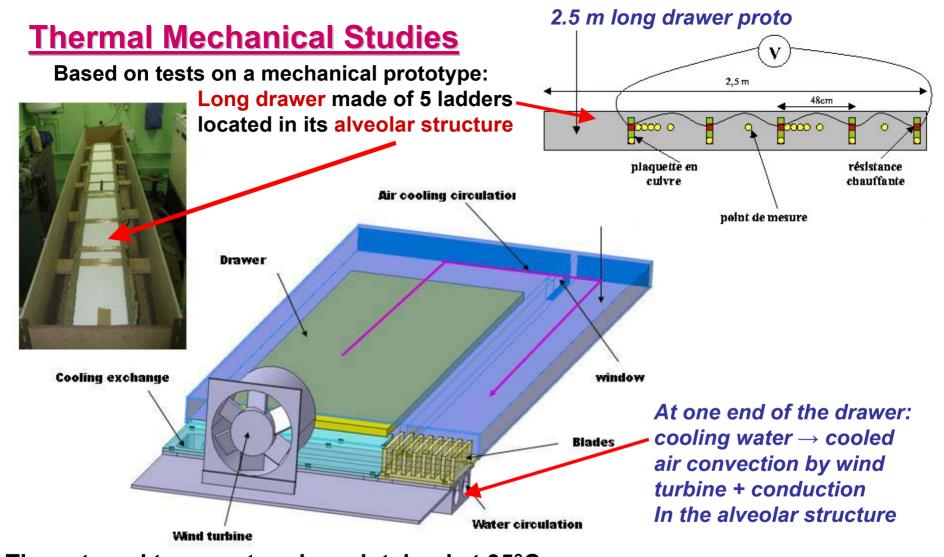
Sensors are positioned one by one on assembly frame

Gluing of the ladder

The long ladder structure is positioned on the 10 sensors with 4 locatings







The external temperature is maintained at 35°C The simulated power dissipation per channel: 400 μ W (i.e. 2 x expected one) The goal is to maintain the temperature on the detector below 30°C, in order to avoid intrinsic noise increase.

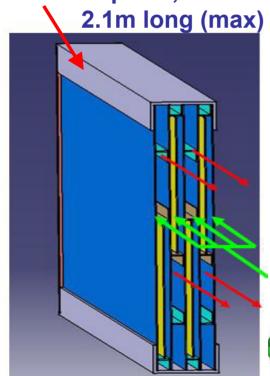
Results:

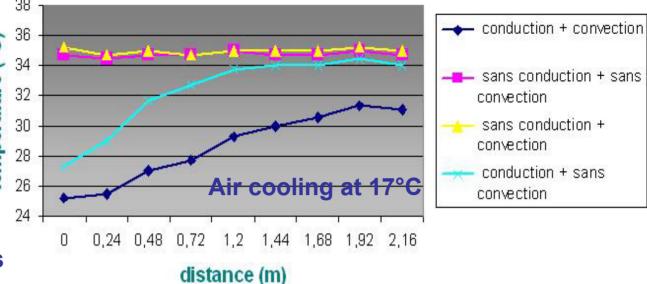
Conduction +convection
by air cooling @ 6.5°C
at one end of drawer

→ T < 28°C over 2.2m

Very important reduction
of material budget !!!

Underway: thermal studies on Si-FCH proto, drawer

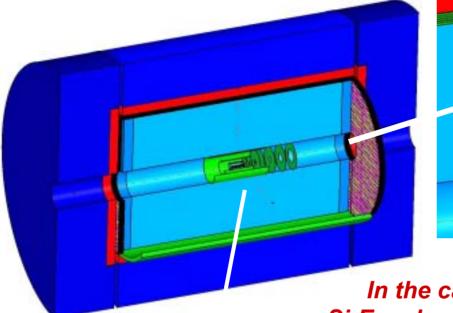


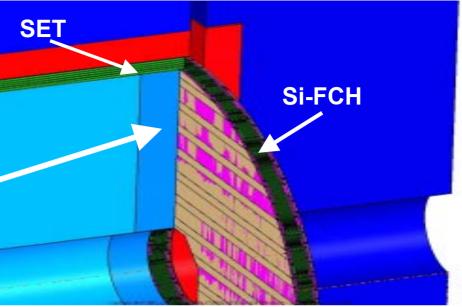




These results on prototypes are used to model the computed results from SAMCEF simulation package.

Integration studies: on Mechanical side





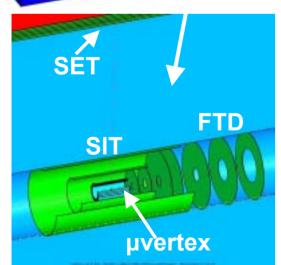
In the case of a Large Detector (i.e. with TPC)
Si-Envelop components are in strategic positions:

- SIT links μ vertex (σ ~2-3 μ m) with TPC (σ ~100 μ m)
- SET links TPC with calorimetry
- Similarly in the FW region: FTD and Si-FCH.

Questions to be answered:

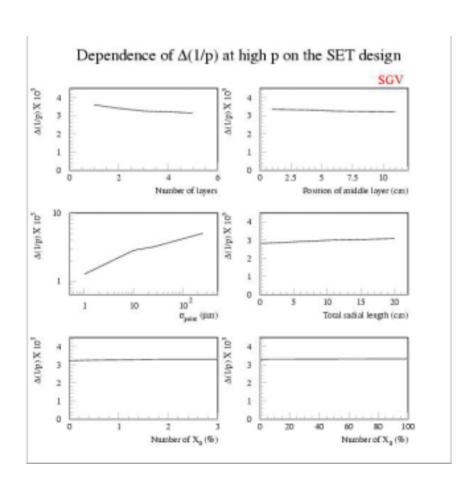
In the case of SET & Si-FCH especially:

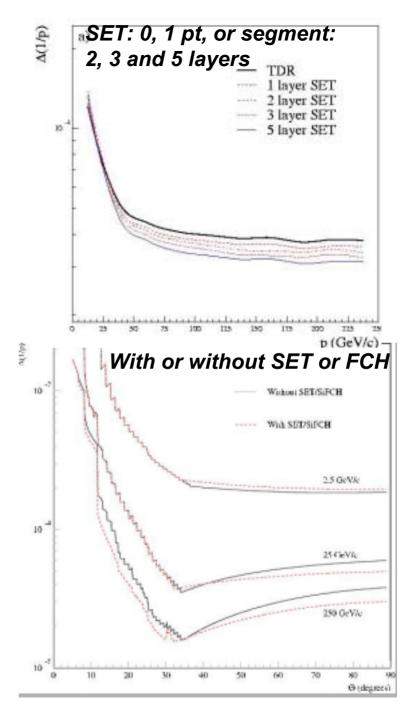
- ➤ One point? What precision?
- One segment?
- ➤ One track? (requested length of tracking level arm?)
- ➤ How this design compares with SD in central & FW?



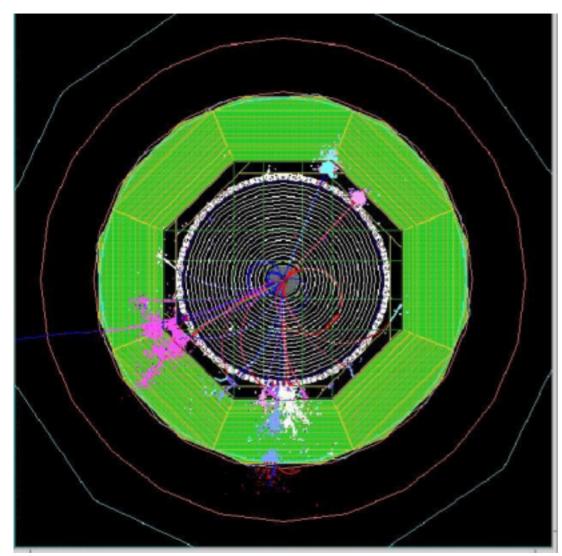
Simulations

To answer previous questions and study detector performances use of SGV fast simu (LPNHE), with first answers.
And work in progress with full simu BRAHMS & MOKKA + G4





Full simulation GEANT 3 and 4 based



Fully G4 simulated $H\rightarrow bb\ Z\rightarrow e+e-$ event including SET (detector in white) (Obninsk)

Conclusions

Important progress achieved on

- Sensor R&D (long ladder tests)
- •R&D on electronics: 2 FEE are developed & ready for foundry by July 04
- ■R&D on Mechanics:
 - CAD of the overall support architecture
 - Construction of long ladder
 - Thermal studies (very encouraging result)
- Alignment studies
- Simulations: setting up BRAHMS and GEANT 4

SiLC is taking speed.

By fall 06: a full prototype on test beam possibly with calorimeter and/or TPC prototypes.