Vertexing and Tracking at the LC

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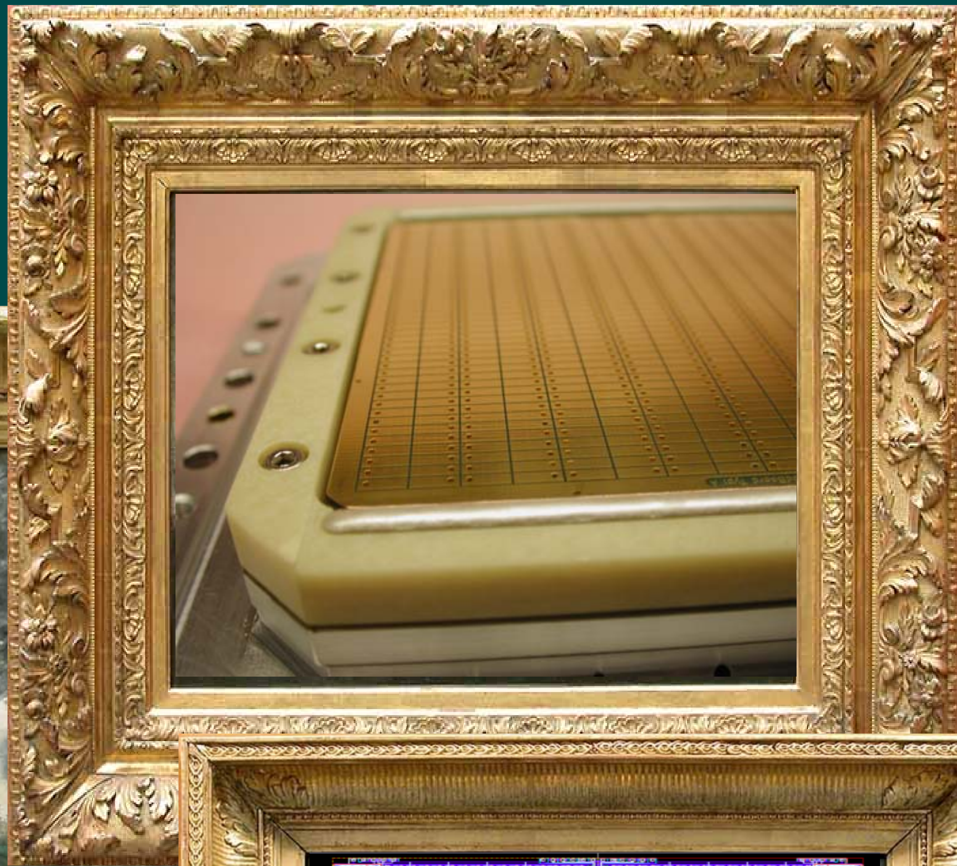
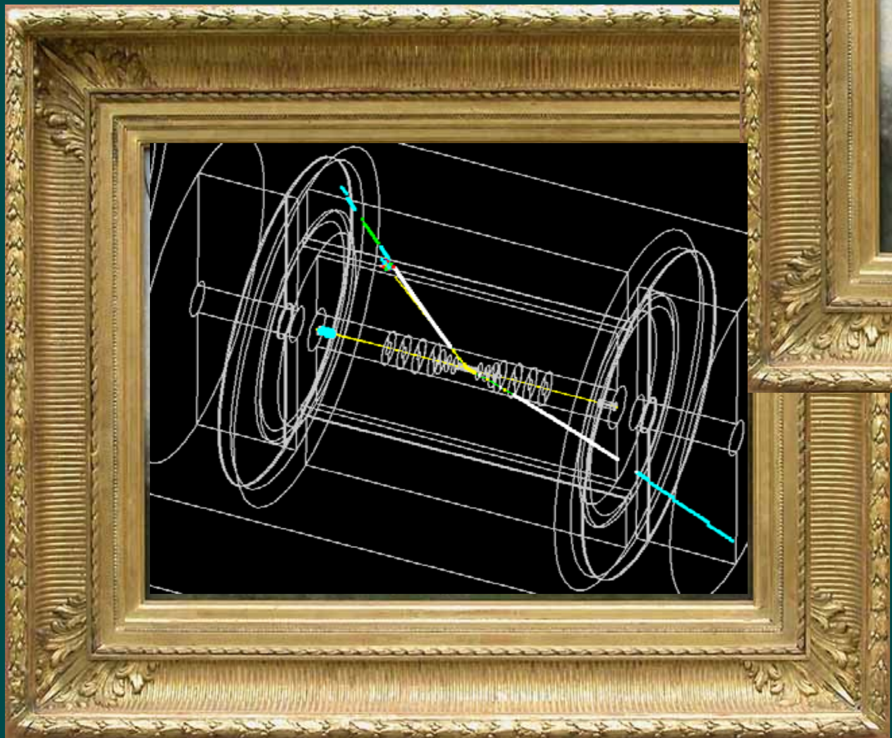
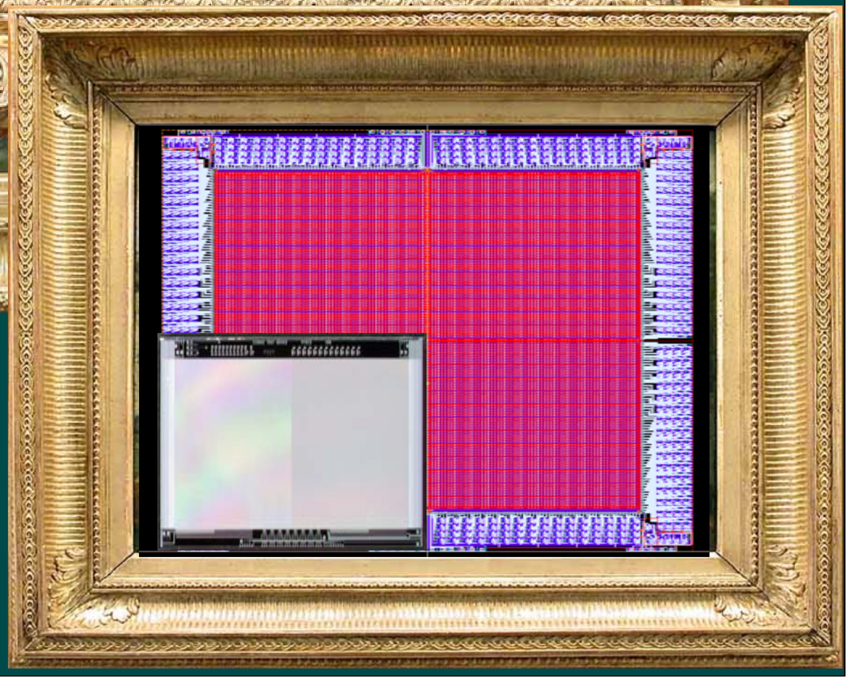
UC Berkeley & LBNL

Paris, April 23, 2004



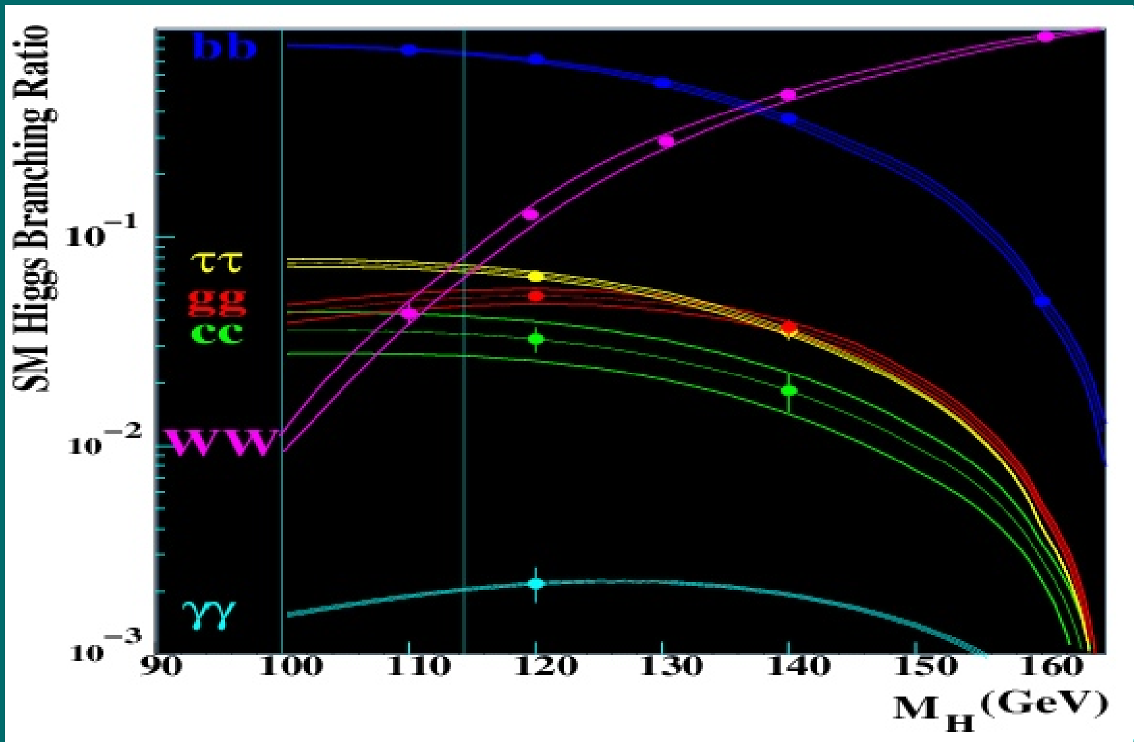


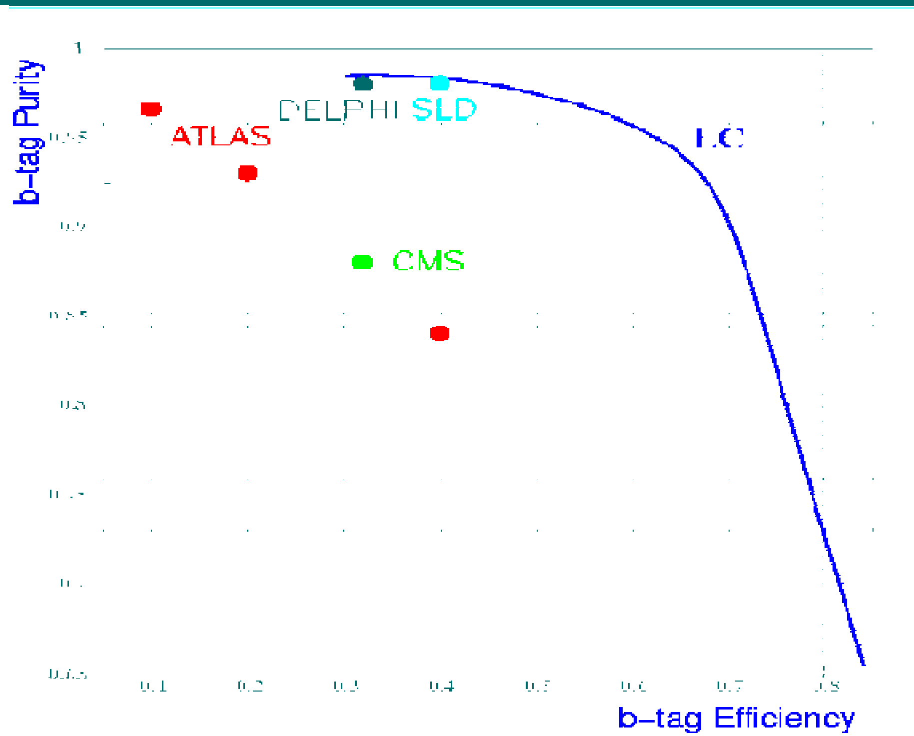


Physics Benchmarks for Tracking: from the Higgs to Cosmology

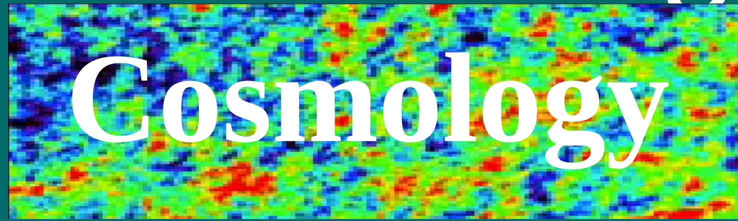
Tracking detectors must provide jet flavour identification capabilities and accurate momentum reconstruction that make the LC unique and enable its physics program: this drives their specs to new levels;

Understanding Origin of Mass and EWSB through Higgs sector requires unprecedented Jet Flavour Tag capabilities through track position resolution

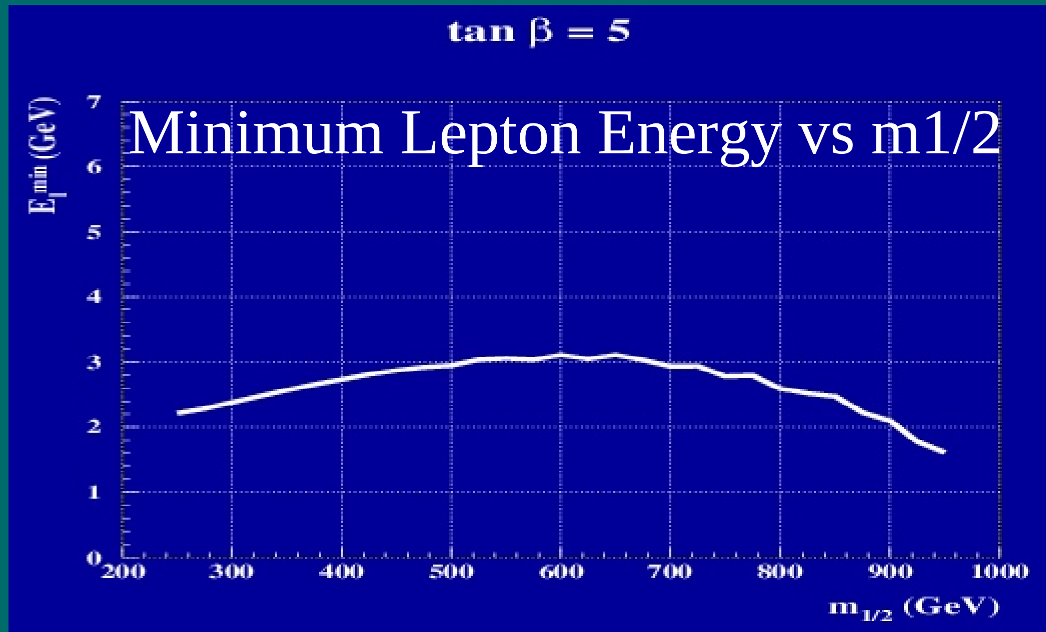


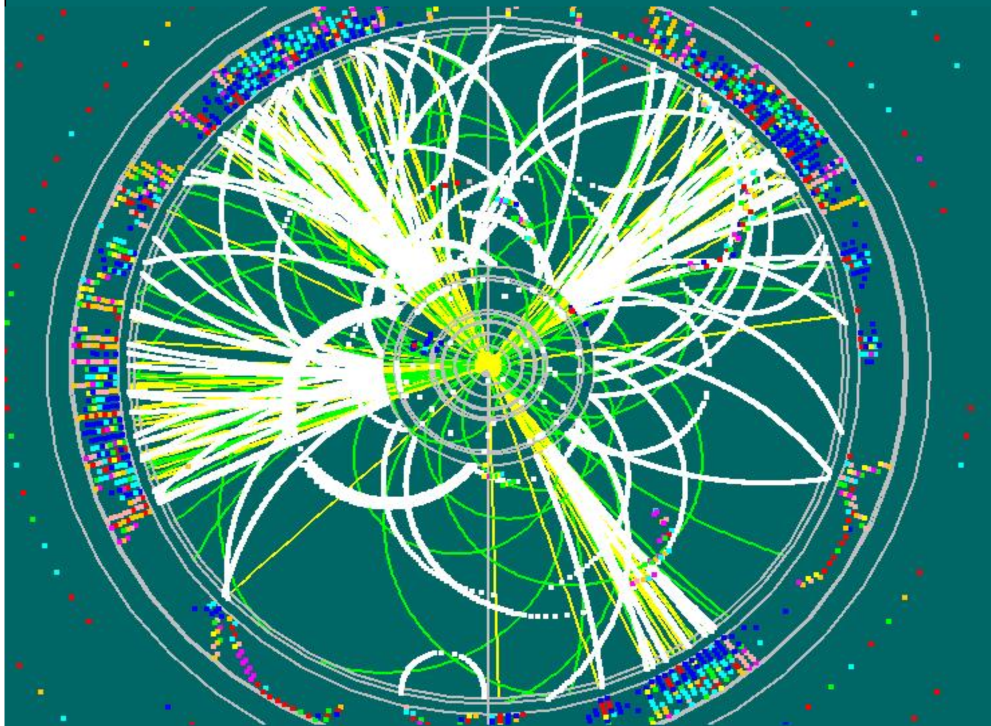


Physics Benchmarks for Tracking: from the Higgs to Cosmology



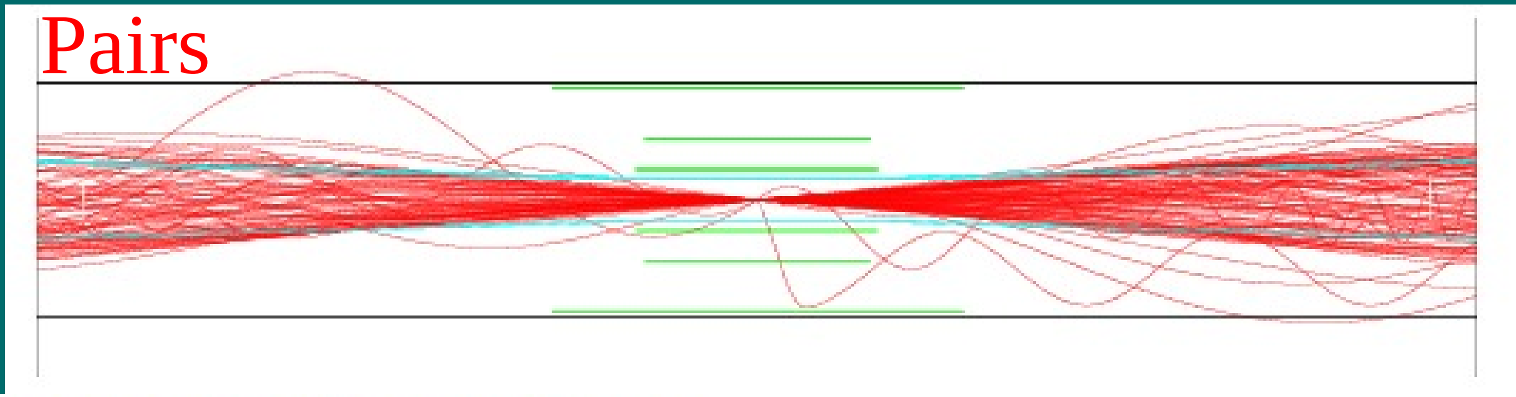
Cosmology motivates study of SUSY scenarios with precise mass relations of sparticle to LSP: typically small mass splittings corresponding to soft pions and leptons
or heavy Higgs decays with large b and track multiplicities





These offer complementary challenges for tracking which must be addressed within the same detector concept.

Machine Induced Backgrounds

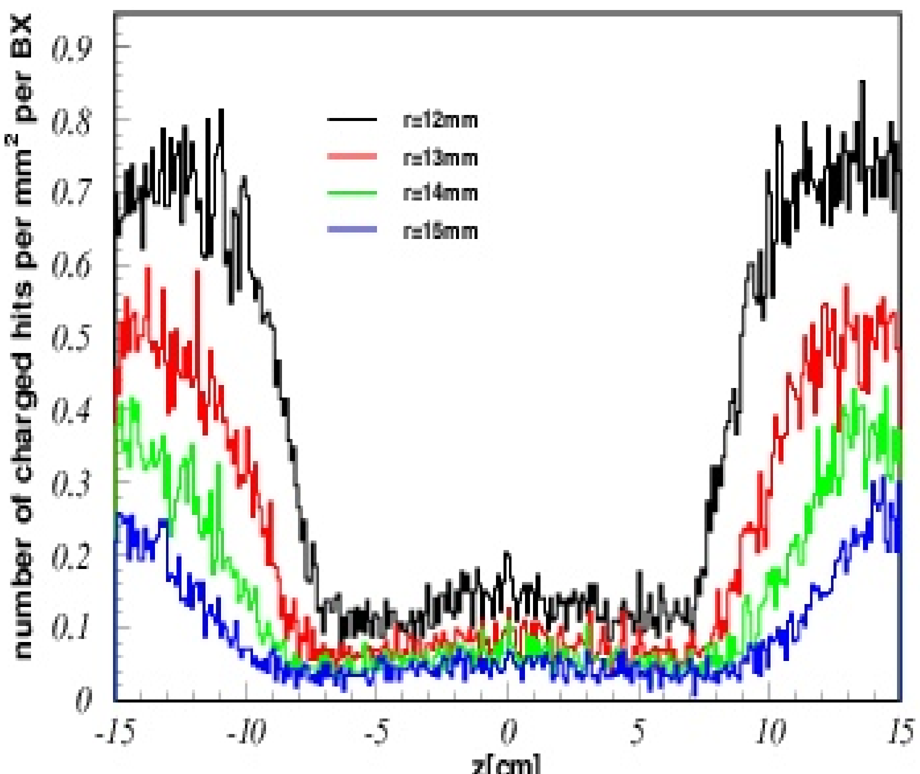


Hits density mm^{-2} from Pairs

LC	$\sqrt{s}$ GeV	R cm	BX^{-1}	25 ns^{-1}	train^{-1}
NLC	500	1.2	0.100	1.80	9.5
TESLA	800	1.5	0.050	0.05	225.0
CLIC	3000	3.0	0.005	0.18	0.8

Local track density

LC	0.5 TeV	0.2-1.0 hits mm^{-2}
CLIC	3.0 TeV	0.5-2.5 hits mm^{-2}
ATLAS	14.0 TeV	$\simeq$ 0.03 hits mm^{-2}/25 ns
ALICE	5.5 TeV/N	$\simeq$ 0.90 hits mm^{-2}/25 ns

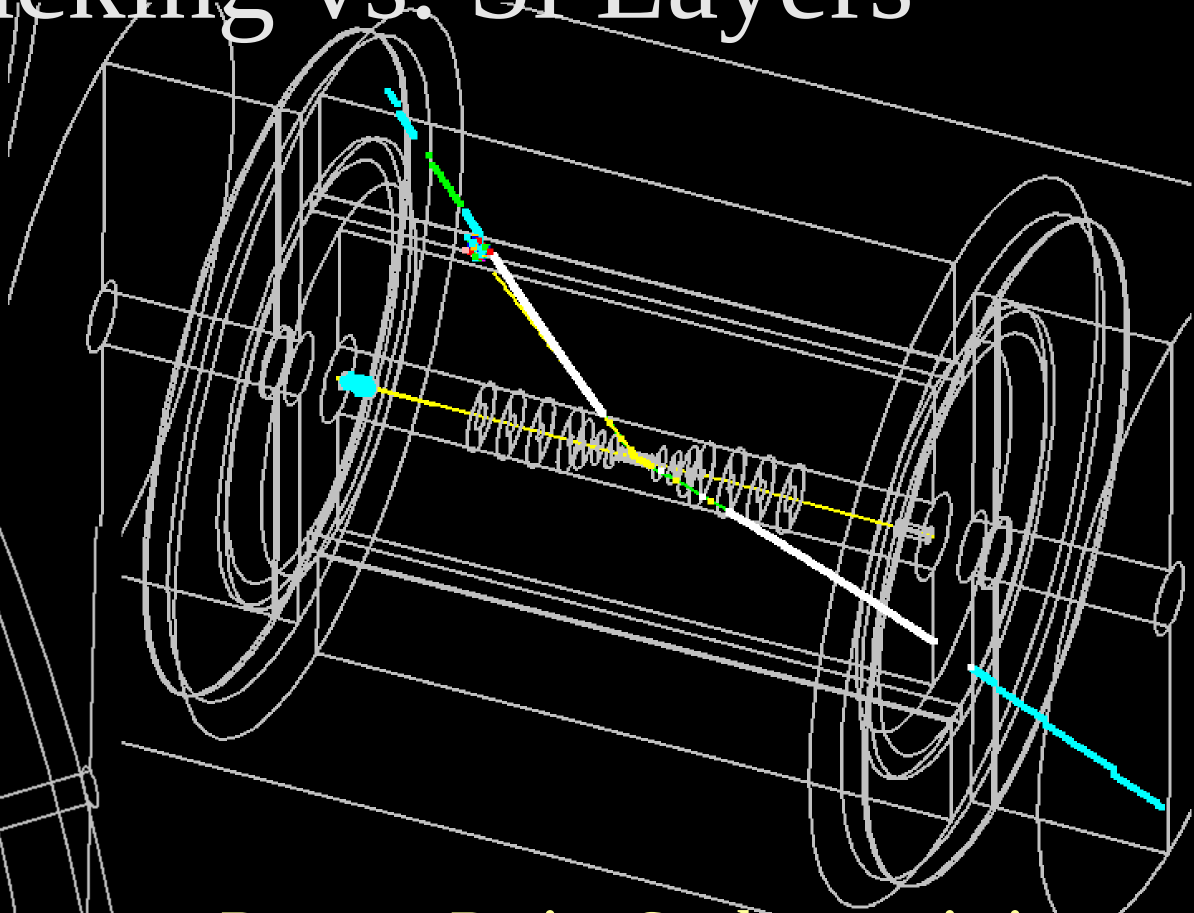


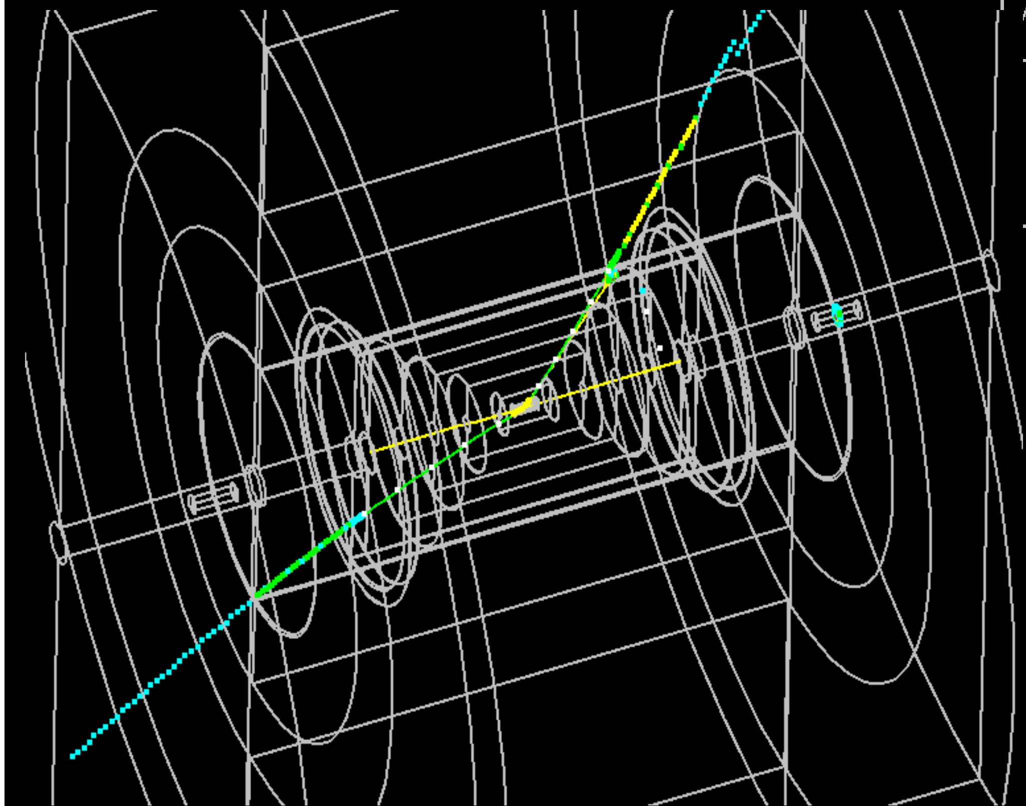
At X band may integrate full 192 BX train and then read in the beam-off time at SC need to multiple readout at 25-50 μs speed.

LD and SiD Detector Design: TPC 3D Tracking vs. Si Layers

Main Tracker technology drives LC detector design:

- **Large Detector** based on 3D **TPC** Main Tracker
- **Small Detector** based on **all-Si** Main Tracker



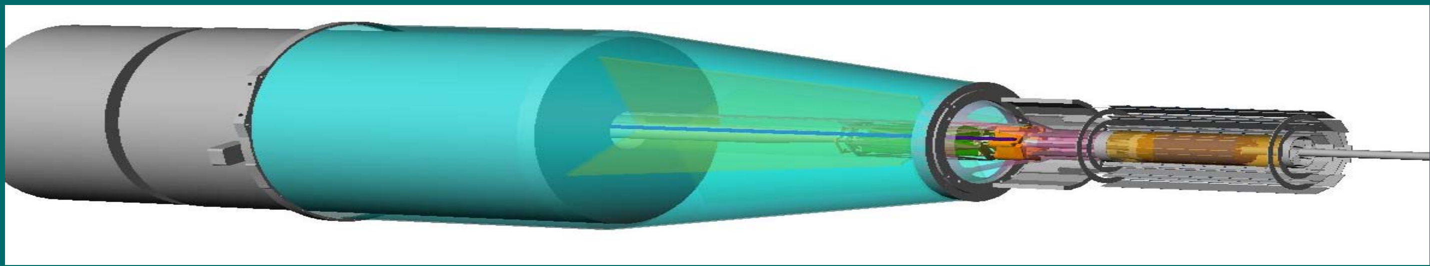


Detector Design Study to optimise, and **physics benchmark** fully integrated **Detector concepts**

Design activity to bridge from **physics** studies to **R&D** assessment

Vertex Tracker R&D

LC environment admits Si sensors which are substantially thinner and more precise than LHC and thus motivates new directions for R&D on Si sensors.



Two track separation and occupancy sets pixel size to ~ 20x20 μm
-> ~ 1 G channels -> needs data sparsification and zero suppression
Impact parameter accuracy better than 5 + 10/pt μm needed setting layer material budget to <0.1% X_o this prompts development of monolithic pixels
Power dissipation management may exploit low LC duty cycle

Choice of RF technology will soon clarify issues for R&D which has to address more significant challenges for Cold RF solution

Very significant developments since last LCWS: two architectures have been further developed and two new concepts realised in test structures, tested with mips and characterised.

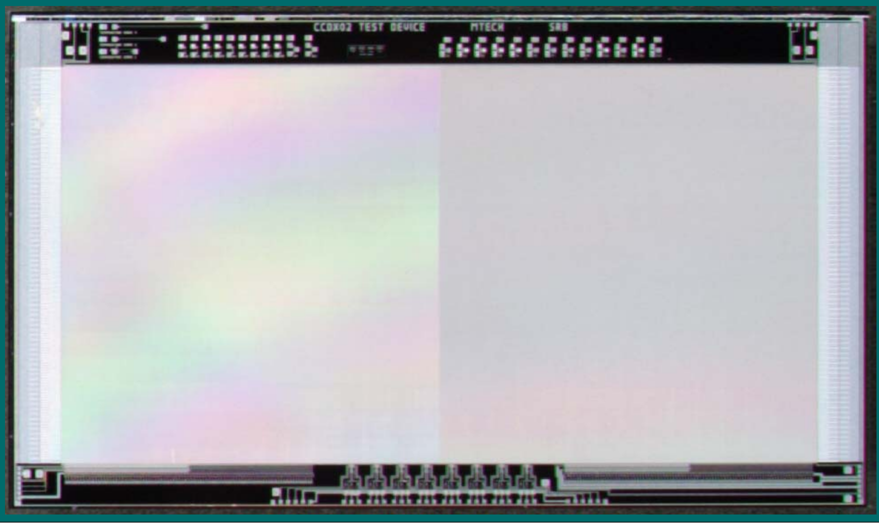
Si Sensor Technology Matrix

CCDs

LCFI, Oregon, KEK et al

Prototype architecture after SLD VXD3 experience, but needs faster readout and rad hard design.

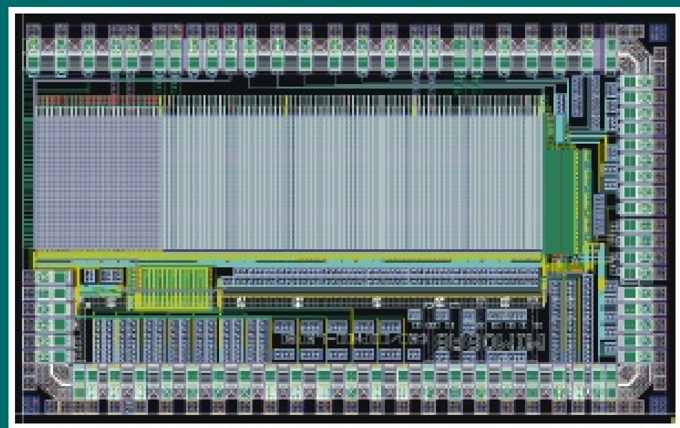
First Column-parallel CCD with low noise, very low driving Voltage and 50 MHz ASIC being tested. Bulk damage induced CTI by n and e- being actively studied with possible countermeasures (sacrificial charge, faster r/o cycle) being considered.



CMOS Monolithic Pixels

Strasbourg, RAL

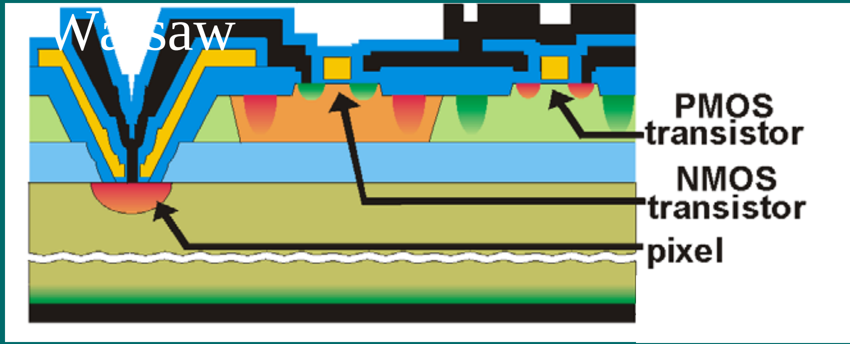
Concept from visible light imagers with eight generations of designs developed and tested, now addressing fast readout and on-chip integration of functionalities 20x20 μm cell CMOS sensor stands n fluxes 100 times larger than expected at LC, gives 2 μm resolution in beam tests is thinned down to 120 μm. Adopted for STAR VTX upgrade at RHIC: will bring experience of full-scale vertex detector application of sensors nearly matching X-band LC requirements.



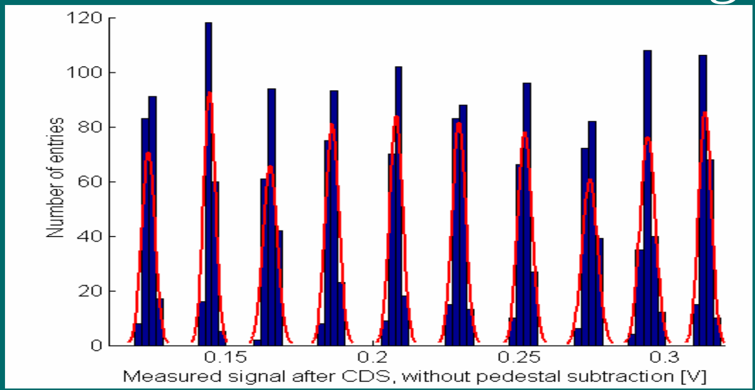
Si Sensor Technology Matrix

SoI Monolithic Pixels

Como, Krakow, Warsaw



Integrate pixel cell and electronics in SOI substrate, potential application span from HEP to medical imaging

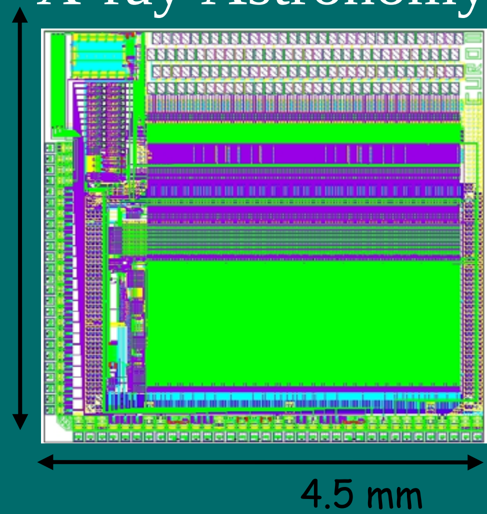


Early results of first test structure with 90-Sr and laser spot give first proof of principle, now develop 150x150 μm pixel prototype

DEPFET Monolithic Pixels

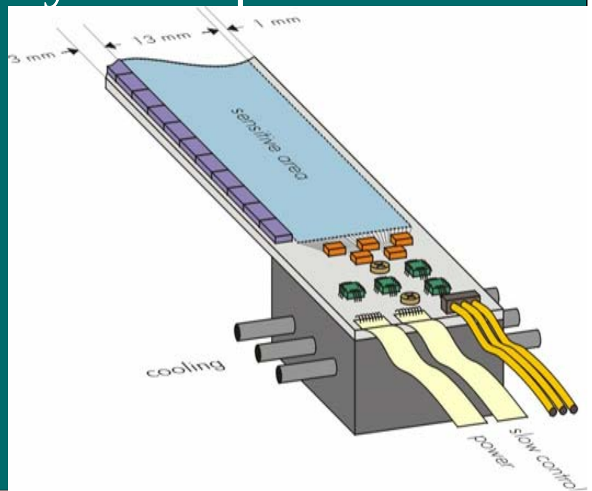
Munich, Bonn

Low-capacitance, low-noise structure with intrinsic low-power consumption and fast signal; applications in HEP and X-ray Astronomy



Readout needs external chip: ASIC with zero suppression and CDS, 50 MHz digital part: readout of full DEPFET array to be performed

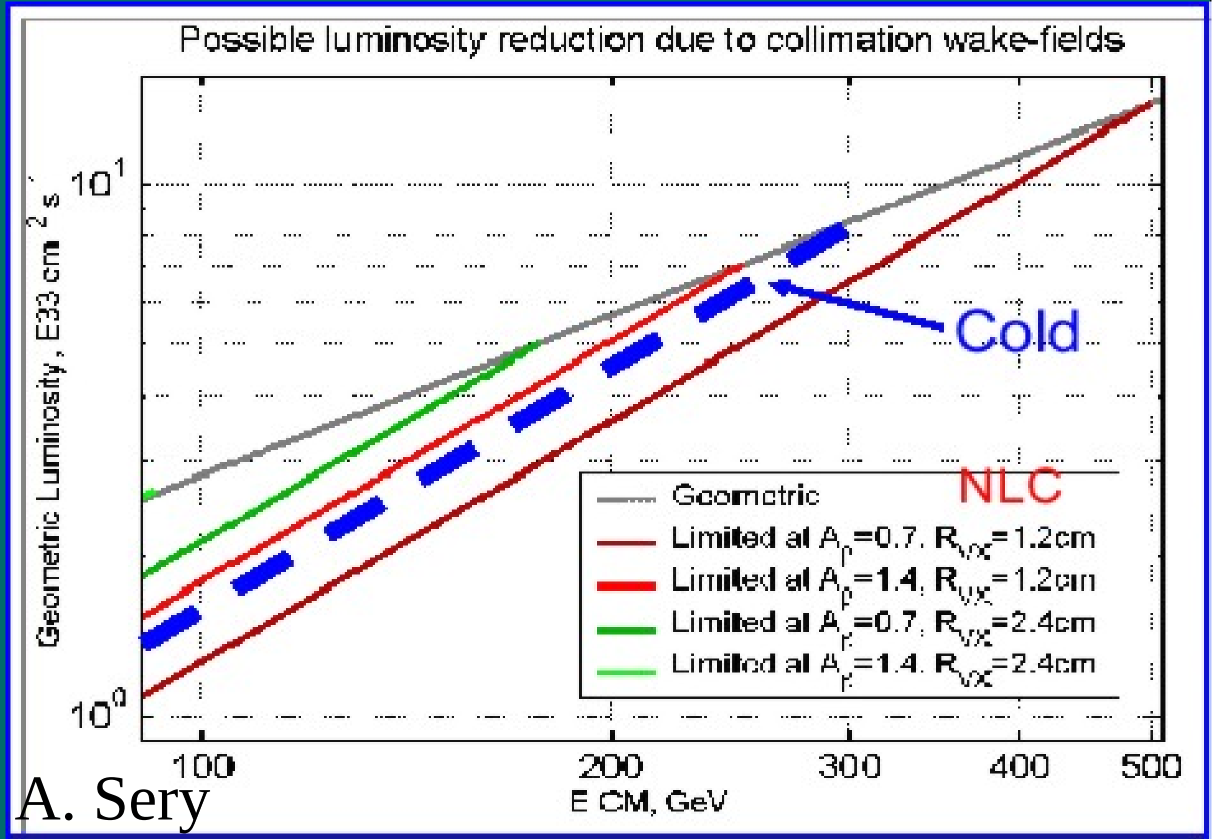
Low noise allows 50 μm thinned down sensors



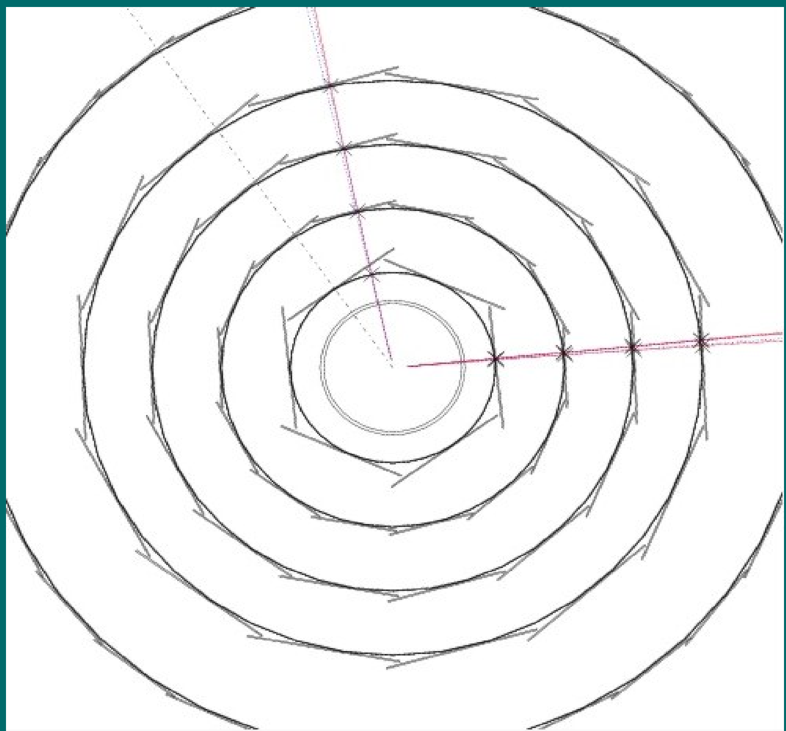
Vertex Tracker Inner Radius

Wake-field collimation sets pressure on beam-pipe radius:

Study of H -> cc/H -> bb using ZVTOP does not clearly indicate an advantage for Rvtx = 1.5 cm;



A. Sery



Need to systematically consider τ tagging in Higgs and SUSY decays and B-charge determination, more sensitive to details of impact parameter performances.

TPC R&D

Large area continuous tracker capability of TPC with timing and dE/dx informations and robust performances make it attractive for precision at LC

Develop Micropattern Gaseous Detectors (MPGD) applied to TPCs

Optimisation of design, geometry and gas choice

Development of TPC Readout schemes

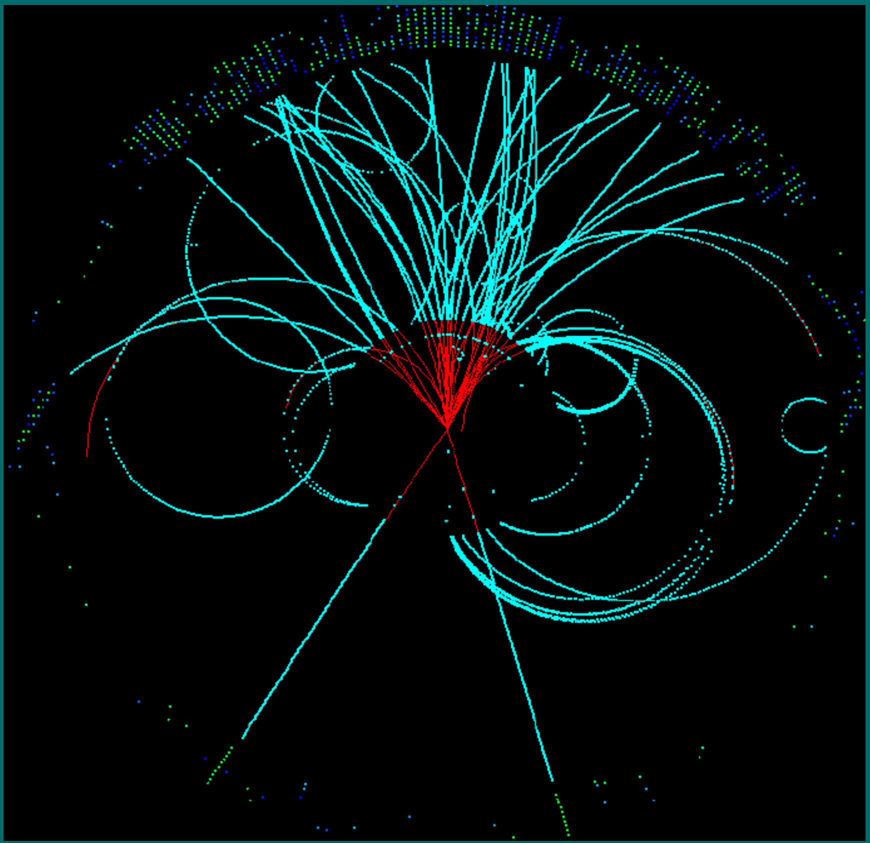
Need to achieve

- $\delta(1/p) = 10^{-4}$ GeV/c^{-1}

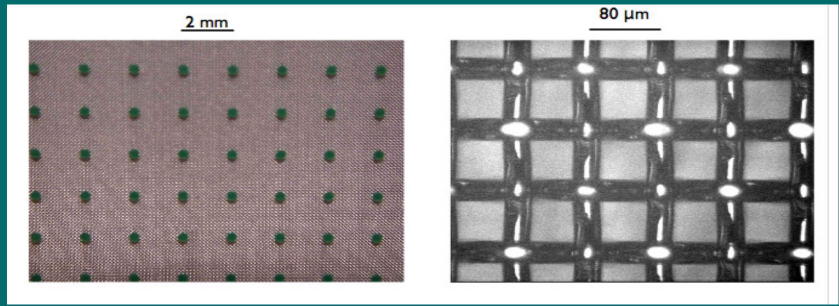
in TPC only;

200 pad rows, 120 μm resolution
OR 1200 pads, digital readout;

Need to demonstrate improvement in point resolution and control alignment to ~10 μm in R-Phi plane.



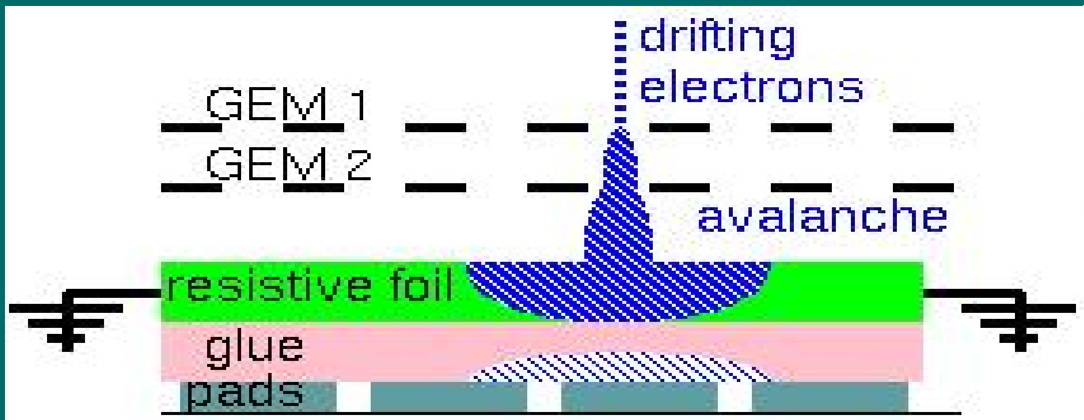
Micropattern Detectors for TPC



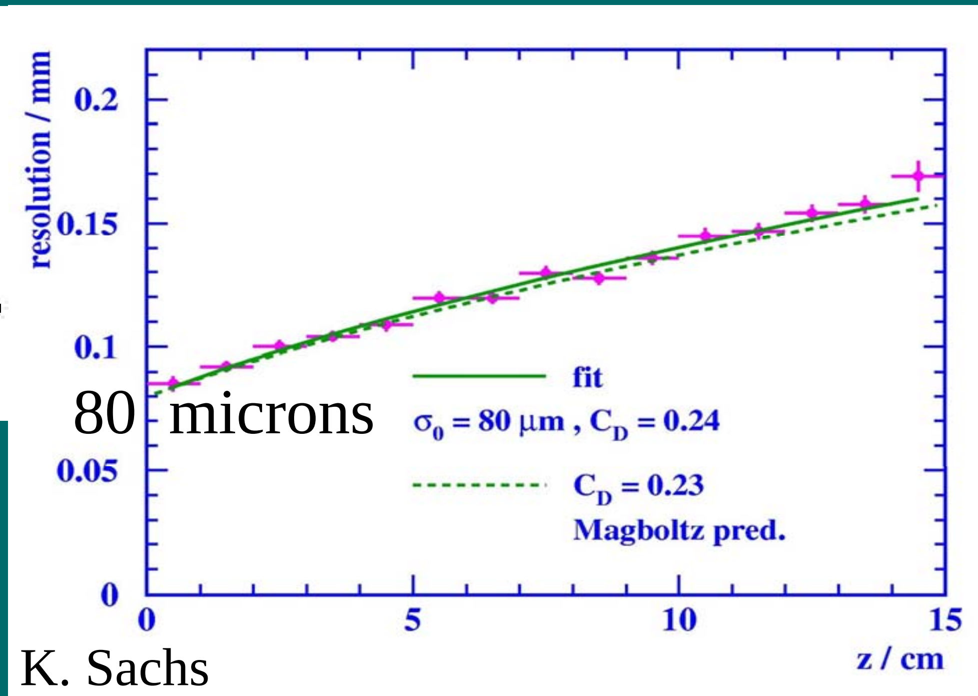
GEM,
Micromegas

MPGD offer significant advantages for TPC readout due to reduced ExB, larger gains, ion suppression and faster, narrower signals providing better space resolutions -> diffusion and defocusing of charge to center of gravity

Achieving the optimal resolution requires improved sampling techniques

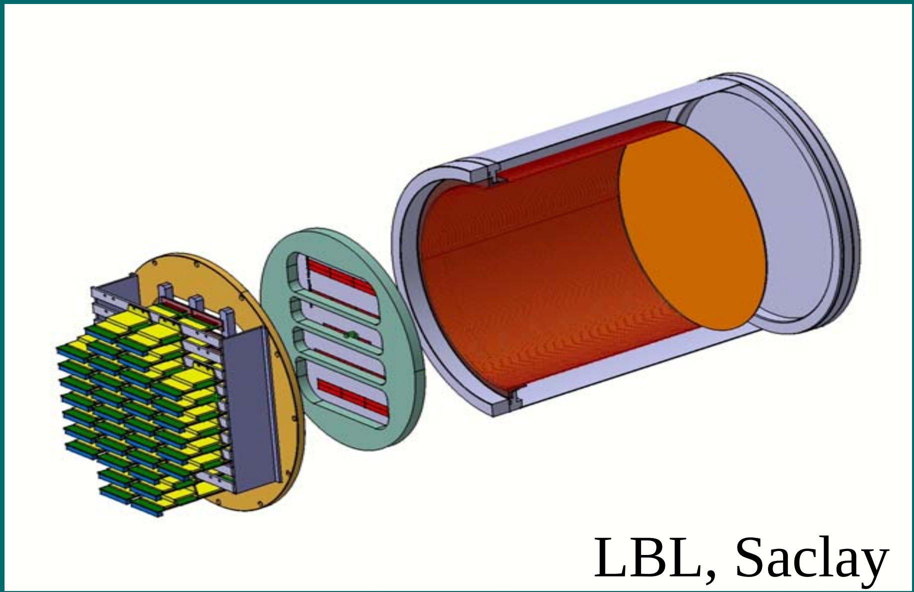


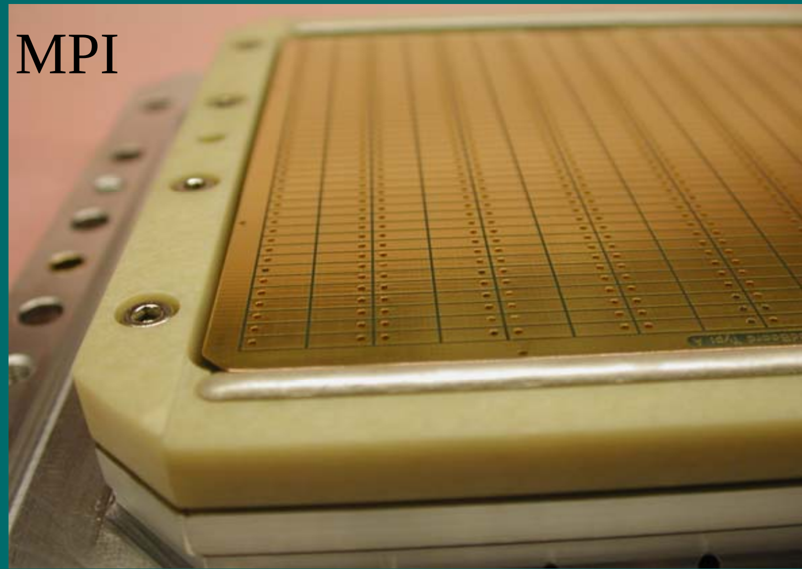
Charge dispersion on resistive anode to improve resolution close to dispersion limit succesfully tested with GEMs



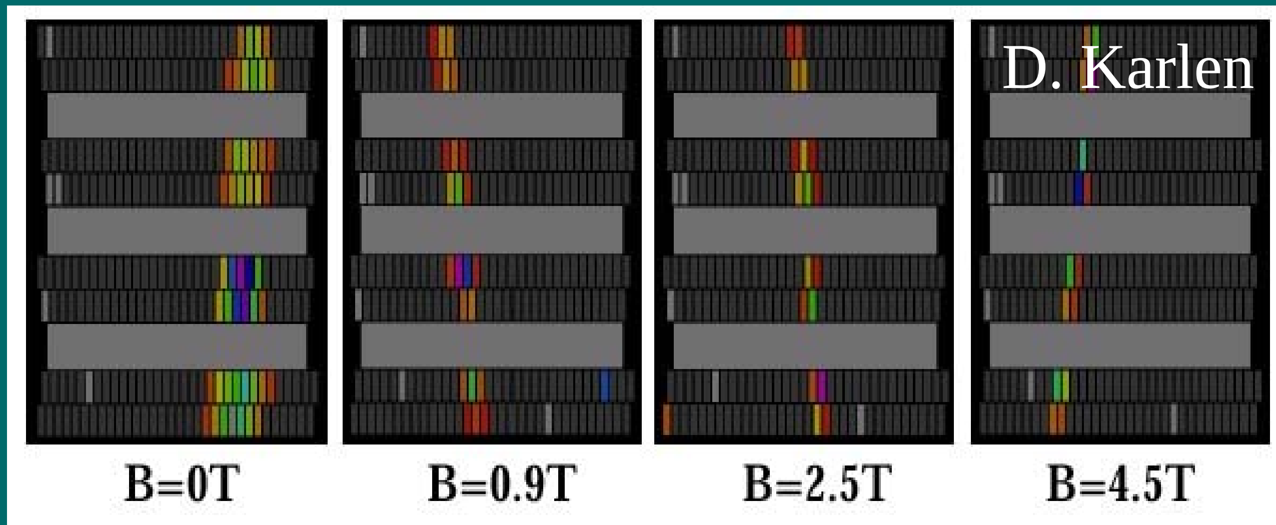
TPC Prototype Tests

Significant effort worldwide (DESY, KEK, LBL, MPI, NIKHEF, Orsay, Saclay, Victoria et al.) in developing test facilities (MPGD + field cage + B field)





Sampling charge techniques need to be tested and optimised in high B fields



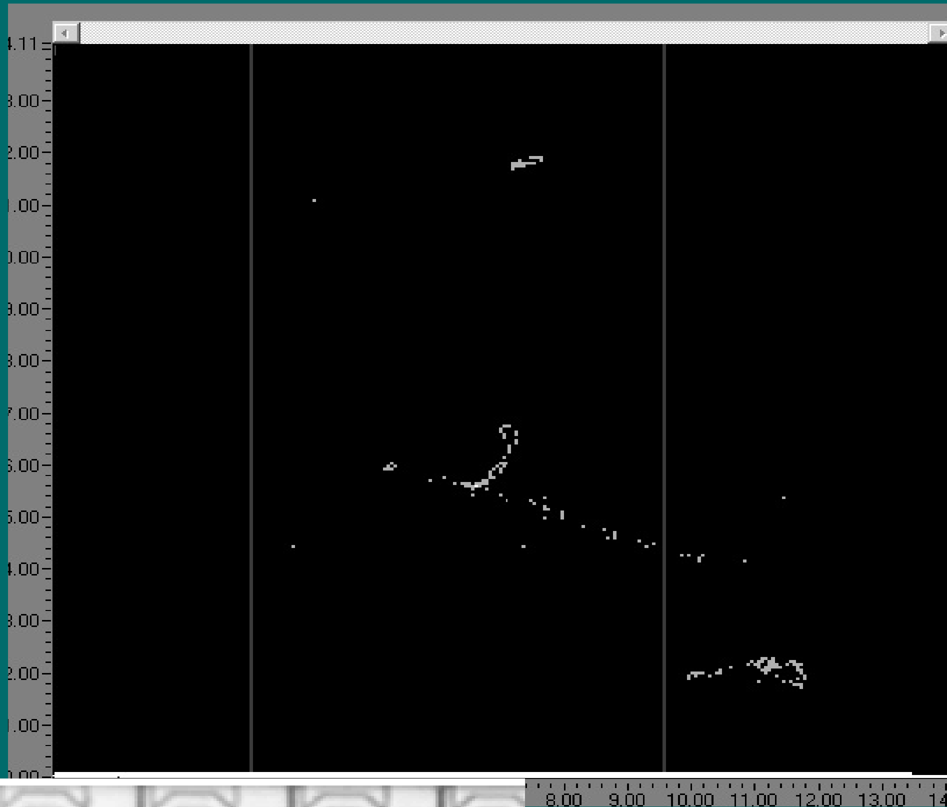
TPC Readout with VLSI Chip

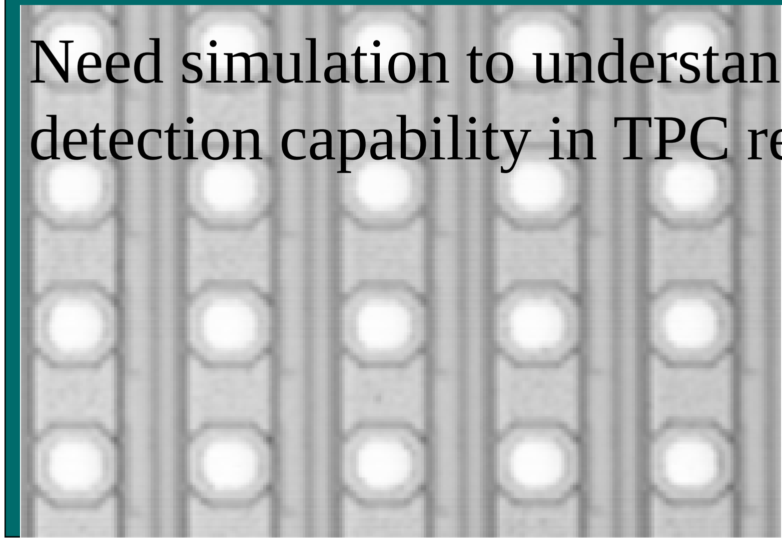
VLSI readout technology inherited from Si dets successfully tested at NIKHEF using MediPix2 chip with Micromega foil;

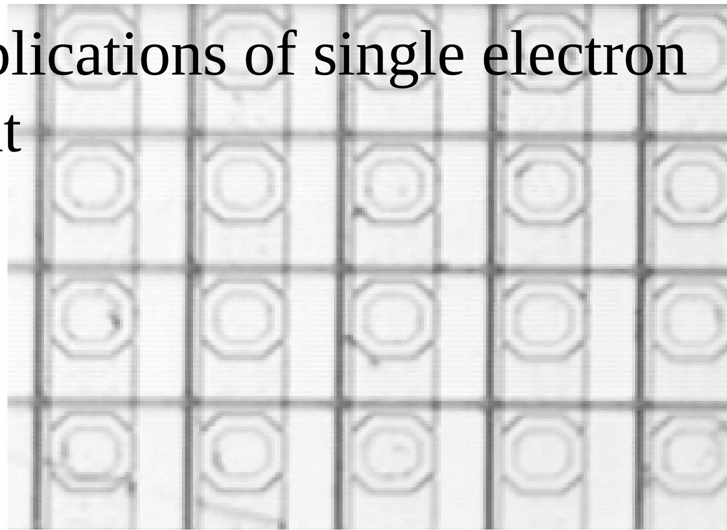
Charge collection with granularity matching primary ionisation cluster spread;

Now consider testing other chips and develop custom chip including time stamping capabilities.

J. Timmermans





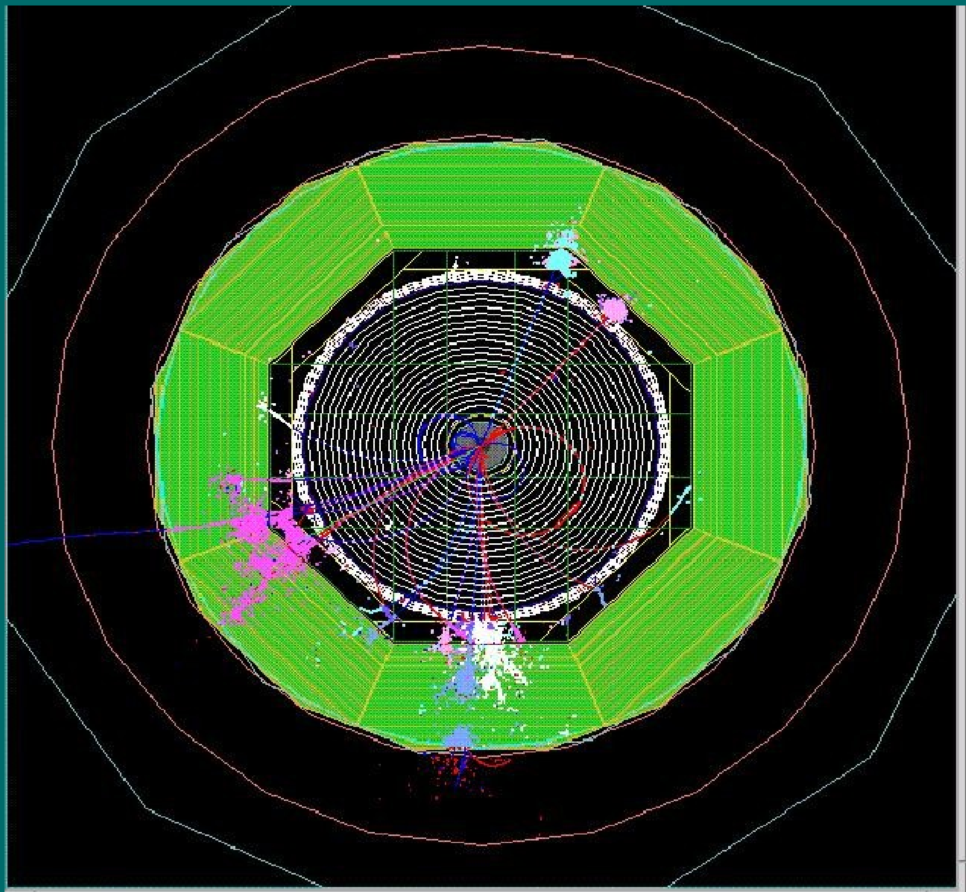


Need simulation to understand implications of single electron detection capability in TPC readout

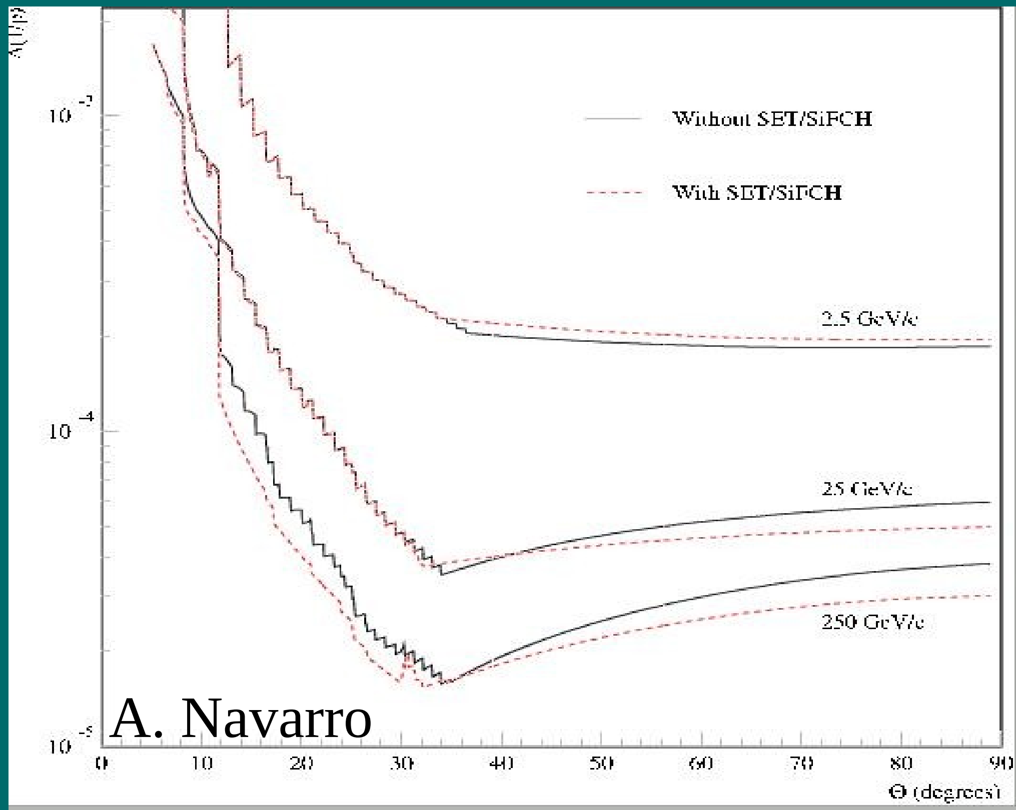
SiD Concept

Multi-layered Si strip detector structure for main tracker in high B field may offer competitive p resolution at reduced material budget, more robust operation and afford smaller radius ECAL;

Dedicated conceptual design and module R&D is starting as world-wide Collaboration (SiLC) inheriting from LHC Trackers experience.



SiD 1/p resolution vs. polar angle

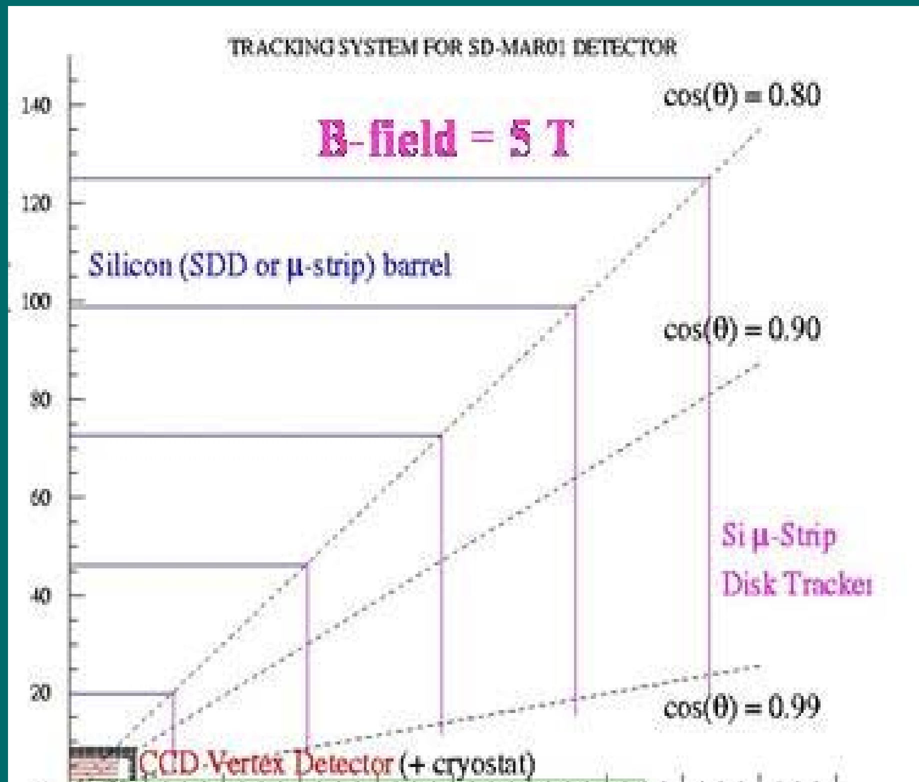


Si Modules R&D

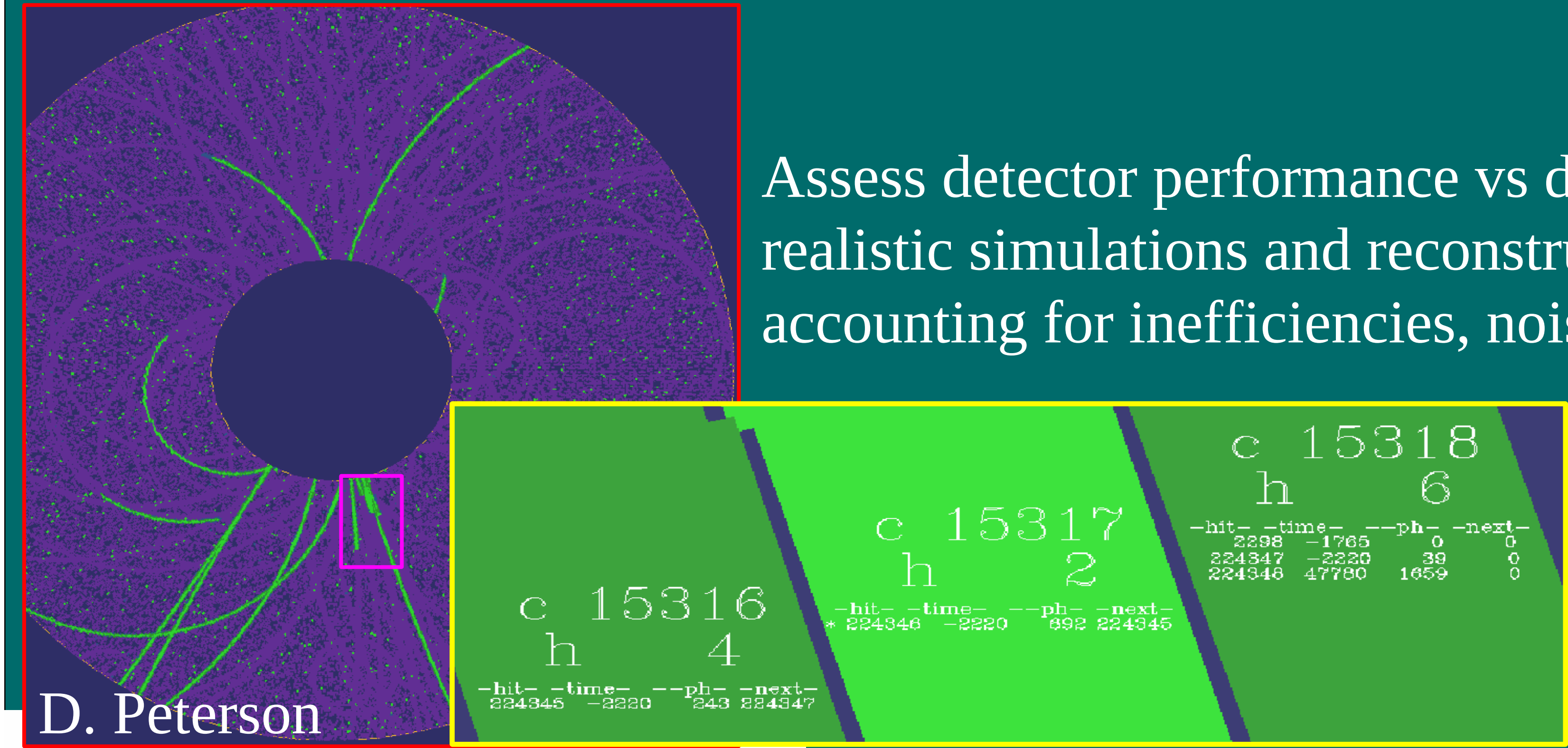
SiLC Coll.

Development of long ladders with long shaping time
Development of new VA chip tailored to LC application
Implement data sparsification and power cycling capabilities

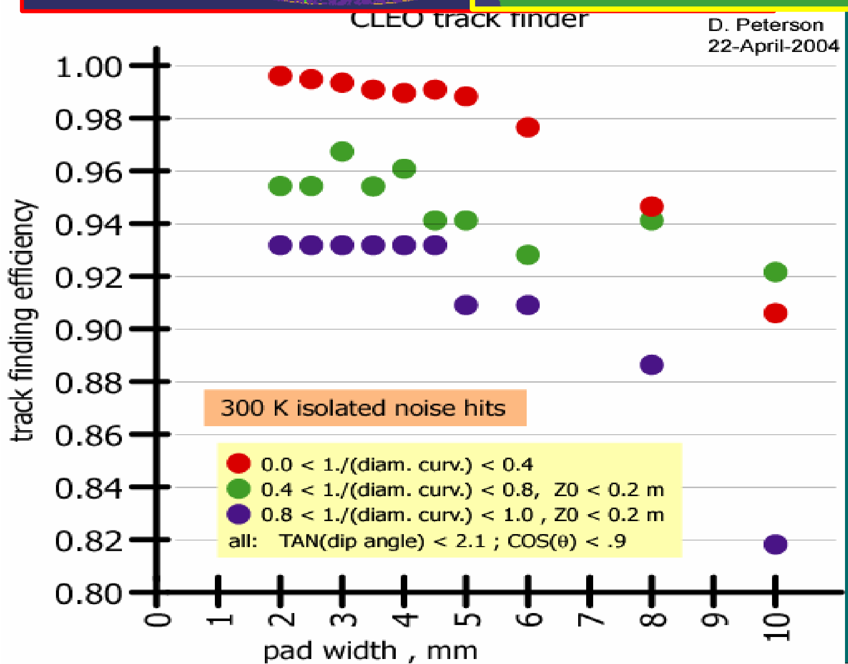
R&D on mechanics of long ladders, stability and cooling and global Tracker structure. Modules can also be adopted as supplemental tracking devices at TPC edges and for end-cap tracking planes



TPC PatRec and Track Reconstruction



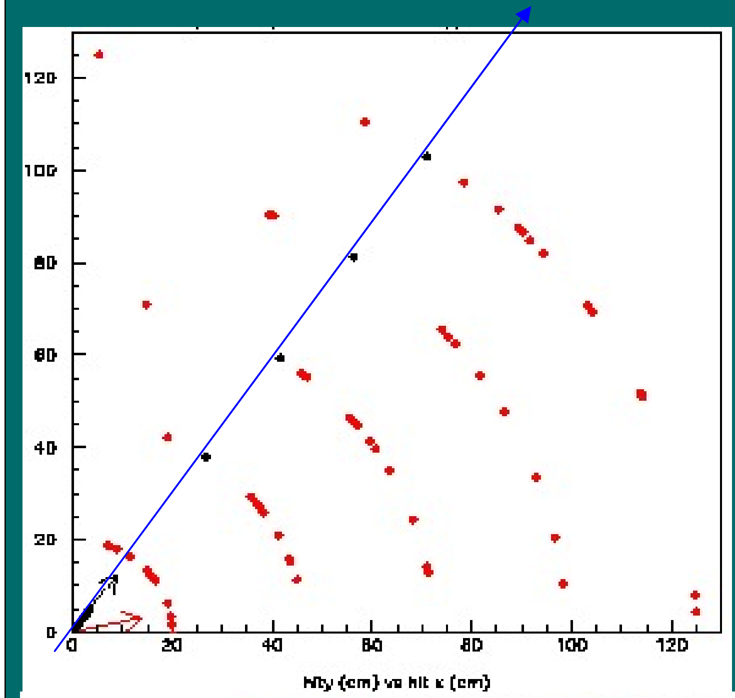
Assess detector performance vs design requires realistic simulations and reconstruction algorithms accounting for inefficiencies, noise, overlaps, bkgs.



Develop model within CLEO simulation and reconstruction framework which includes debugging tools for understanding reconstruction failures

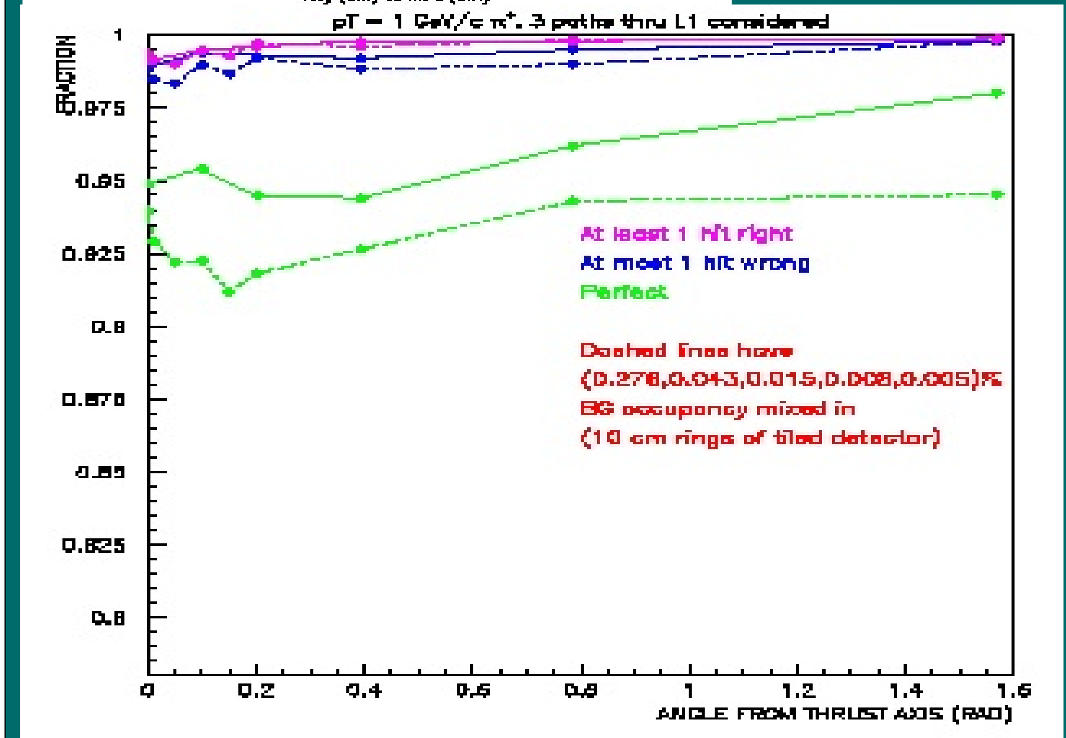
TPC Rec efficiency > 0.99 for non-curling trks and is unaffected by noise up to 1% occupancy

SiD Patrec and Track Reconstruction



qq Events at 0.5 TeV -> 45 hits/layer + Bkgs

Need to reduce occupancy/confusion by tiling (readout strips in modules (10x10 cm) rather than full half-barrel ladder) or timing to reduce bkg: R=20 cm layer occupancy = 0.83 -> 0.27



Defining efficiency as 9/10 hits correct (but 10% of tracks will have degraded resolution) give > 0.965-0.985 in jets

Study already gives useful feedback to R&D, need to extend to more complex events, address V^0 identification, ...

Status and Perspectives

Present talk would have been quite significantly different if written before this Workshop;

Physics program at LC is motivating a major R&D effort in sensors and detector concepts for achieving vertex and tracking with unprecedented accuracy;

Importance of efforts has motivated aggregation of several spontaneous regional and world-wide R&D collaborations;

To match LC detector road-map ahead, R&D must be guided by continuing physics and simulation programs and sustained by significant funding awarded to projects with highest priority for proving that the LC detector can deliver the accuracy that the LC physics needs.