Strategies for pickup and noise suppression with different vertex detector technologies

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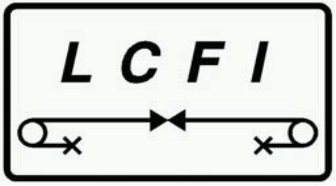
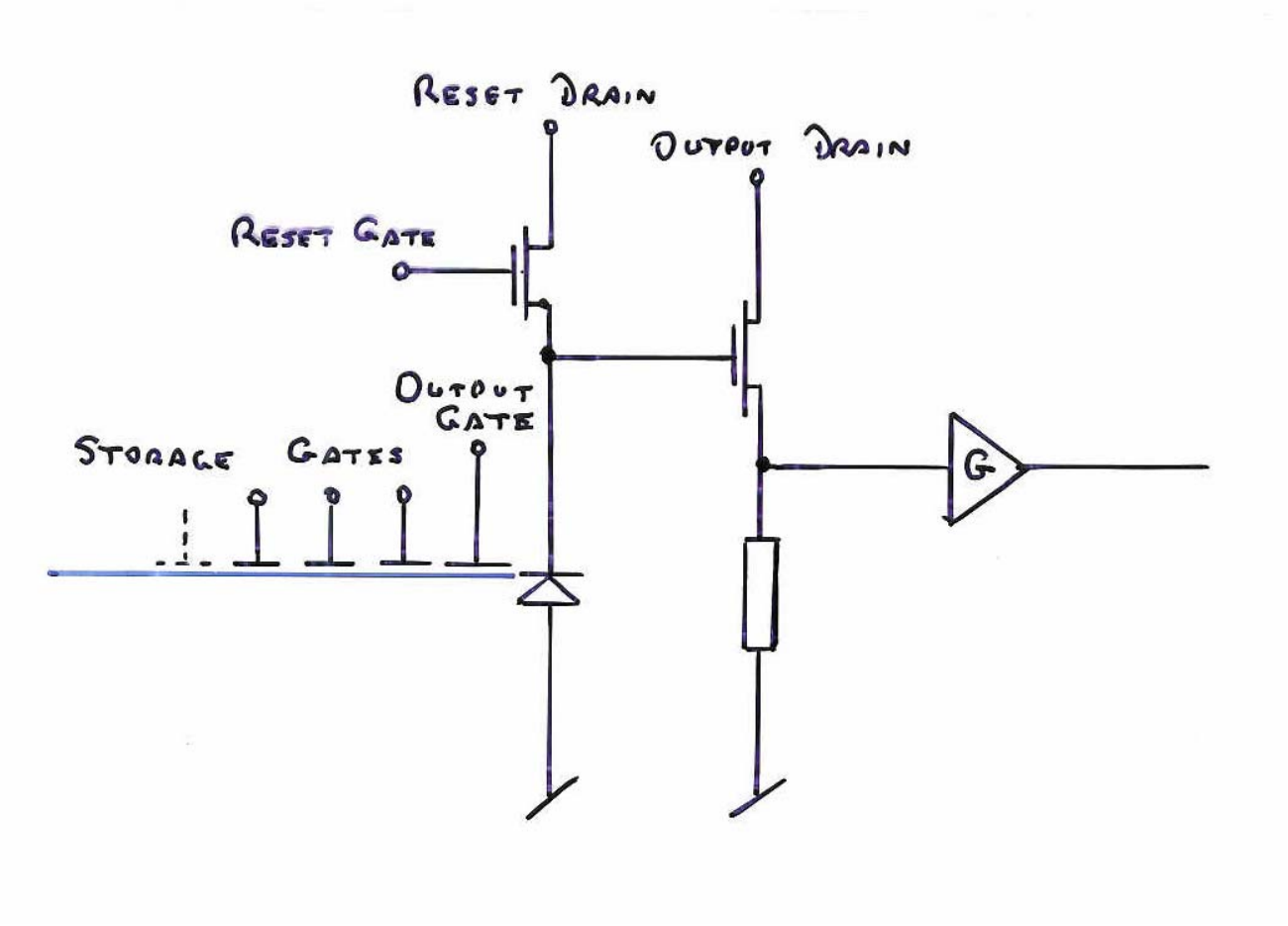
On behalf of the LCFI collaboration

- The challenge at TESLA: 10^9 tiny signals (~1000 e-) needing to be amplified purely electronically and read in conditions of severe beam-related RF pickup
- Reality check: 300 Mpixels at SLD
- Detector at NLC (natural evolution from SLD)
- Detector at TESLA
- Last December we thought of a possible solution (thanks to Renato Turchetta and David Burt for valuable discussions)
- We recently found that it isn't a new idea at all, and many of our requirements have been established. ISIS (Image Sensor with In-Situ Storage) looks extremely promising

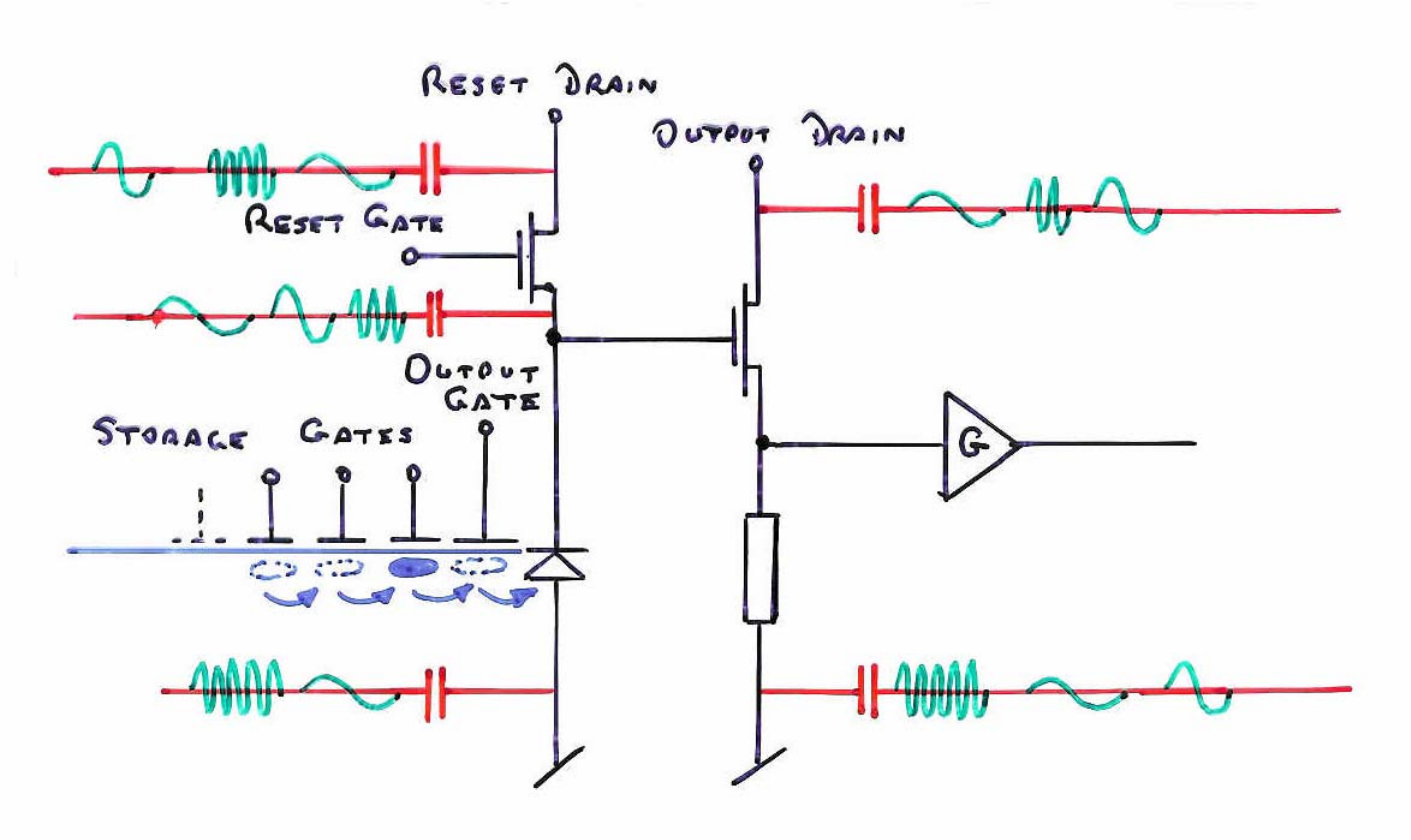


- A Linear Collider is intrinsically more hostile in terms of beam-related RF than storage rings. Why?
  - Collimators, beampipe irregularities, BPMs, position monitors can be much more disruptive, due to single pass operation
  - Due to requirement of nm spots, invasive diagnostic tools are essential. Imperfections in shielding of cables, optical ports, …
- Vertex detector is more vulnerable to pickup than others. Why?
  - Intimately enmeshed with beampipe – Faraday cage ideals tend to be compromised
  - Tiny signals from thin silicon active layers (~1000 e-) with need for purely electronic amplification
  - SLD experience: massive pickup observed, and optical transmission was disrupted by every bunch – took tens of μs to recover
  - However, a readout strategy was developed that worked …

Ideal CCD:

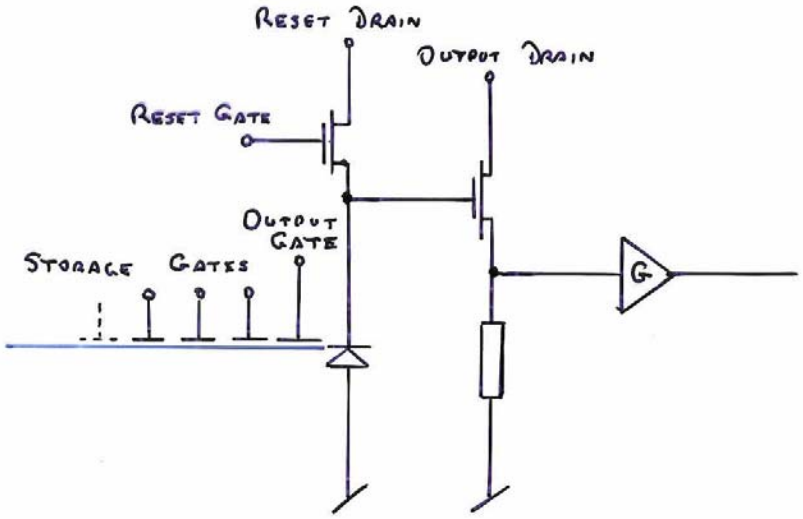

RESET DRAIN
OUTPUT DRAIN
RESET GATE
OUTPUT GATE
STORAGE GATES
G

Readout at Linear Collider during bunch train:



Malos's first rule of electronics: 'There is no such thing as ground …

Why *whisper* just when an express train roars through the station?

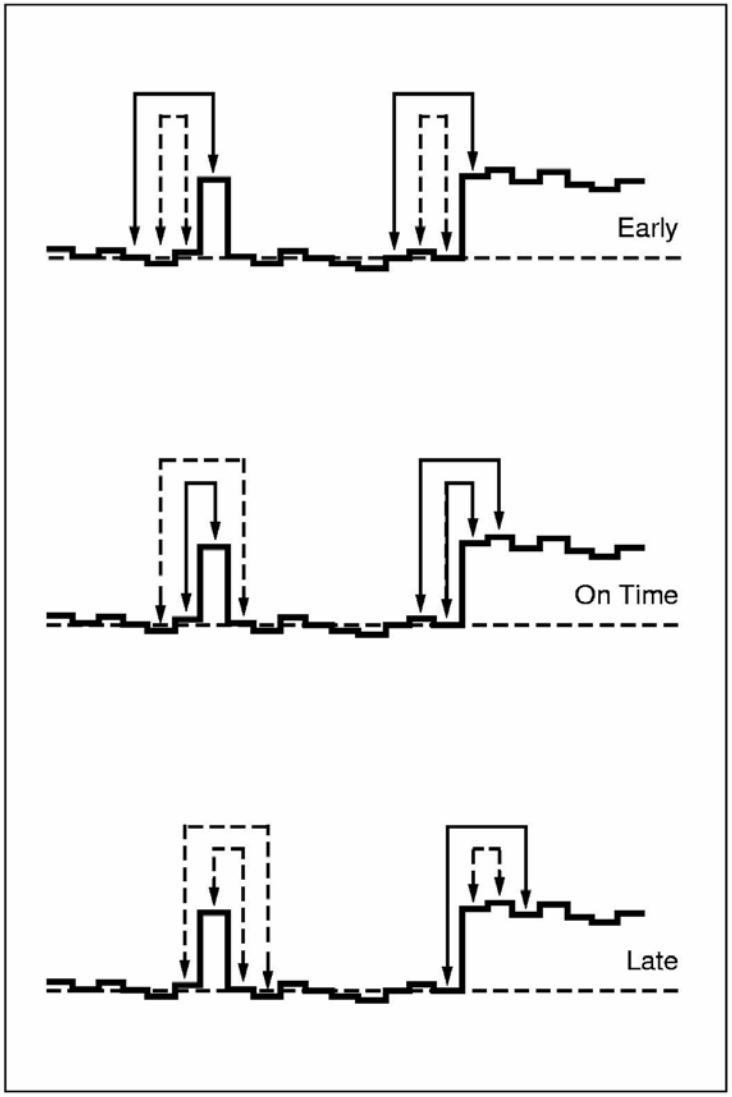


- **SLD approach:**
  - **During bunch train, signal charge from MIP is stored safely in buried channel of the device (~10^9 greater pickup immunity than output cct)**
  - **Only long afterwards, when pickup has died down, is charge transferred to output node and sensed as voltage on the gate of the output transistor. Even then, it is important to suppress pickup from non-beam sources …**
  - **Classical Correlated Double Sampling (CDS):**

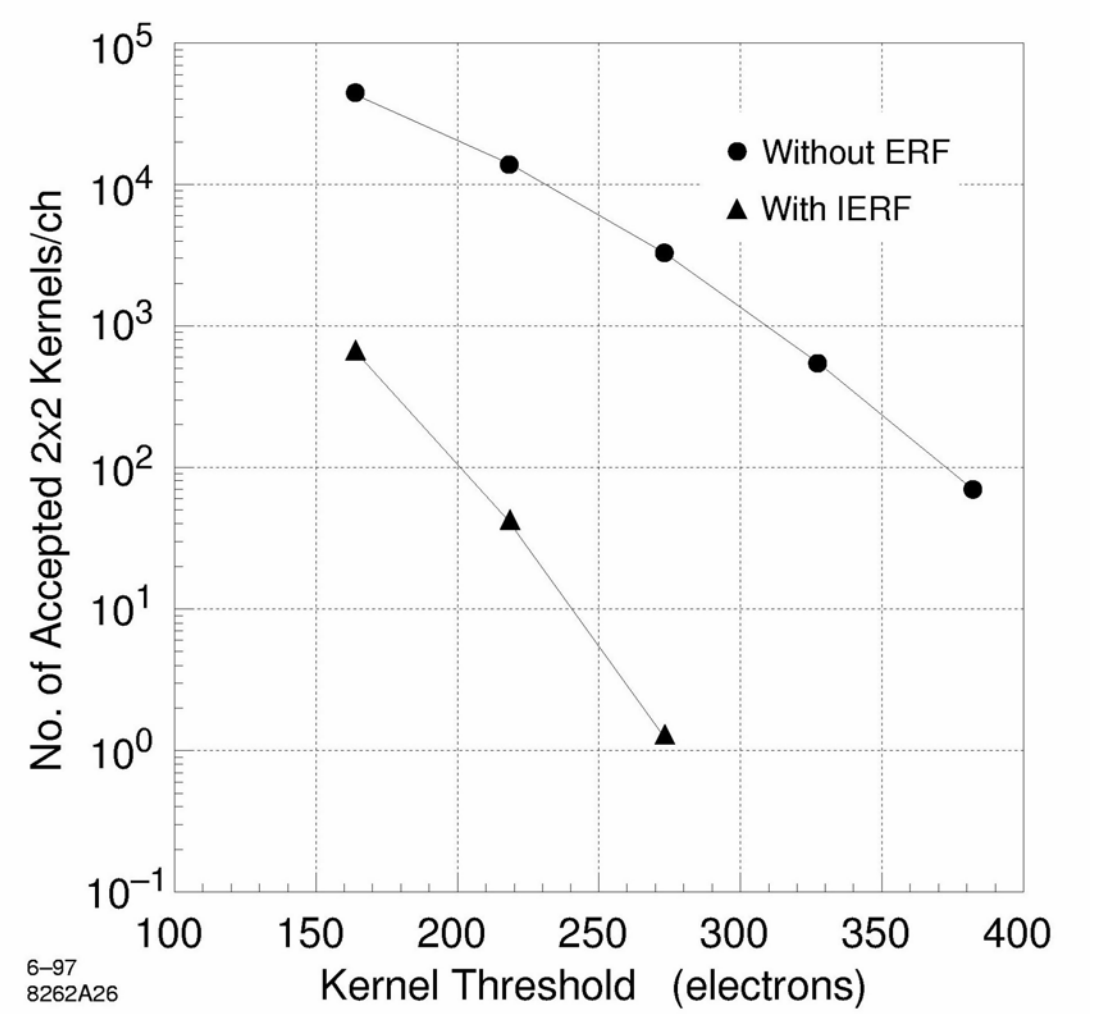
    RESET/READ 1/TRANSFER/READ 2 (originally to suppress reset noise)
  - **Sparse data scenario permits faster (but equivalent) noise suppression:**

    RESET/READ 1/TRANSFER/READ 2/TRANSFER/READ 3/ …

Extended Row Filter (ERF) suppresses residual pickup:



SLD experience:



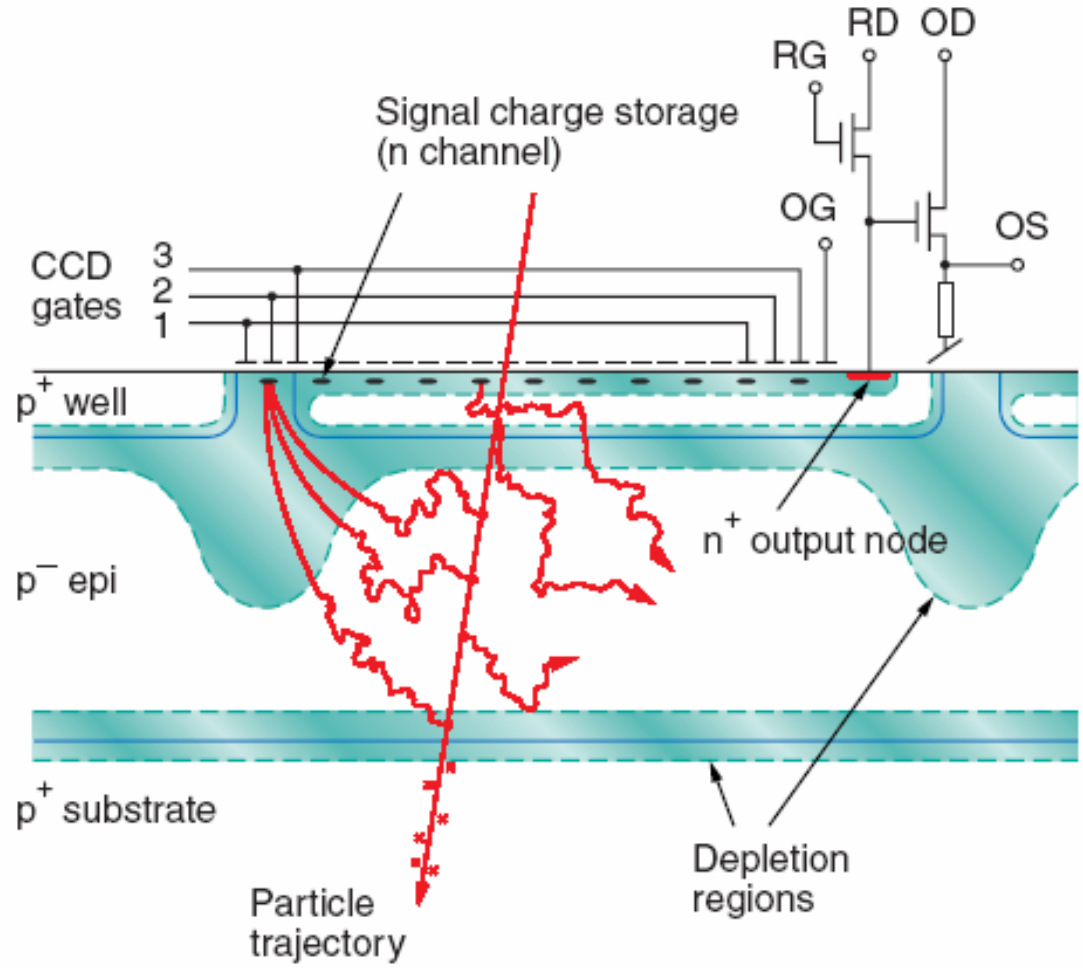
Without ERF, rate of trigger pixels would have deluged the DAQ system

Read out at 5 MHz, during 'quiet' inter-bunch periods of 8 ms duration

Origin of the pickup spikes? We have no idea, but not surprising given the electronic activity, reading out other detectors, etc

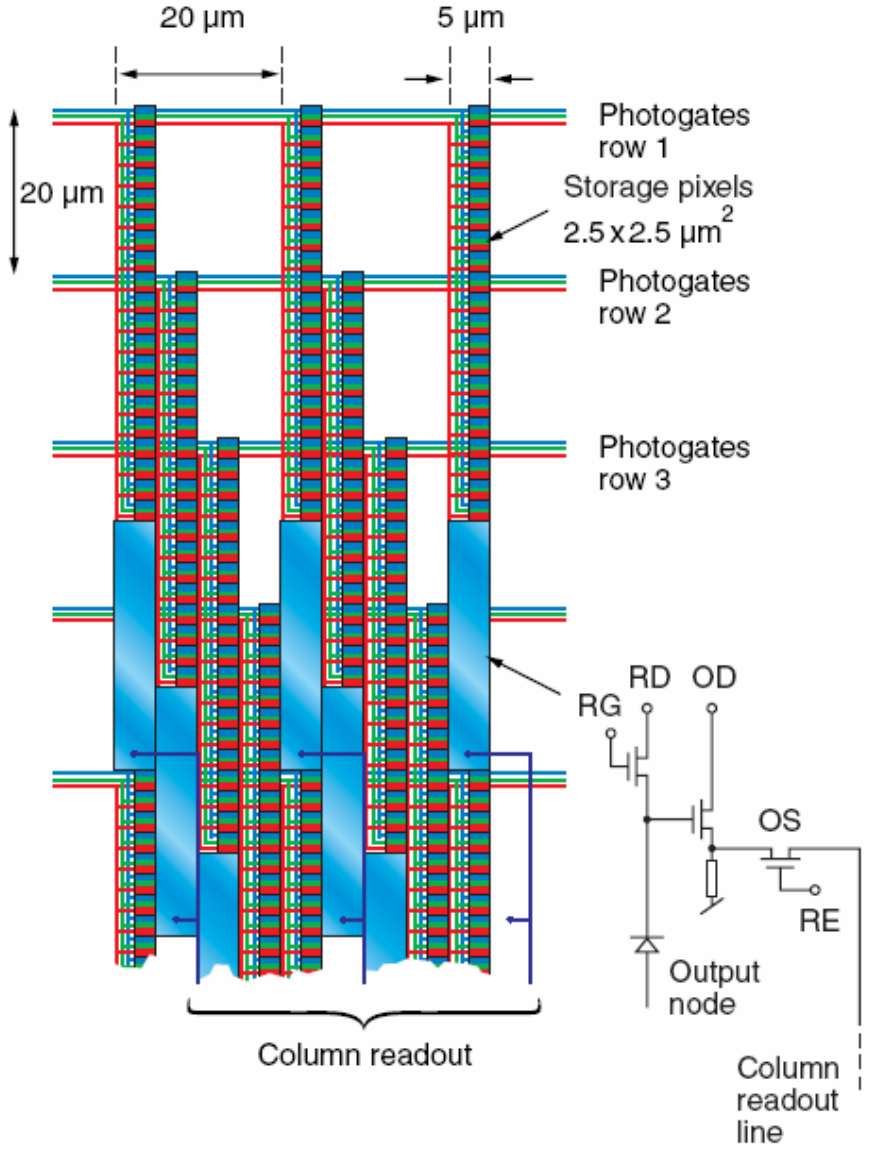
In-situ storage of signal charge: a new architecture for TESLA

- Strategy of reading inner layer 20 times during the train is now considered to be suspect
- Simulation is impossible – at least according to all RF experts we have consulted
- Idea of 'final focus lab' has been proposed, but regarded with great scepticism – everything depends on minor details. Under pressure of the real installation process, these details will not be precisely replicated
- If there are problems, diagnosis is almost impossible. Can only run beams with the detector closed
- So we looked for a solution which avoids multiple readout of voltage signals – wait till the express trains have long ago disappeared into the beam dumps!
- Secret may lie in the robust storage of charge in a buried channel, which cannot be disrupted even by massive pickup to the clocking gates or to ground
- Strategy is to transfer signal charge from photogate to a linear register inside each pixel, at intervals of 50 μs

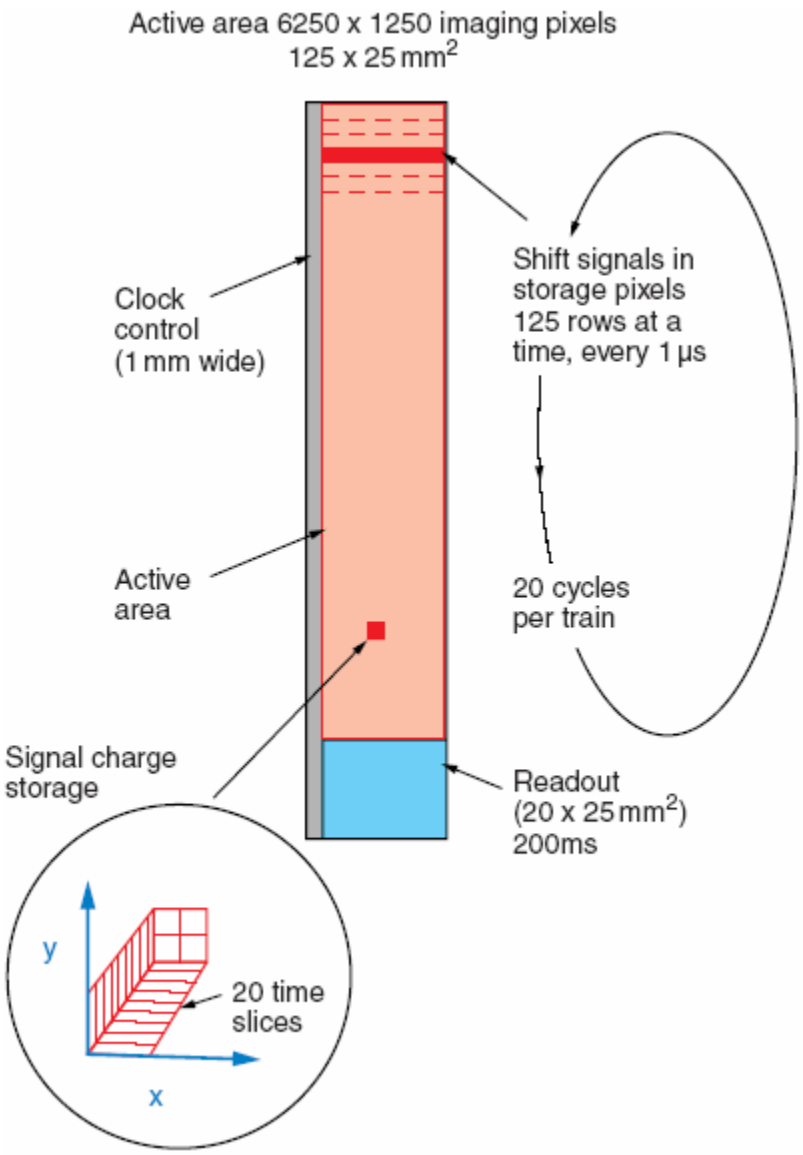


- **charge collection to photogate from 20-30 μm silicon, as in a conventional CCD**
- **signal charge shifted into storage register every 50μs, to provide required time slicing**
- **string of signal charges is stored during bunch train in a buried channel, completely avoiding charge-voltage conversion**
- **totally noise-free charge storage, ready for readout in 200 ms of calm conditions between trains**
- **particles which hit the storage register (~30% area) leave a small 'direct' signal (~5% MIP) – totally negligible or easily corrected**

Pixel unit cell: practical layout

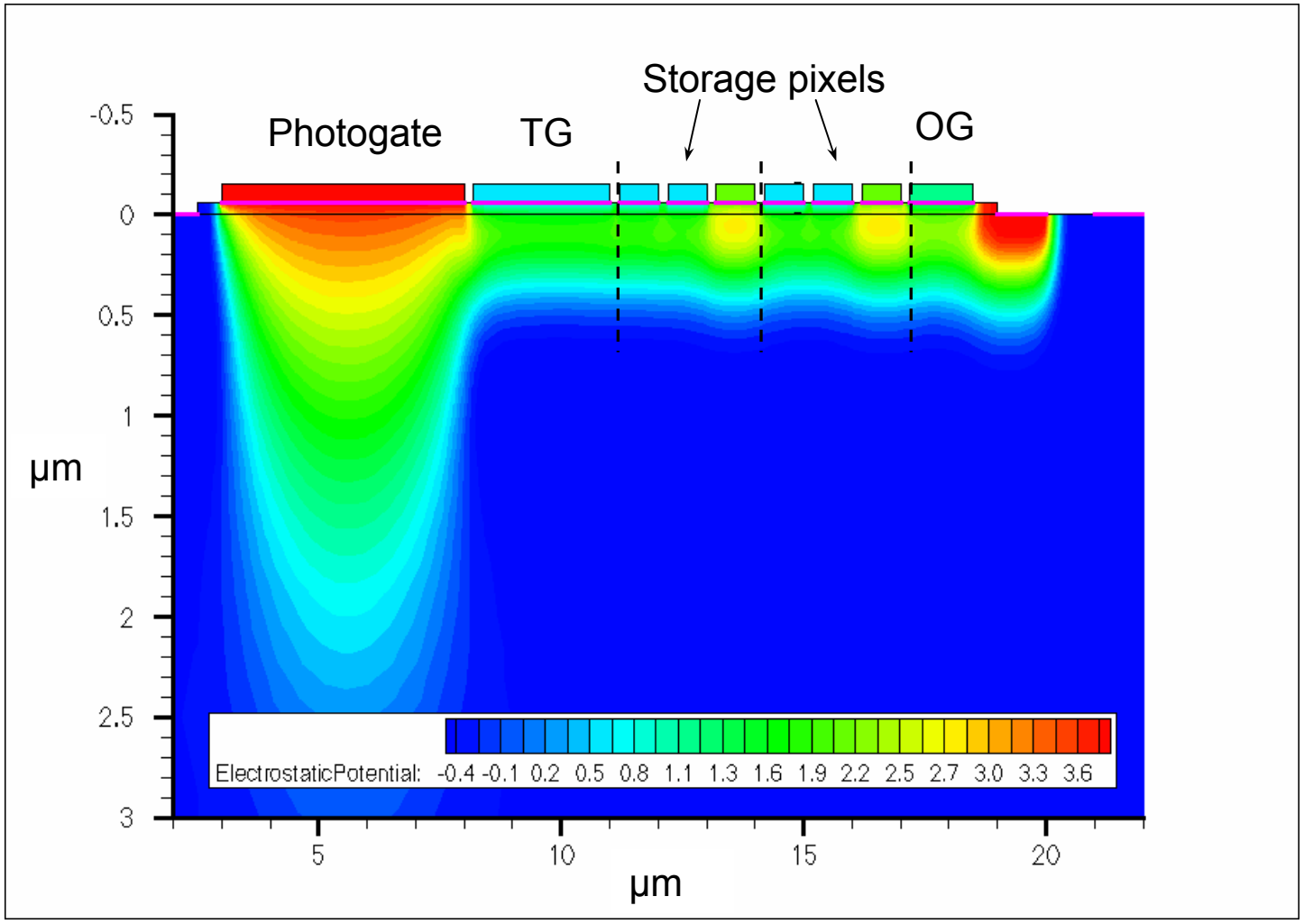


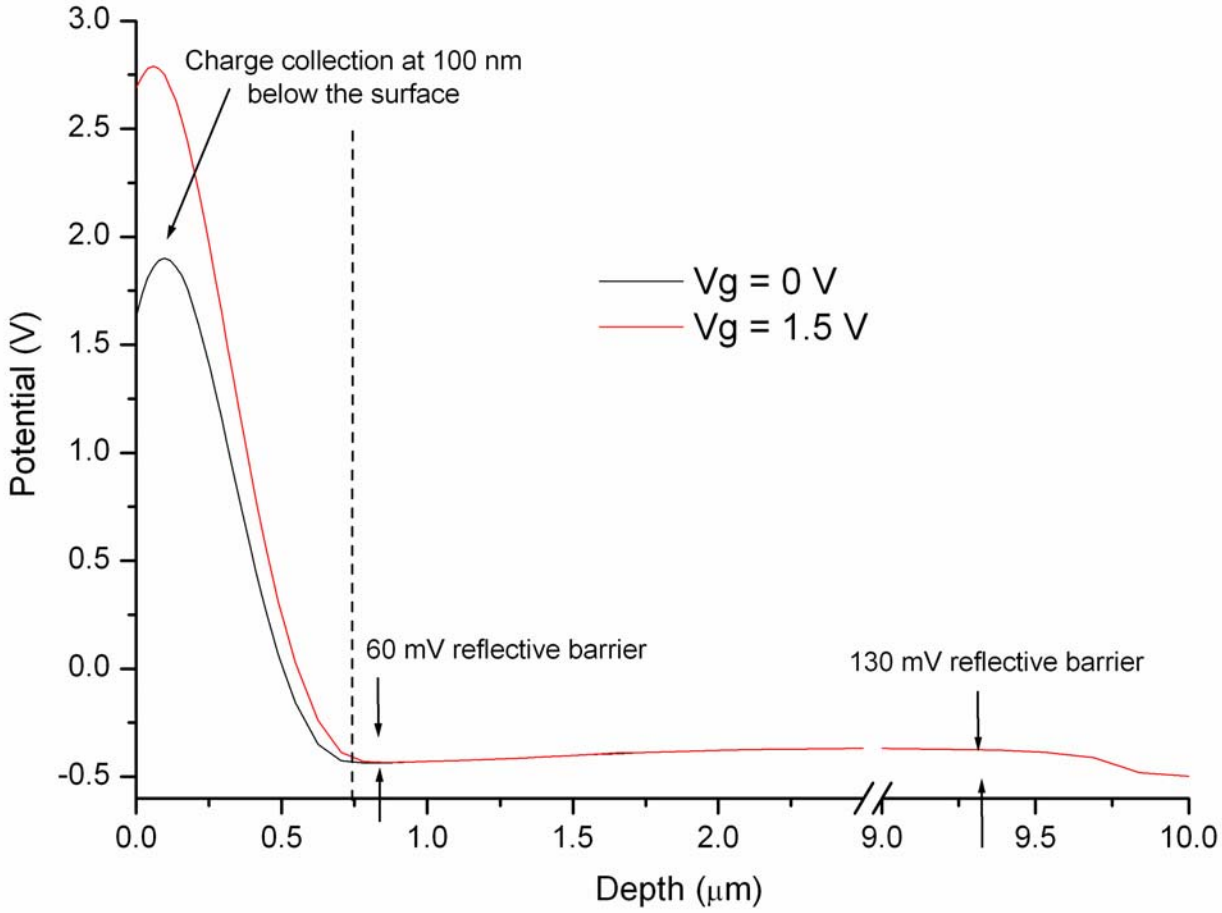
- **imaging pixels on 20x20 µm² slightly trapezoidal layout**
- **storage register plus output circuit fits within 5x80 = 400 µm²**
- **output cct is usual 3 T, plus a row enable switch to close connection to column readout busline**

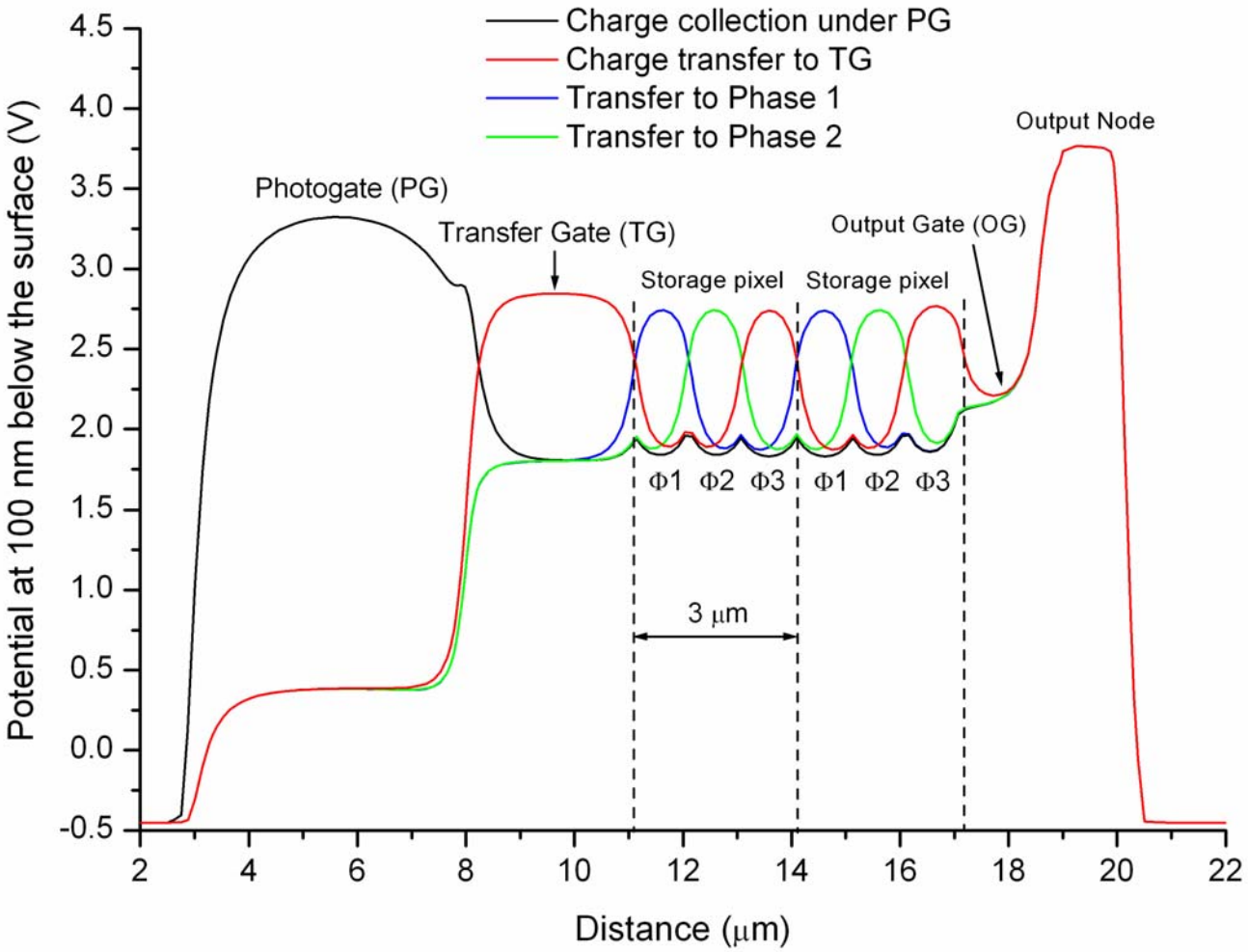


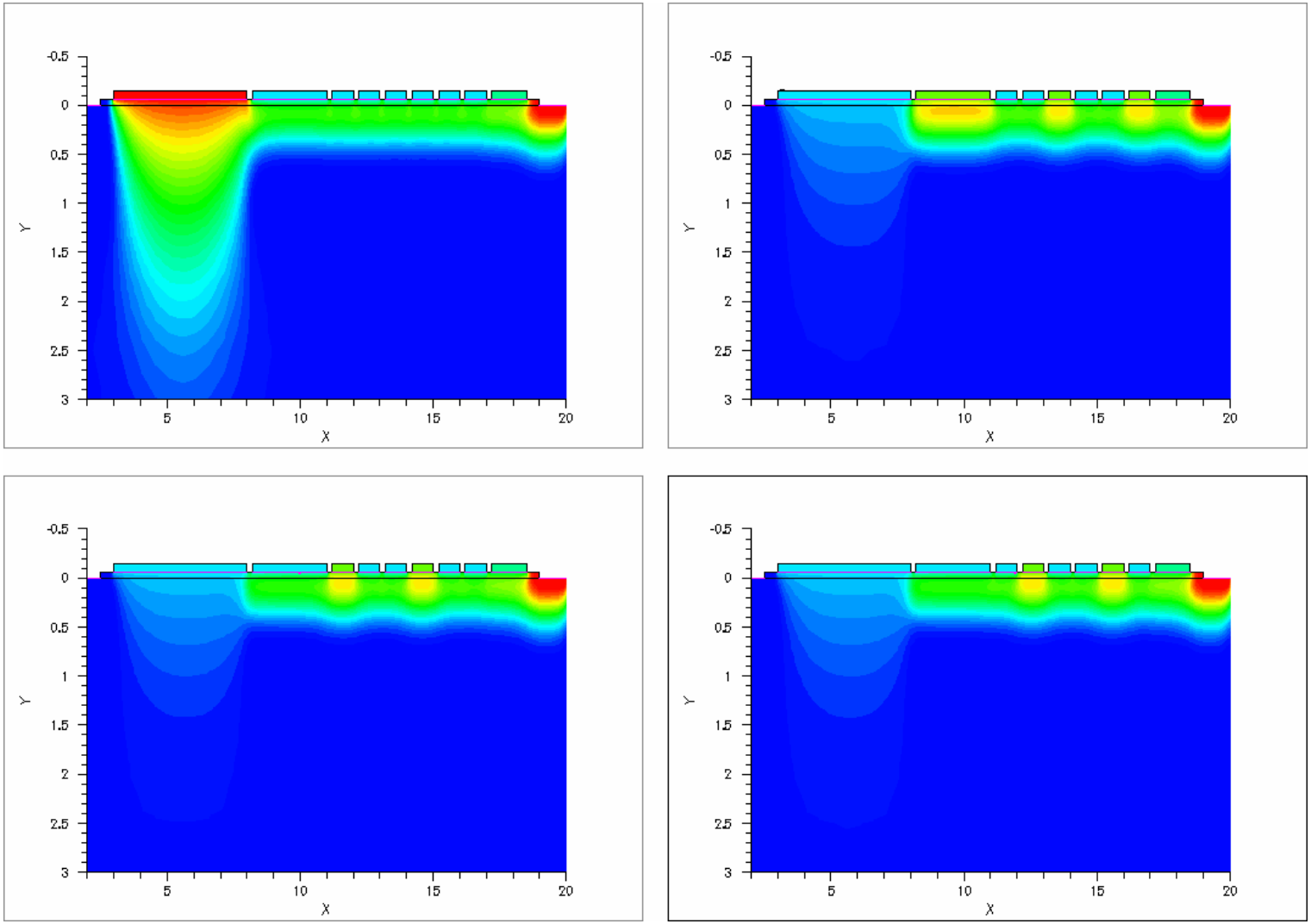
- during bunch train, shift 128 rows at a time by 1 storage pixel, at relaxed frequency of 1 MHz
- cycle round active area (length 12.5 cm) every 50 µs
- at end of train, every imaging pixel contains stored signal charges for 20 time slices
- between trains, column parallel readout just as in CPCCD
- full power of CDS and ERF in quiet inter-train period, as at SLC or NLC
- Relaxed sampling at 1 µs per stored signal implies 125 ms for complete detector readout
- no problem to process $2*10^{10}$ signals with low noise and effective pickup suppression
- could change from 128 to 256, 512, .. rows per block, at even more relaxed frequency – detailed question of optimising driver design

Following 4 beautiful simulation slides thanks to Konstantin Stefanov and ISE-TCAD

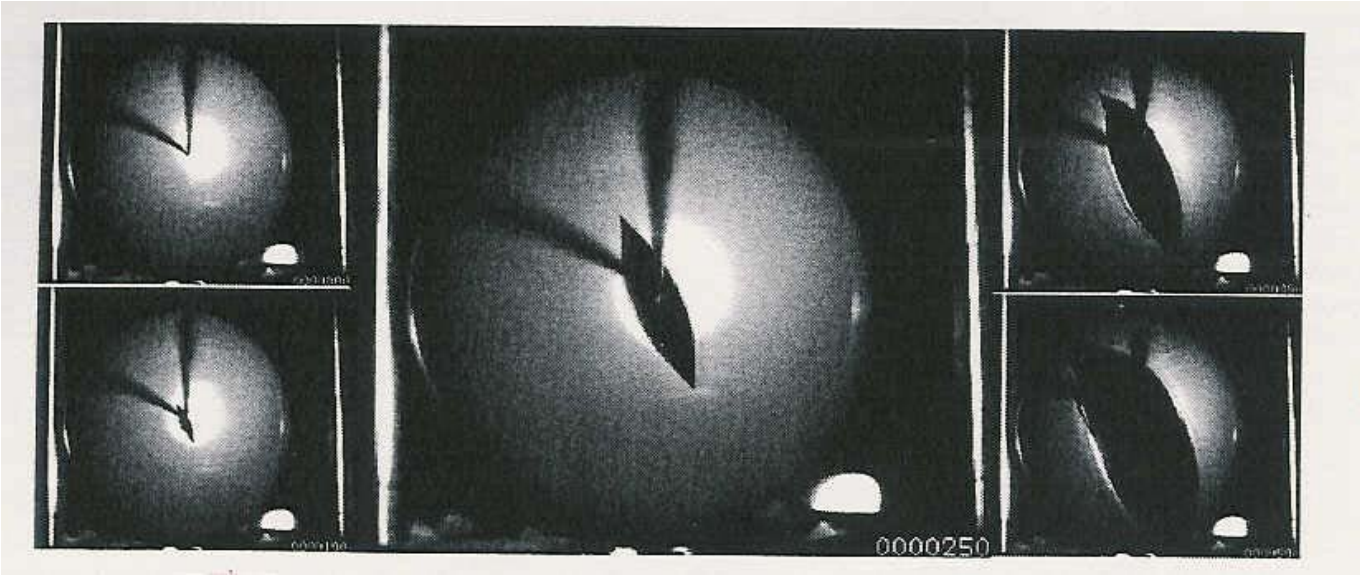



Charge collection at 100 nm
below the surface
Vg = 0 V
Vg = 1.5 V
60 mV reflective barrier
130 mV reflective barrier
Potential (V)
Depth (μm)
3.0
2.5
2.0
1.5
1.0
0.5
0.0
-0.5
0.0
0.5
1.0
1.5
2.0
9.0
9.5
10.0


Charge collection under PG
Charge transfer to TG
Transfer to Phase 1
Transfer to Phase 2
Photogate (PG)
Transfer Gate (TG)
Storage pixel
Storage pixel
Output Gate (OG)
Output Node
Φ1 Φ2 Φ3 Φ1 Φ2 Φ3
3 μm
Potential at 100 nm below the surface (V)
Distance (μm)
4.5
4.0
3.5
3.0
2.5
2.0
1.5
1.0
0.5
0.0
-0.5
2
4
6
8
10
12
14
16
18
20
22


-0.5
0
0.5
1
1.5
2
2.5
3
Y
5
10
15
20
X

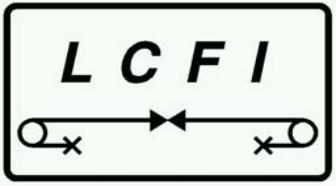
ISIS: Imaging Sensor with In-situ Storage



- Pioneered by W F Kosonocky et al IEEE SSCC 1996, Digest of Technical Papers, p 182
- T Goji Etoh et al, IEEE ED 50 (2003) 144
- 1 Mfps, seen above running at 100 kfps (312x260 pixels) – dart bursting balloon
- Evolution from 4500 fps sensor developed in 1991, which became the de facto standard high speed camera (Kodak HS4540 and Photron FASTCAM)

Feature	ISIS 2003	Goal for TESLA
Particle-sensitive?	no	yes
Imaging pixel size μm^2	66x66	20x20
Storage pixel size μm^2	5.1x5.1	2.5x2.5 *
Frame rate	1 MHz	20 kHz
Frames stored	100	20
Resolution (amplitude)	10 bits	5-6 bits
Well capacity	25000 e-	5000 e-
Pickup immunity	solid	solid
Radiation resistance	??	Robust – easy to achieve 100 times standard CPCCD

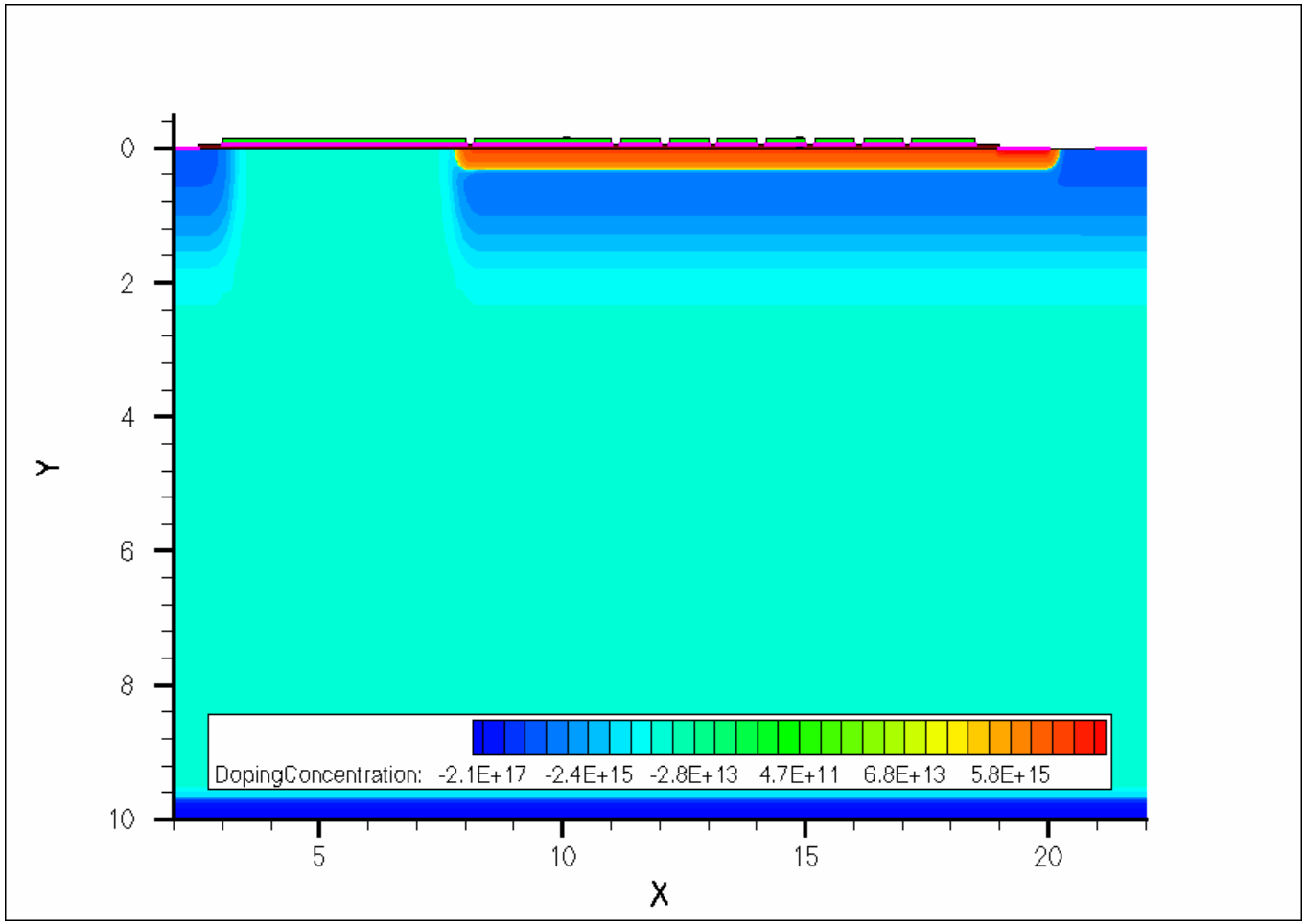
* Kosonocky achieved 1.5x3 μm^2 BCCD storage elements in 1996 with 1.5 μm design rules!

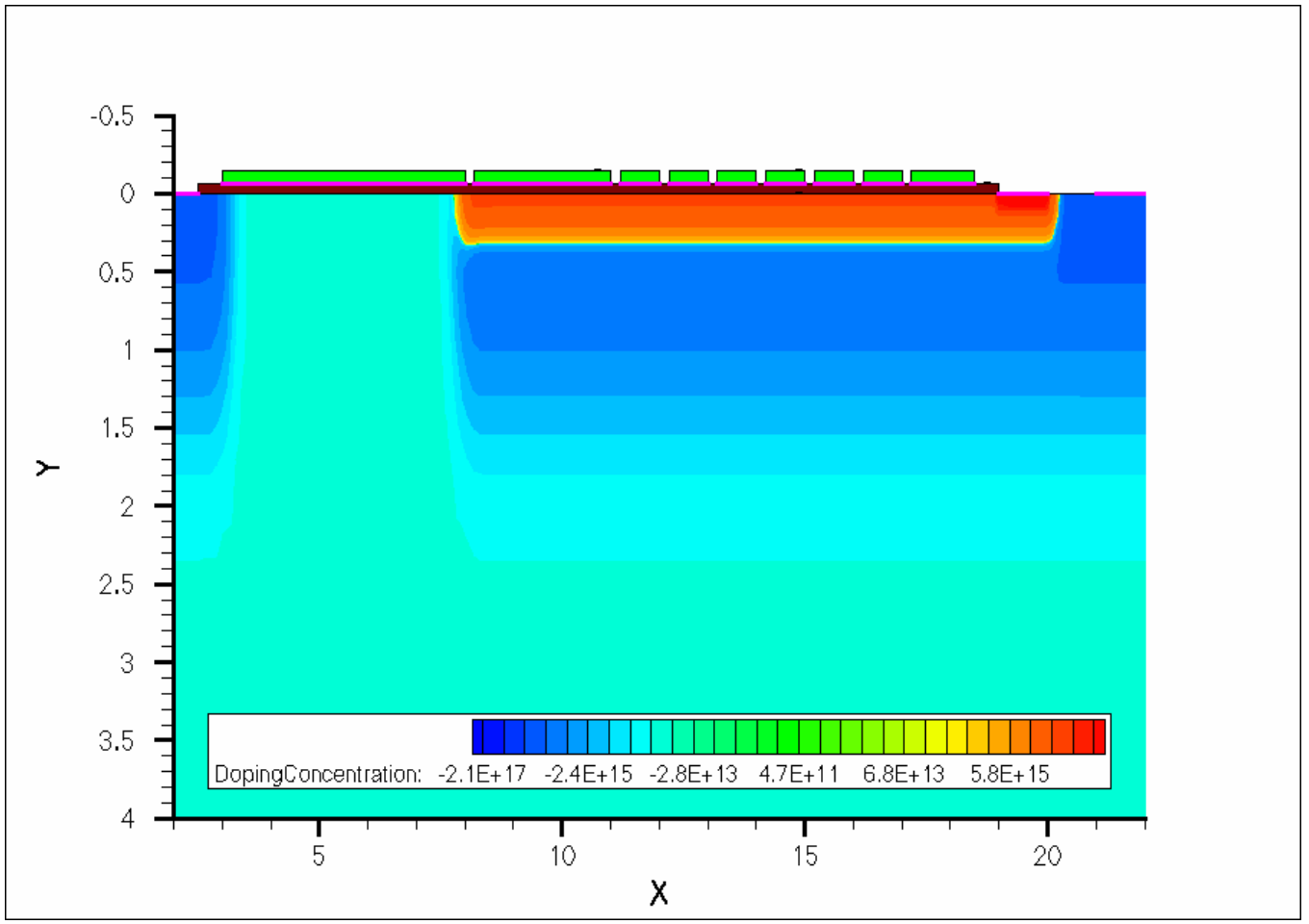


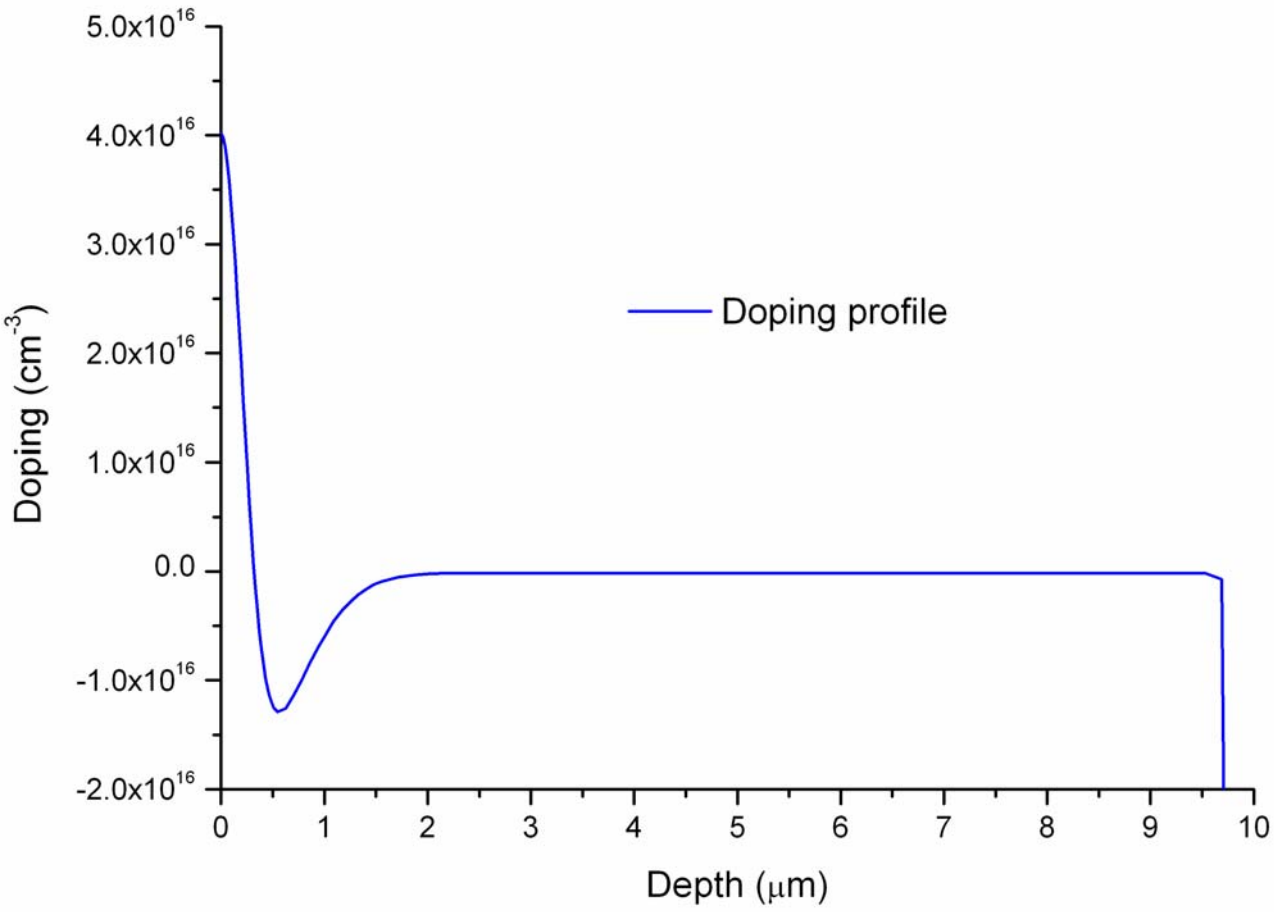
- **Manufacture requires specific features drawn from ‘standard’ CCD and CMOS technology:**
  - **2 or 3 metal layers for horizontal and vertical tracks**
  - **Design rules 1.5 μm or better**
  - **large area precise stitching, of course**
- **Such flexibility is available in companies producing advanced imaging devices, but not ‘off the shelf’**
- **Development being explored with e2V, DALSA Image Sensors (formerly Philips Scientific Imaging) and Sarnoff (formerly RCA)**

CONCLUSIONS

- The combination of tight collimation (generating large wakefields) and instrumentation essential for a single pass collider (BPMs etc) tends to create severe RF pickup during the bunch train – already encountered at SLC, and probably more extreme at the TeV collider
- One should aim to avoid delicate voltage sensing and amplification during this period
- ISIS - Imaging Sensor with In-situ Storage, in principle offers a solution to the problem
- Required developments appear to be achievable, much more so than we imagined last December when we thought we had invented the idea ourselves!
- 'Standard' CPCCD looks fine for NLC, but for TESLA we have started a serious evaluation of the ISIS architecture as a promising way forward.
- Solves other problems with the CPCCD approach: dramatically reduced power requirements for CCD clocks, improved spatial resolution (maybe to ~1 μm), orders of magnitude overkill in radiation hardness, near-room temperature operation, …


0
2
4
6
8
10
Y
5
10
15
20
X
DopingConcentration: -2.1E+17 -2.4E+15 -2.8E+13 4.7E+11 6.8E+13 5.8E+15


-0.5
0
0.5
1
1.5
2
2.5
3
3.5
4
Y
5
10
15
20
X
DopingConcentration: -2.1E+17 -2.4E+15 -2.8E+13 4.7E+11 6.8E+13 5.8E+15


5.0x10^16
4.0x10^16
3.0x10^16
2.0x10^16
1.0x10^16
0.0
-1.0x10^16
-2.0x10^16
Doping (cm^-3)
Doping profile
0
1
2
3
4
5
6
7
8
9
10
Depth (μm)