

Electronics integration of the ALICE Pixel tracking detector

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CERN-PH/ED

DTI meeting
CERN, June 30, 2004

Outline

- No detailed technical presentation

- **What** should it do?
- **Why** is it difficult to make it?
- **How** did we solve the problem?

WHAT?

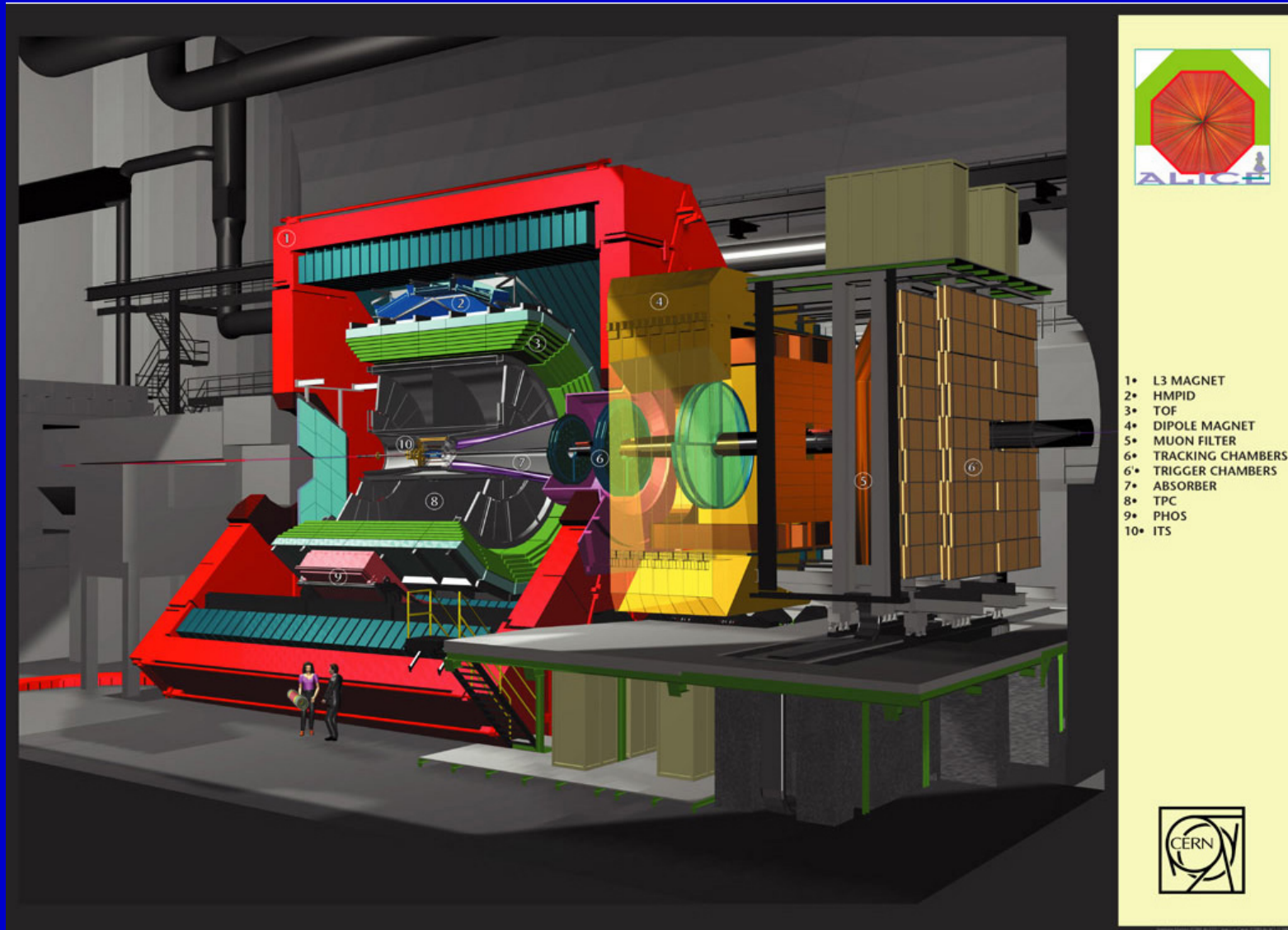
WHY?

HOW?

Only one attack of a block diagram



Silicon Pixel Detector in ALICE



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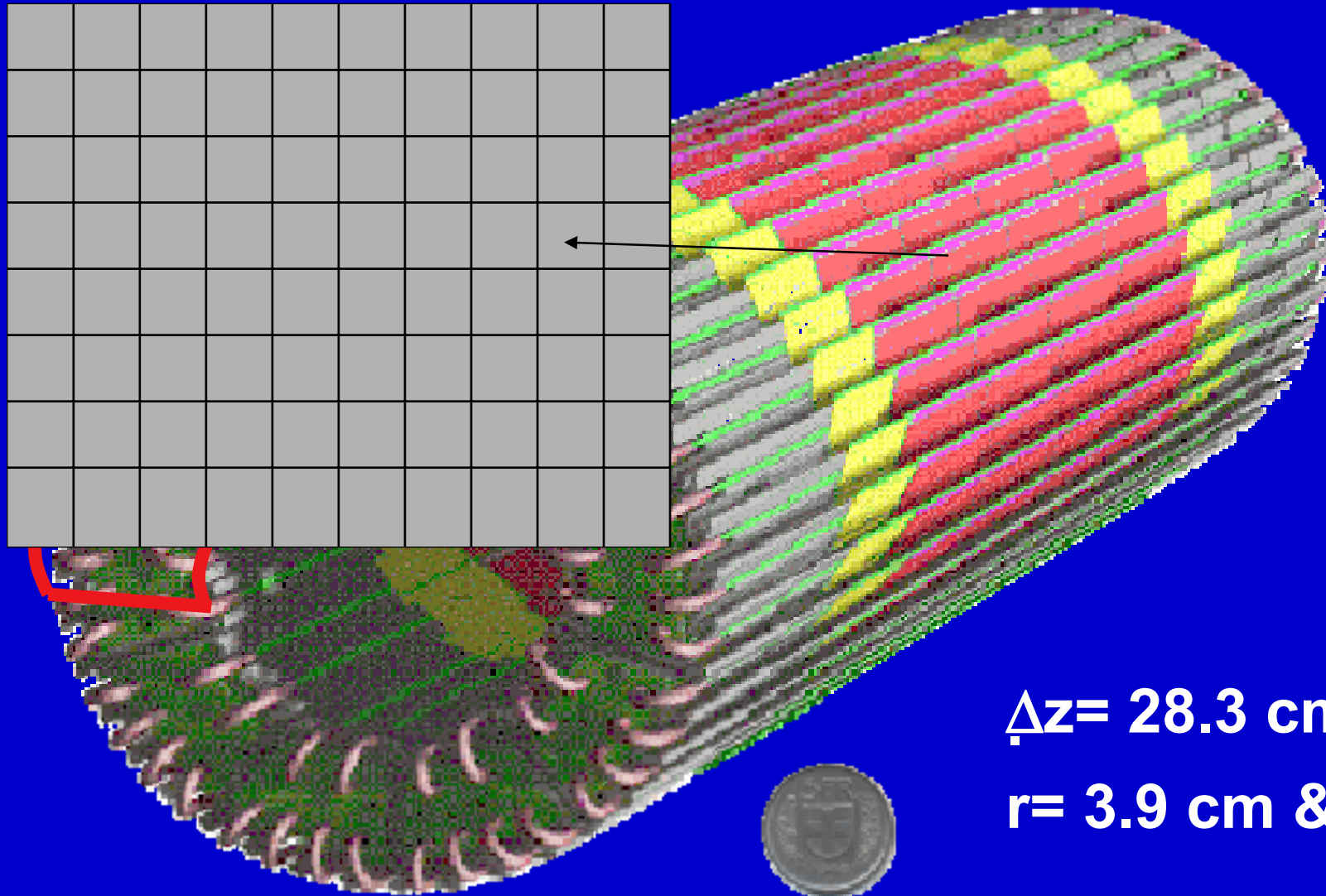


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SPD detector

WHAT?



$\Delta z = 28.3 \text{ cm}$

$r = 3.9 \text{ cm} \ \& \ 7.6 \text{ cm}$

Why is it so difficult?

WHY?

Challenges, Tasks to solve

Challenge

WHY?

- **Many channels in small volume**
 - 10 million channels in very confined physical space
- **1kW of power dissipation**
 - In a volume of 5 dm³
- **Limited amount of matter**
 - Material budget
- **Radiation**
 - 250 krad, Total dose effect and single event upset

Challenge

WHY?

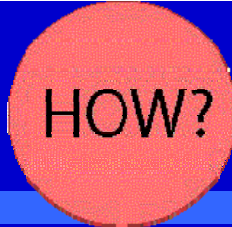
- **High data rate**
 - 1GByte/s
- **Data transfer over 100 m**
 - Signal integrity issues
- **Low number of modules**
 - Industry interest is usually for high quantities

Challenge

WHY?

- **Information whether collision occurred only after 6 us**
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- **Time available to readout data is 256 us**
- **Final application environment can only be simulated**

How?



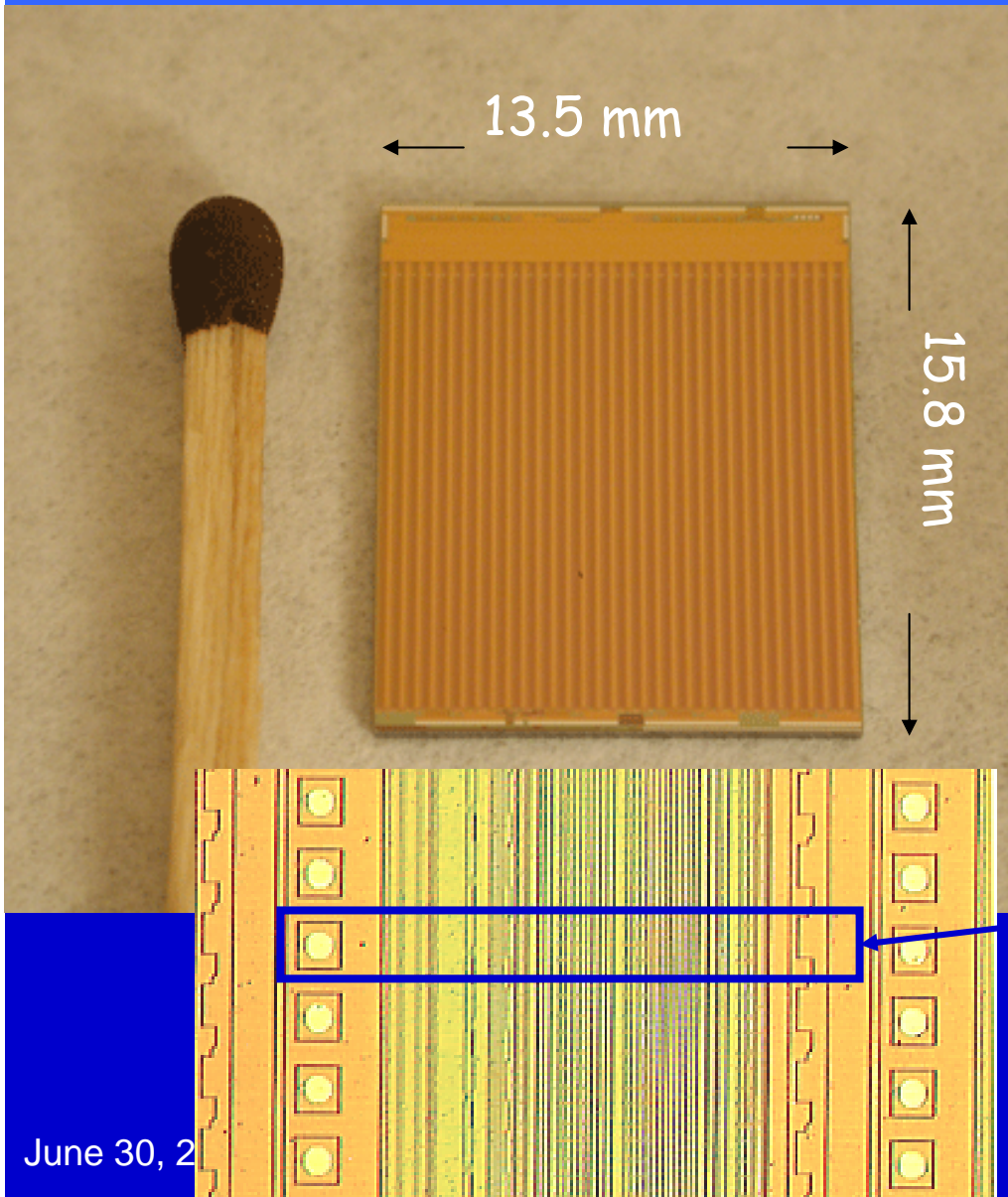
Challenge

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Pixel Readout Chip

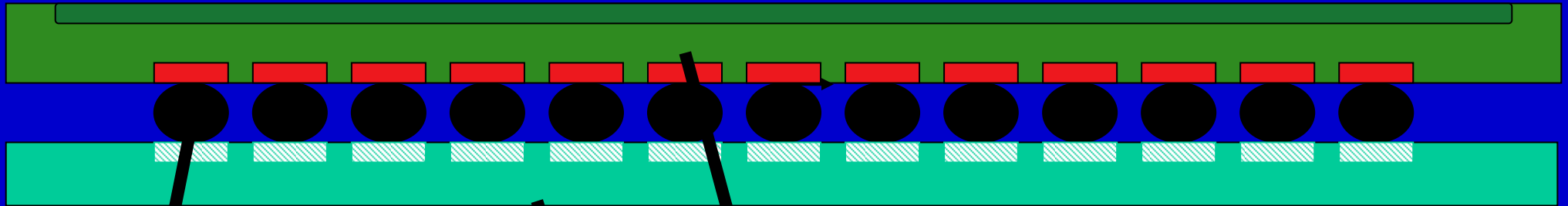
HOW?



- Mixed signal (analogue, digital)
- Produced in a commercial 0.25 μm CMOS process
- Radiation tolerant design (enclosed gates, guard rings)
- 8192 pixel cells
- 50 μm x 425 μm pixel cell
- ~100 μW /channel

Bump Bonding

HOW?



Bump-bonding:

- Pb-Sn solder bumps

Detectors:

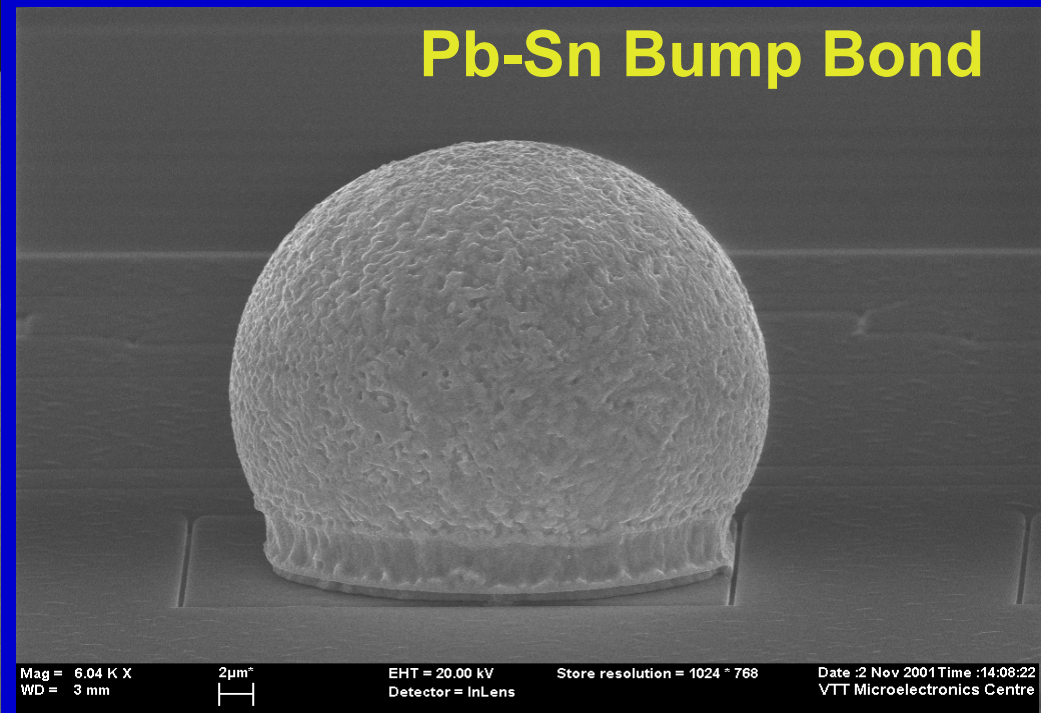
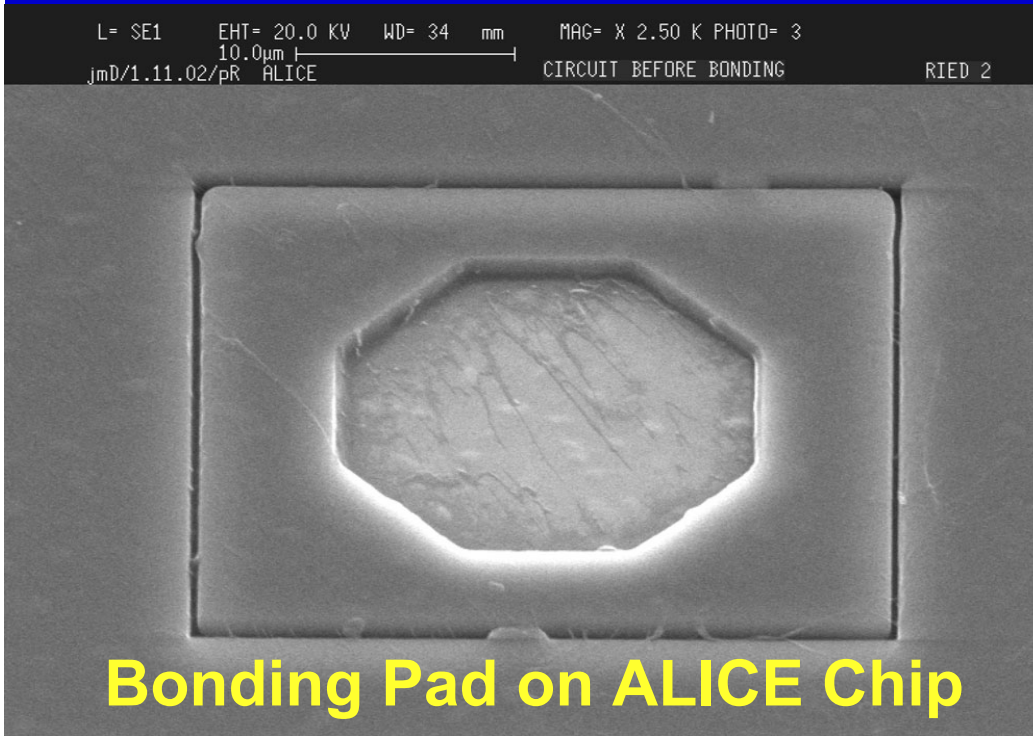
- 5 chip + detectors for ladders
- thickness: 200 μ m

Chips:

- thickness: 150 μ m

Bump Bonding

HOW?



SPD half stave

HOW?

On detector
Readout electronics

1 ladder

1 ladder

10 readout chips

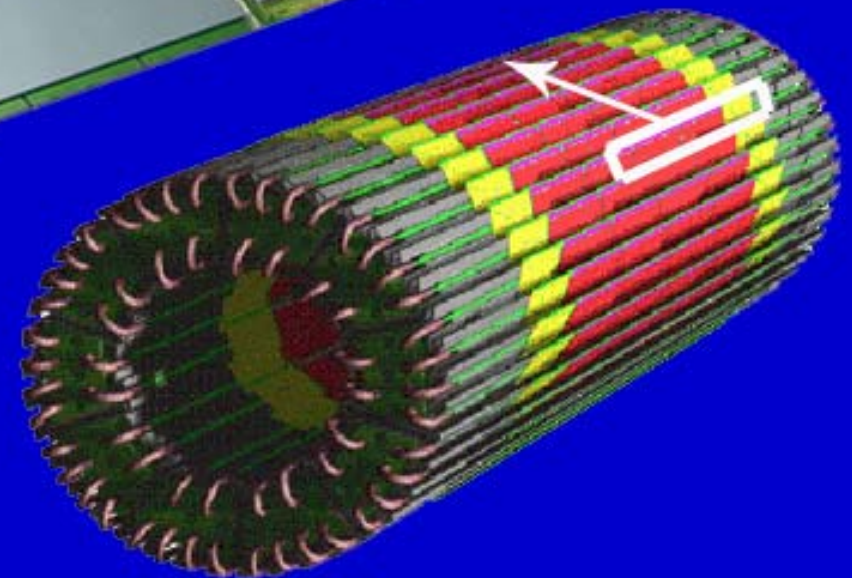
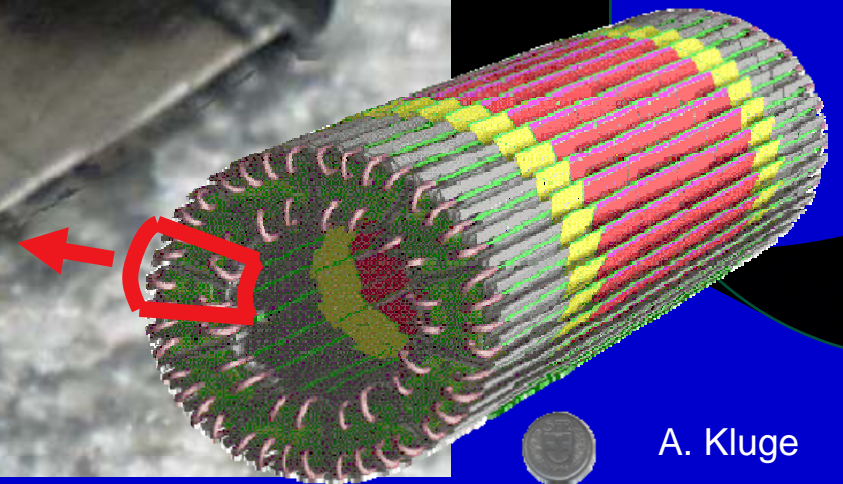


Image:INFN(Padova)

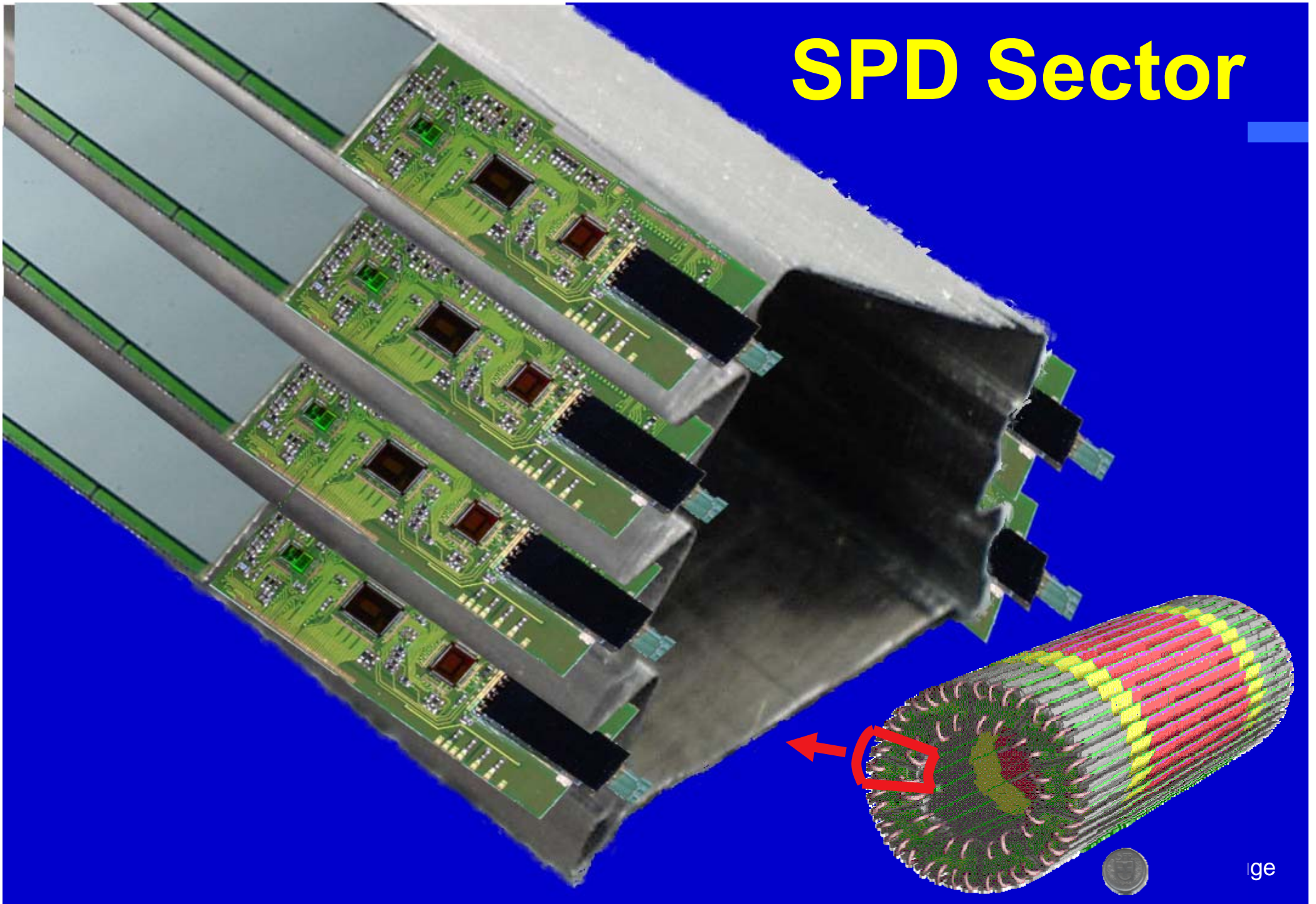
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SPD Sector



SPD Sector



On detector integration issues

- **No commercial electronics**
- **Small and THIN**
- **Small quantities**

No FPGAs -> custom designed ASICs

Prototypes are not accessible for debugging, fragile, cutting edge technologies

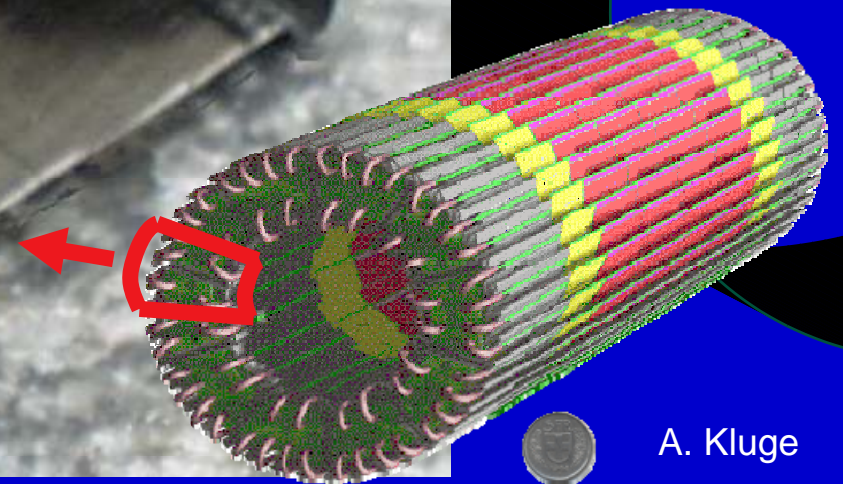
New technologies applied, lack of experience, turn around times

Challenge

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SPD Sector



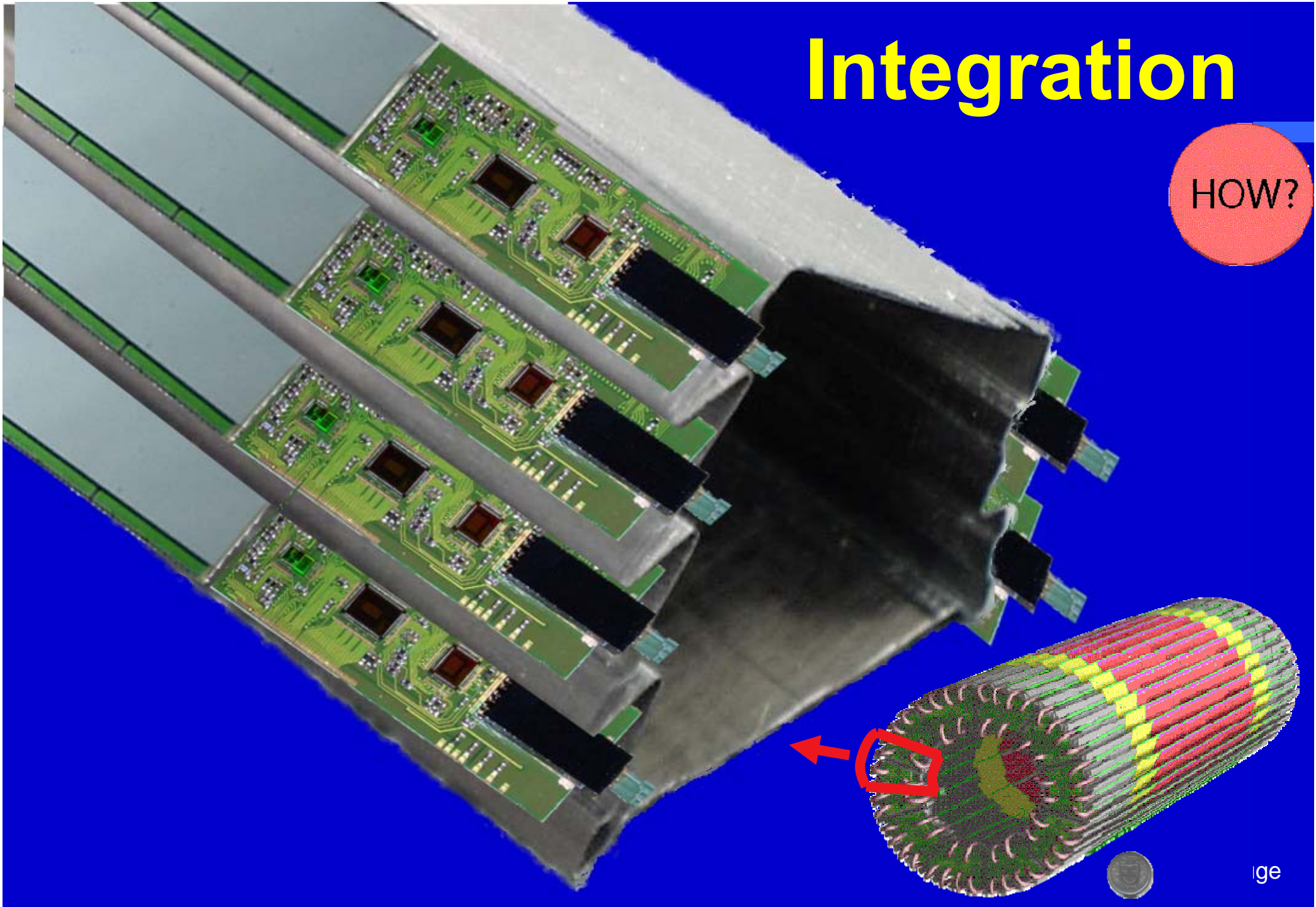
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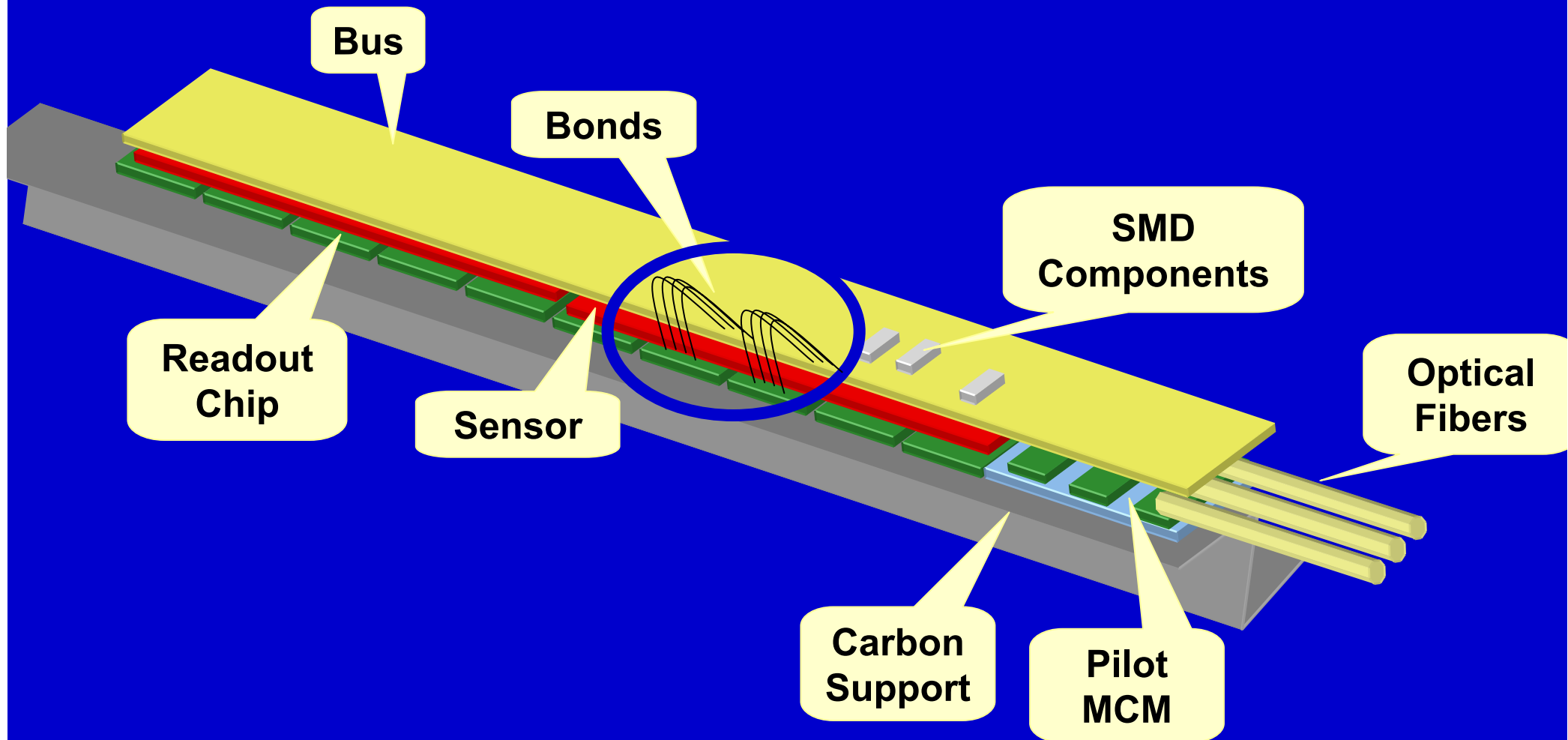
Integration

HOW?



Electronics integration

HOW?



The Bus

HOW?

Length: ~ 20 cm, width ~13 mm

Total thickness: 220 μm

5 layers: Power, GND, 3 signal layers

Each layer thickness: 5 μm to 30 μm

Length of stair: 500 μm

Distance of bonding pads: 120 μm

Aluminum Bus

HOW?

Material budget -> Aluminum,

No industrial solution

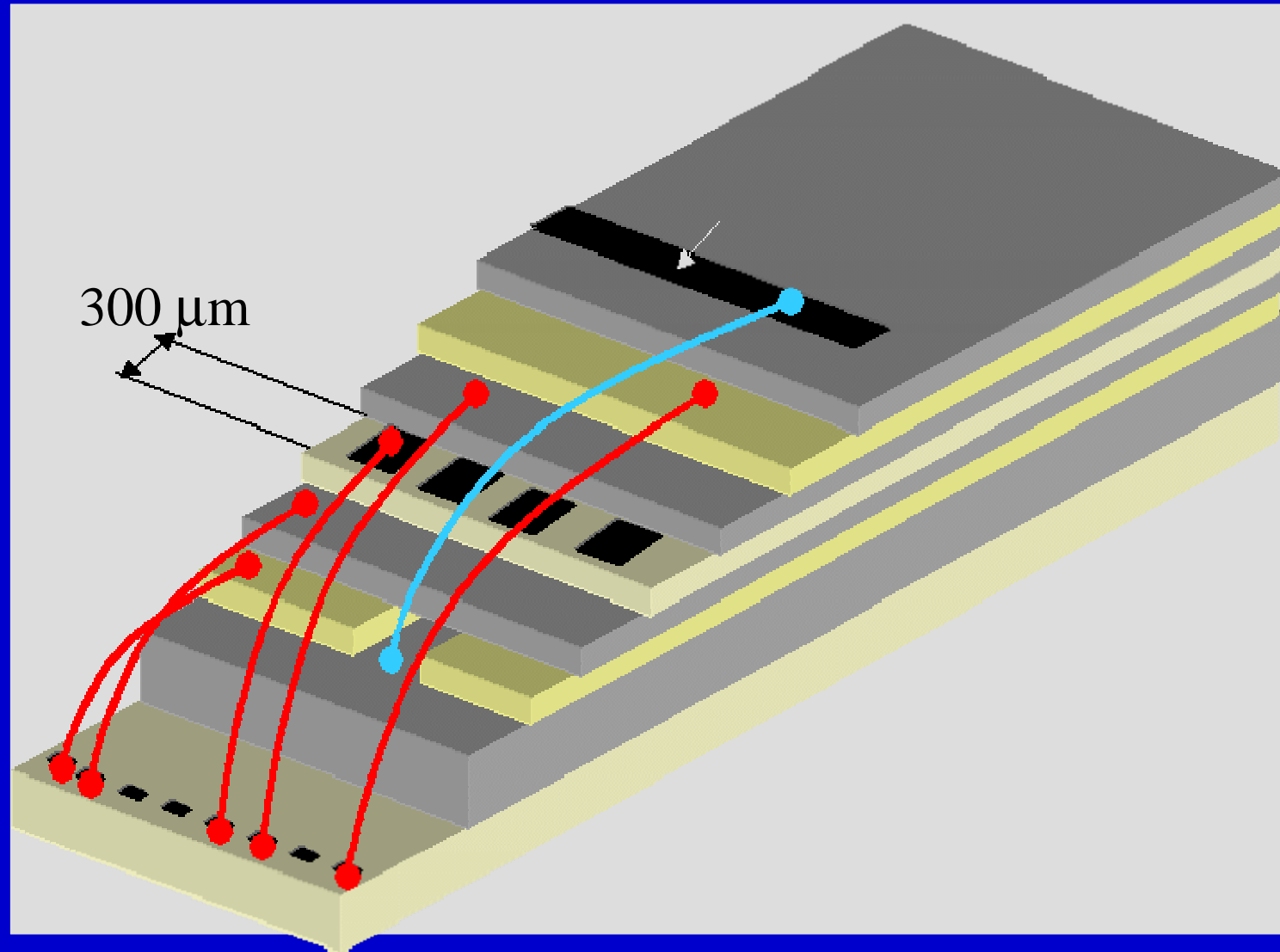
No previous experience of
Aluminium thin multi layer
structures

Connections between layers
(vias) are difficult to make

Vias only for signals
Power uses stair case
structure

The Bus

HOW?



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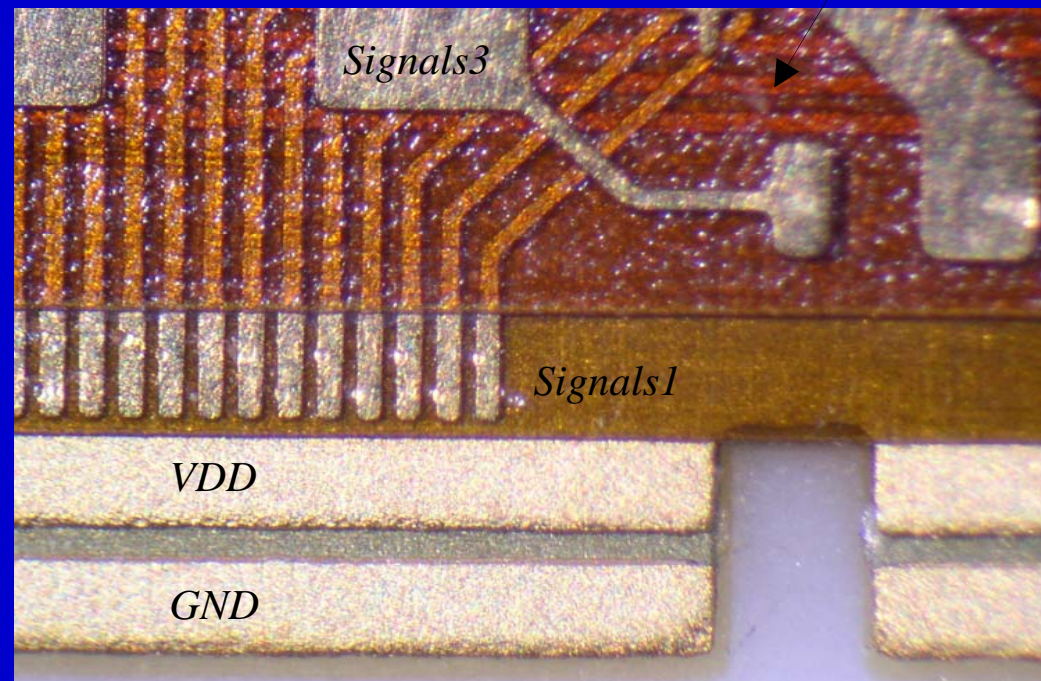
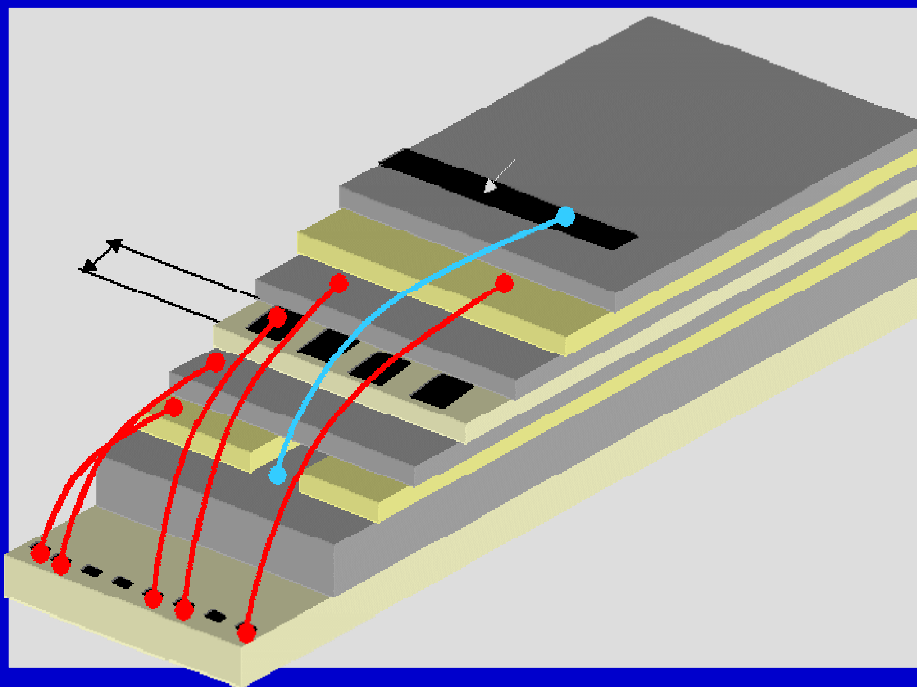
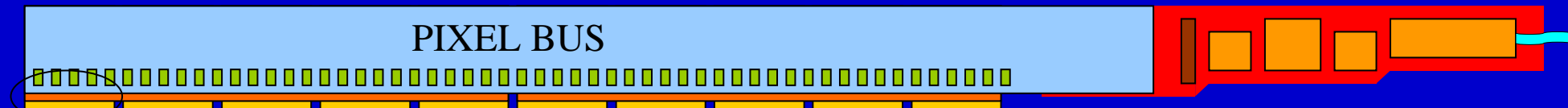
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The Bus

HOW?

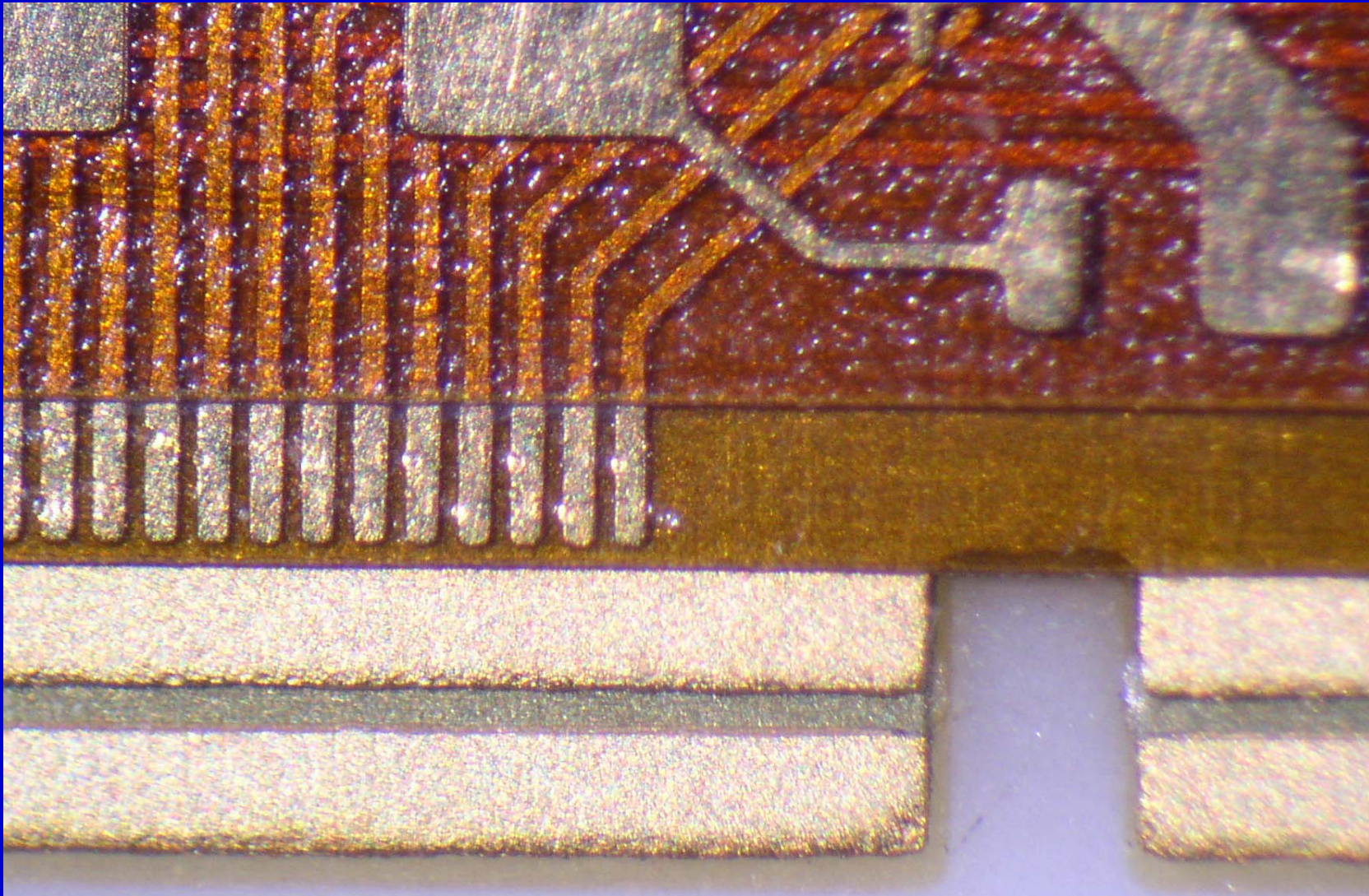
MCM

PIXEL BUS



5 layer Al/Cu bus

HOW?

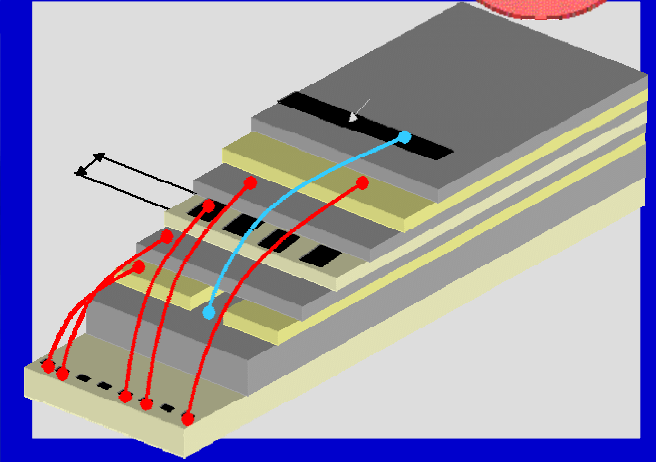
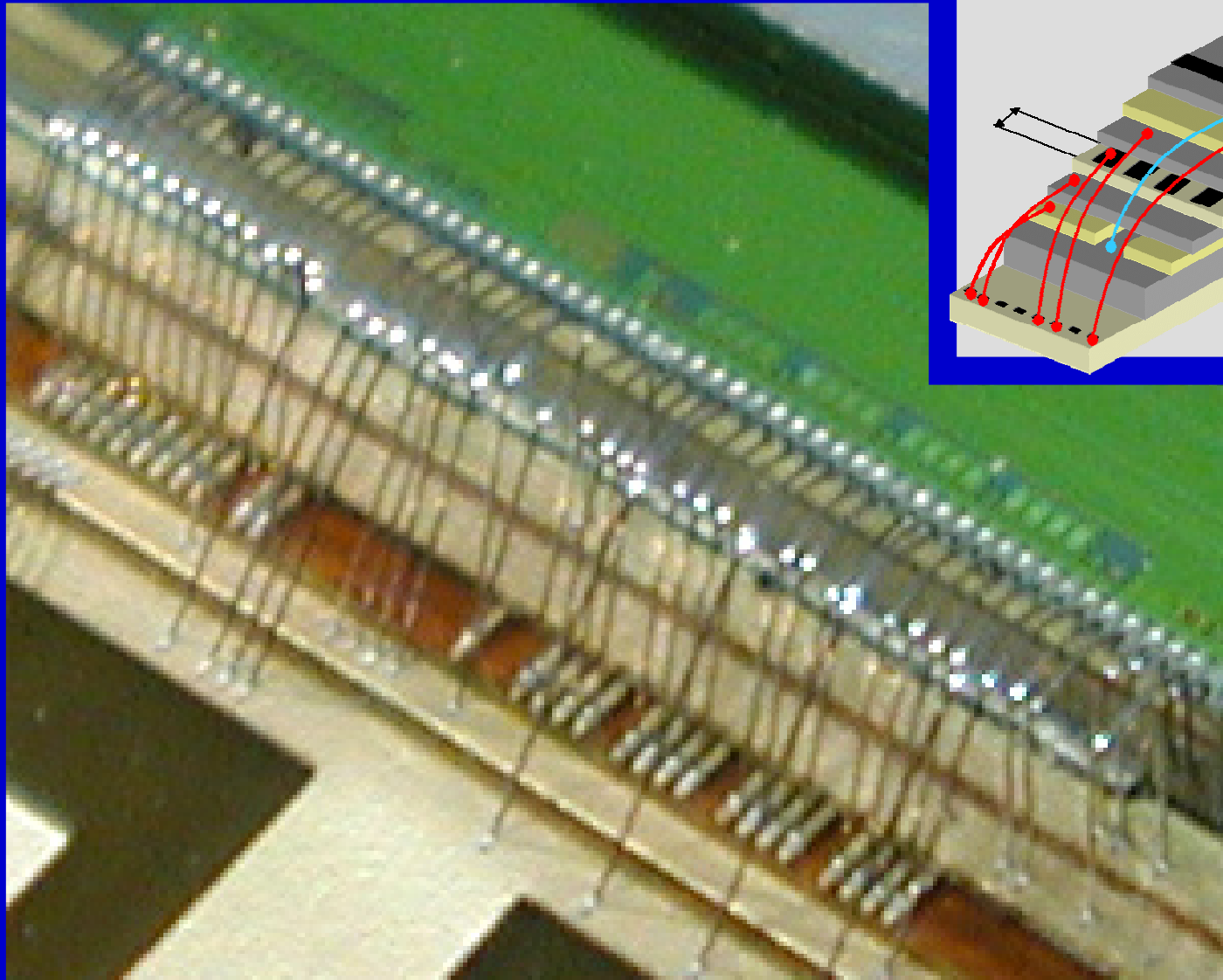


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Bonds on stairs

HOW?



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Challenge

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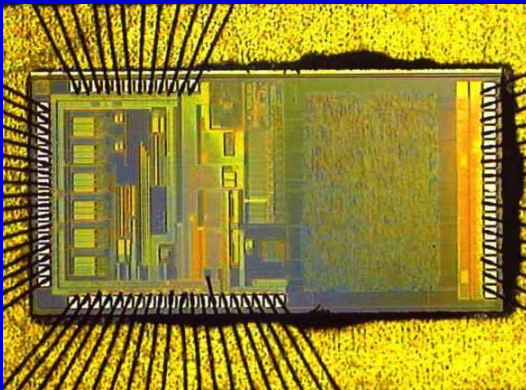
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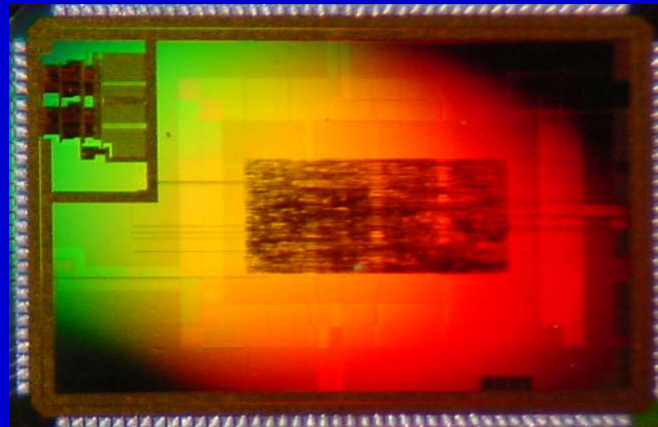
ASICs

HOW?

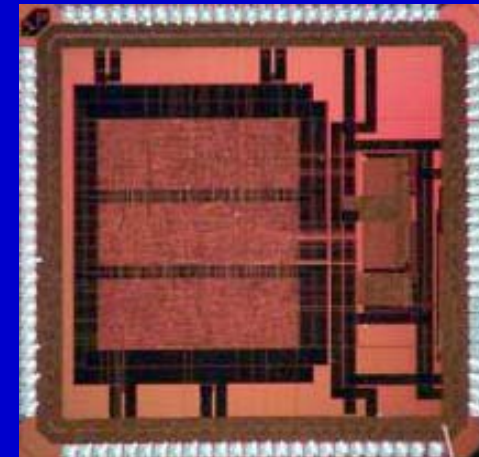
ANAPIL1



Digital Pilot1

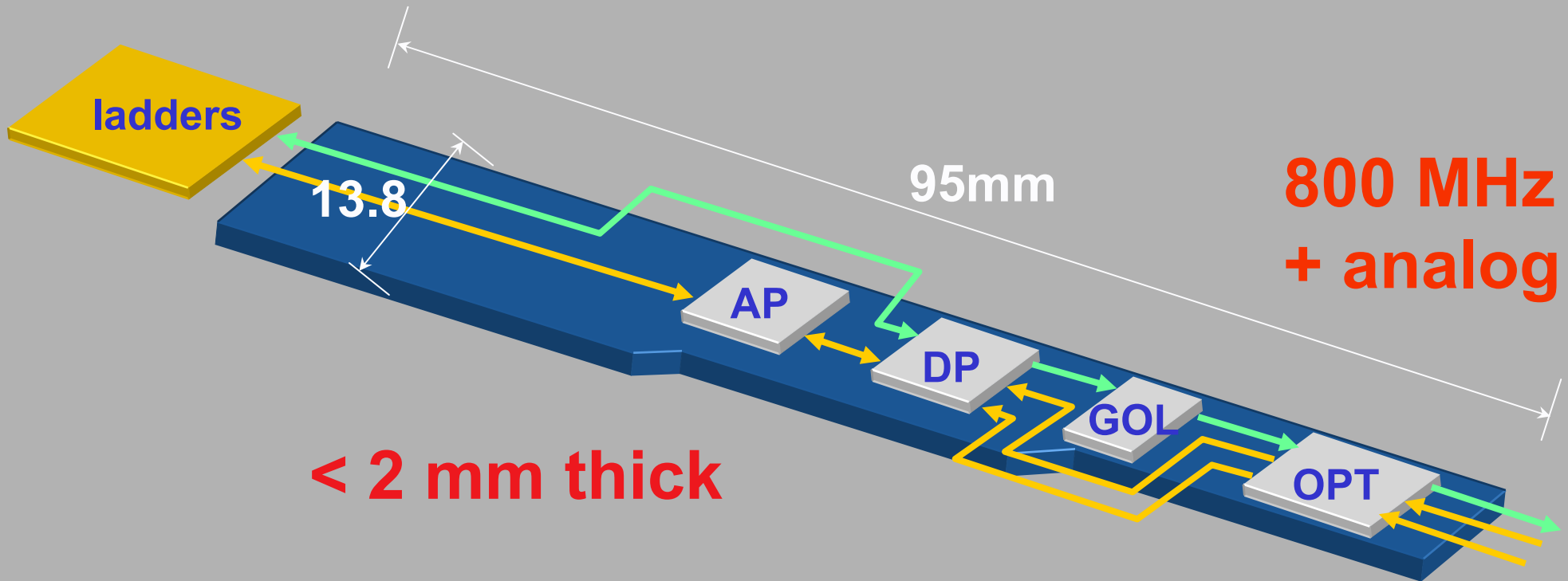


GOL



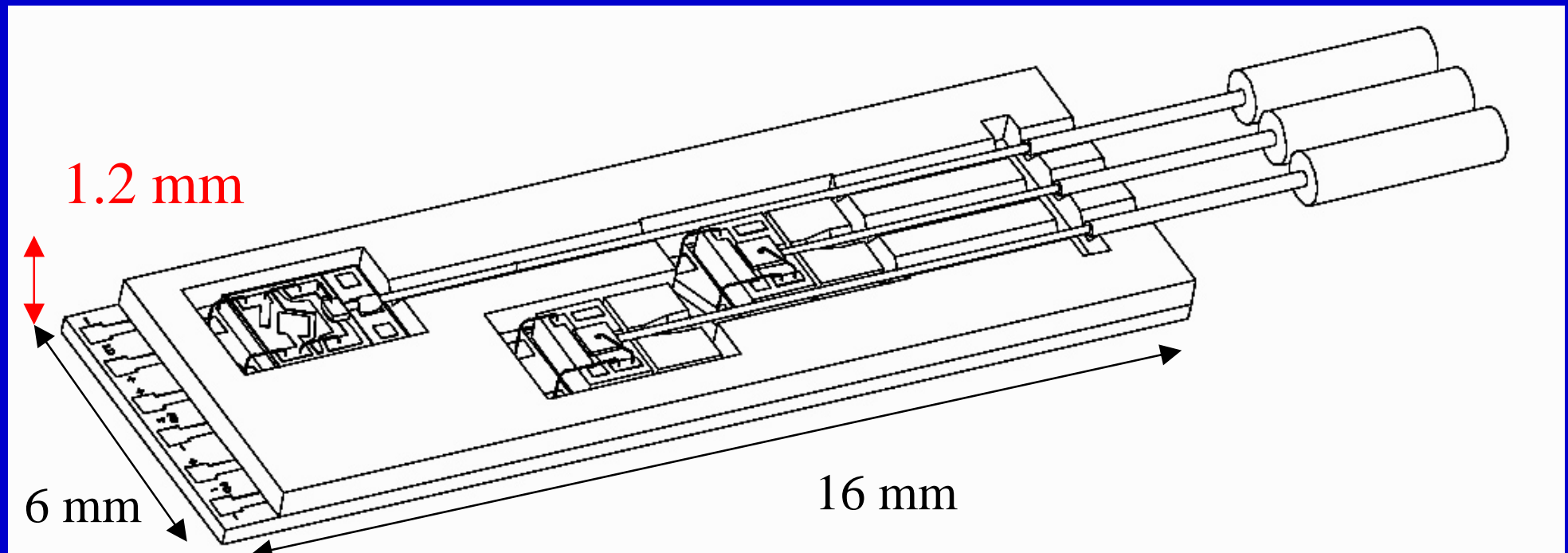
MCM

HOW?



MCM Optical package

HOW?

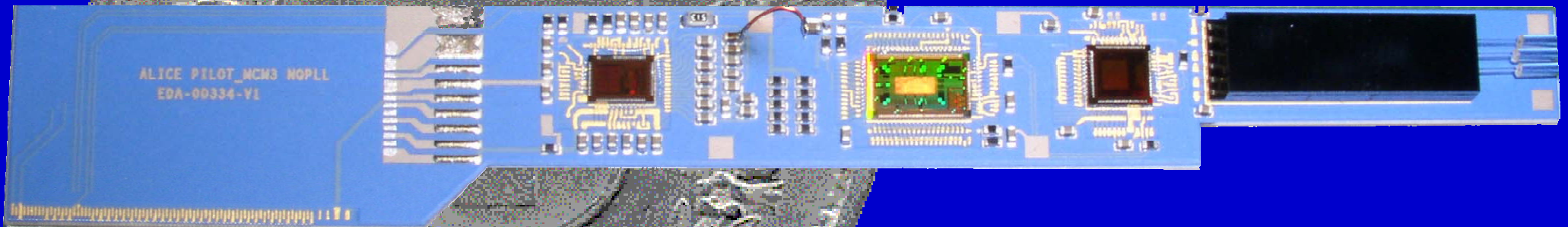


MCM

HOW?

No Copper connections

No data processing, no memory



Analog (10mV) + digital (800MHz) Small quantity

Dense

Fragile: thin, no packages

Small: no probing, limited reworking

Picture of OPT

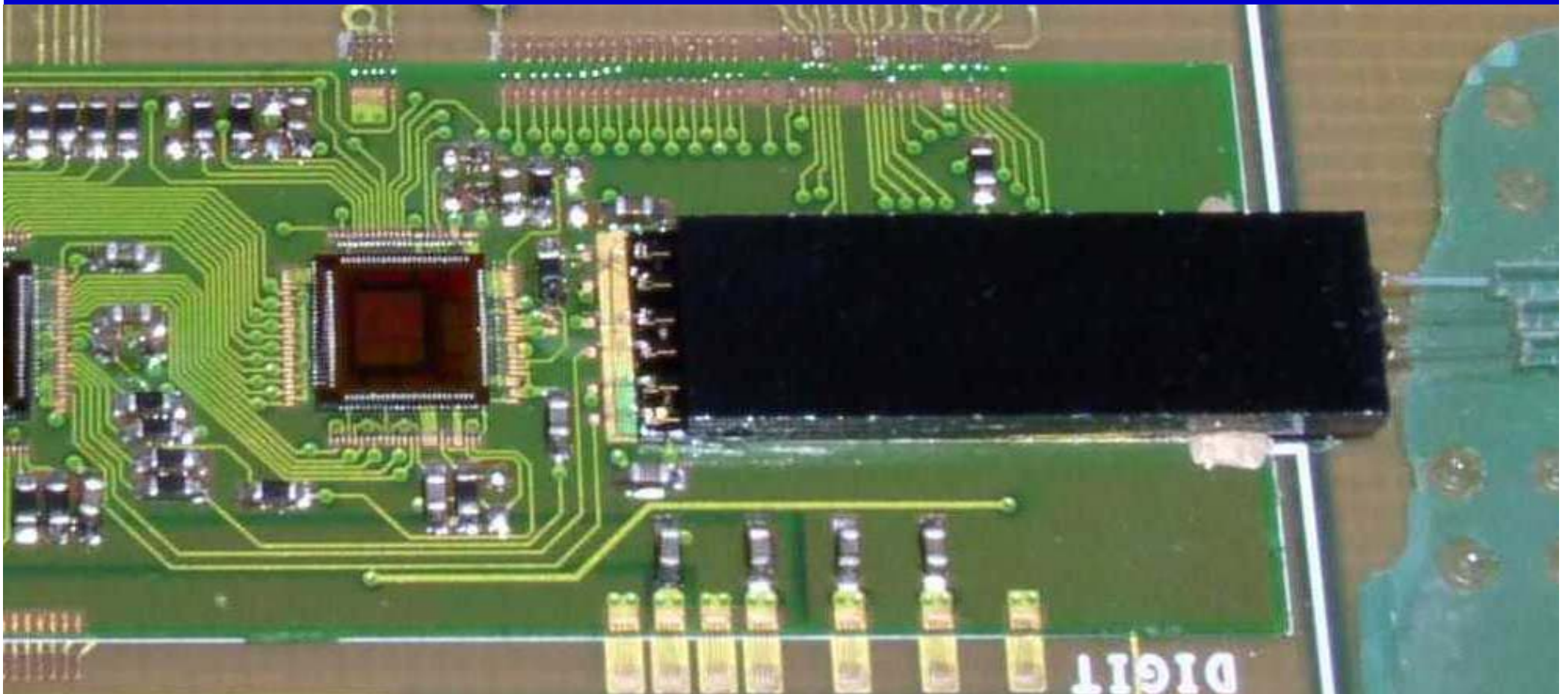
HOW?

Successfully tested

Difficult to produce

Custom designed

Difficult to handle



Challenge

WHY?

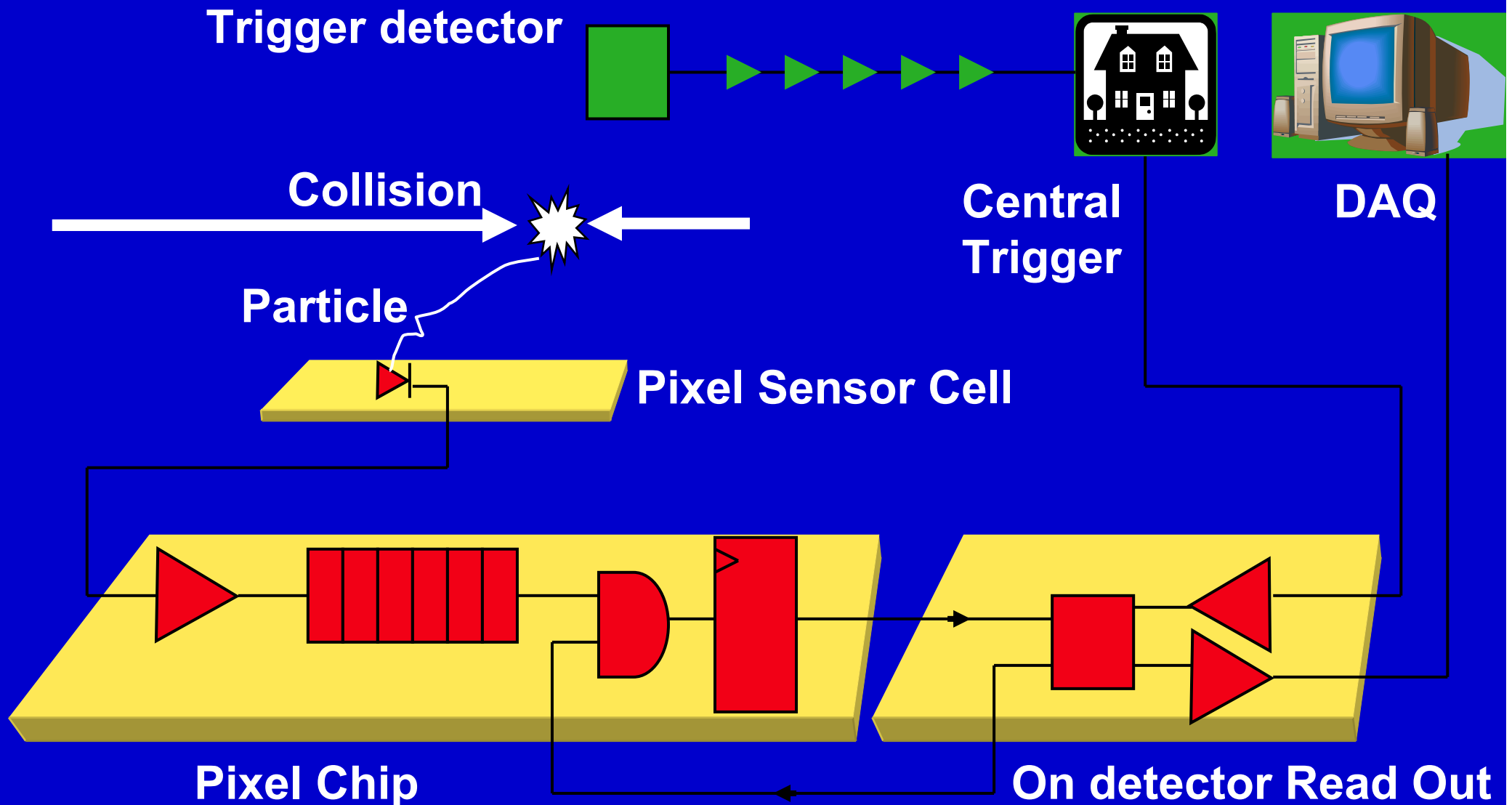
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 - L1 trigger decision
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- Final application environment can only be simulated

The only attack of THE block diagram



What are we building?

WHAT?

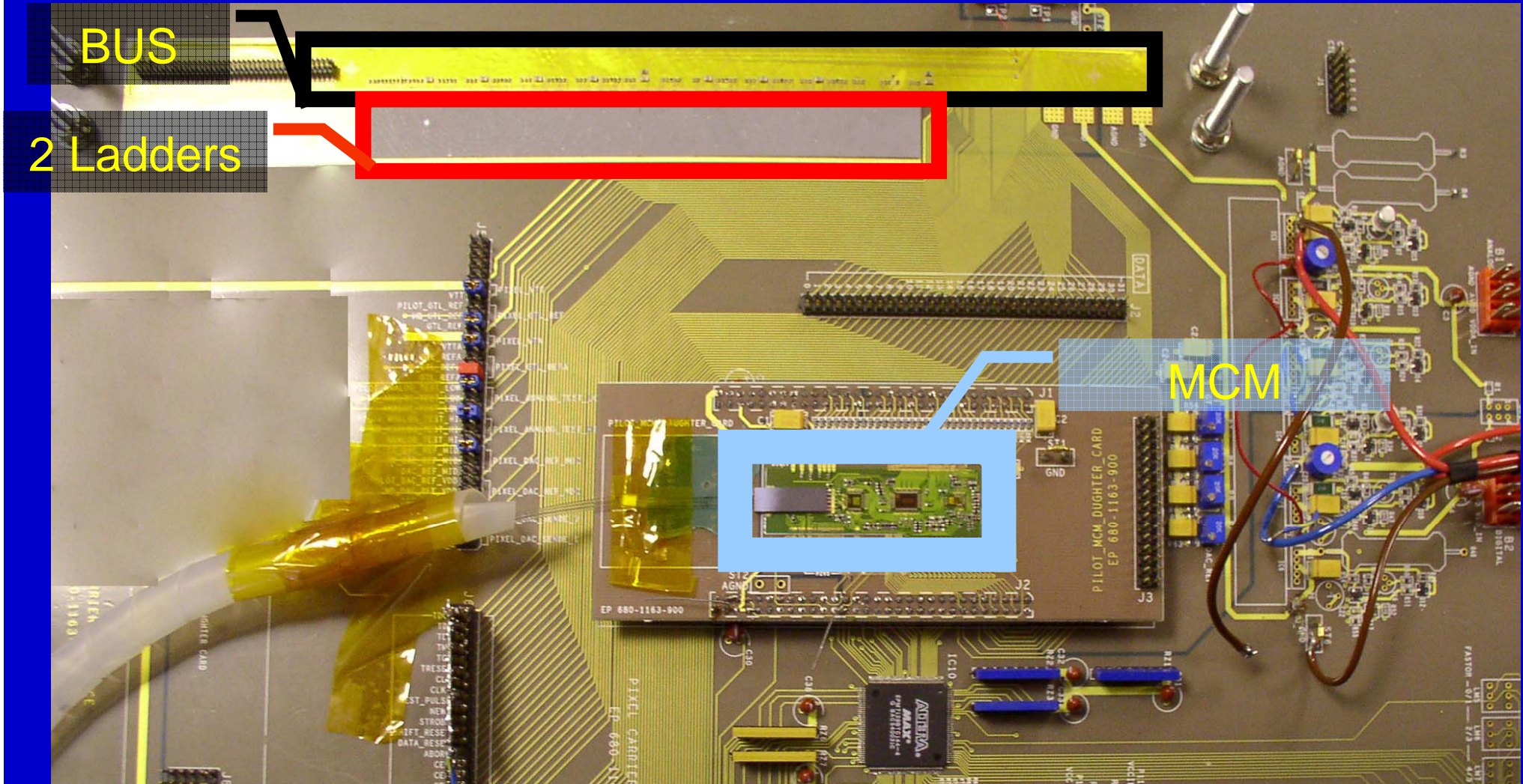


Challenge

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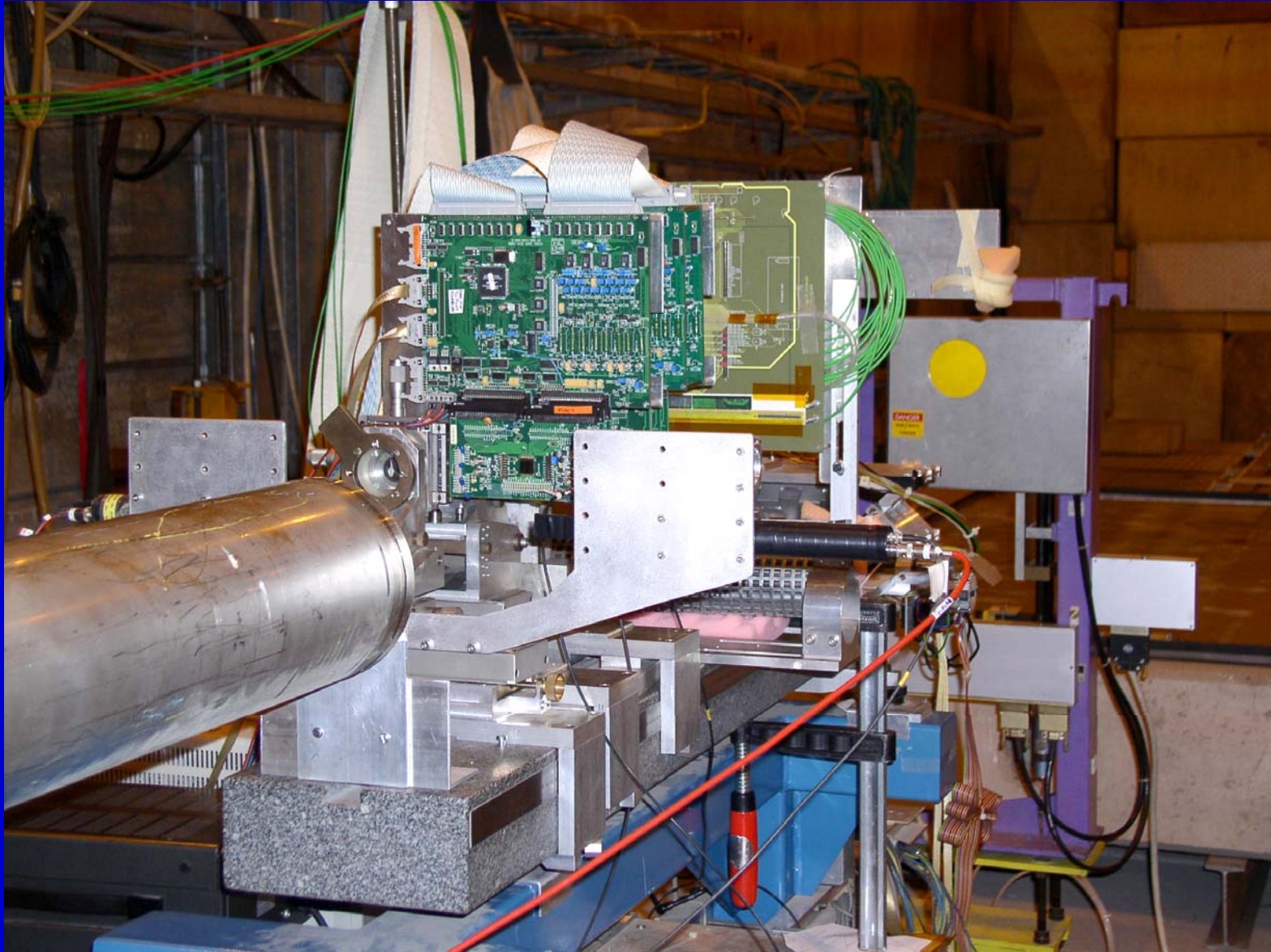
MCM and 2 ladders on bus



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First test beam correlation

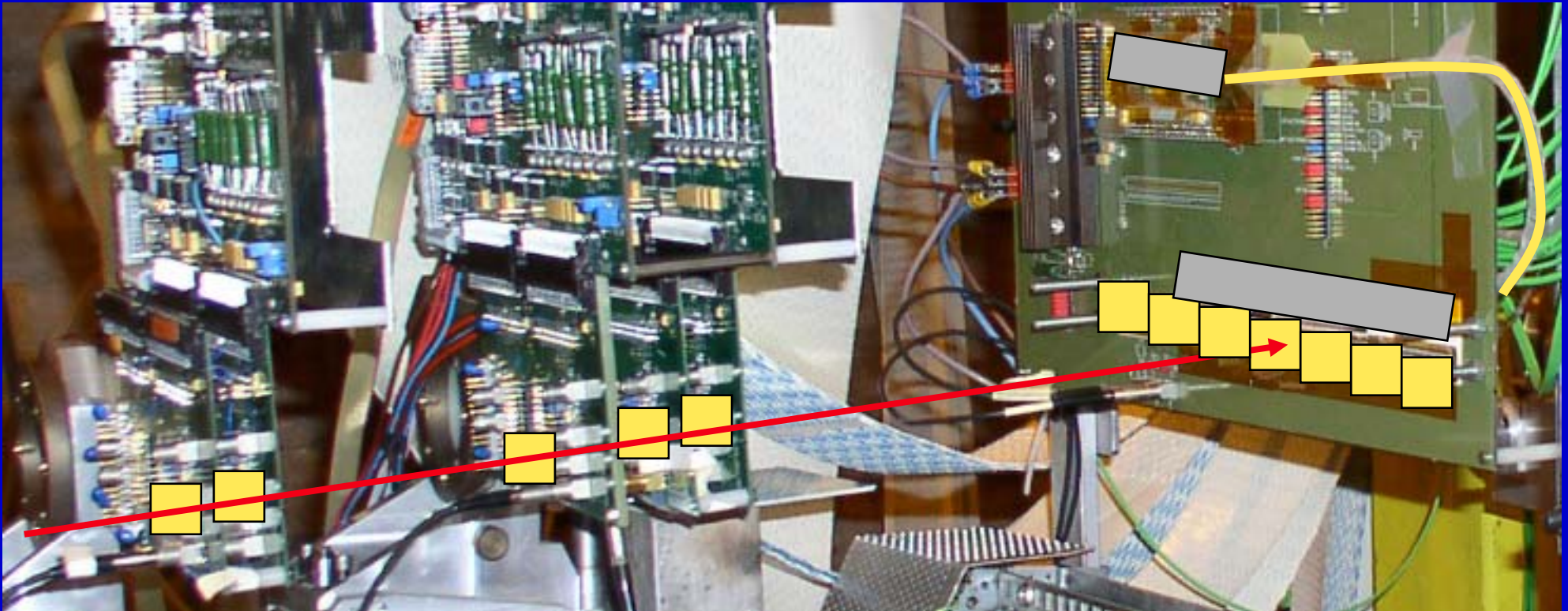


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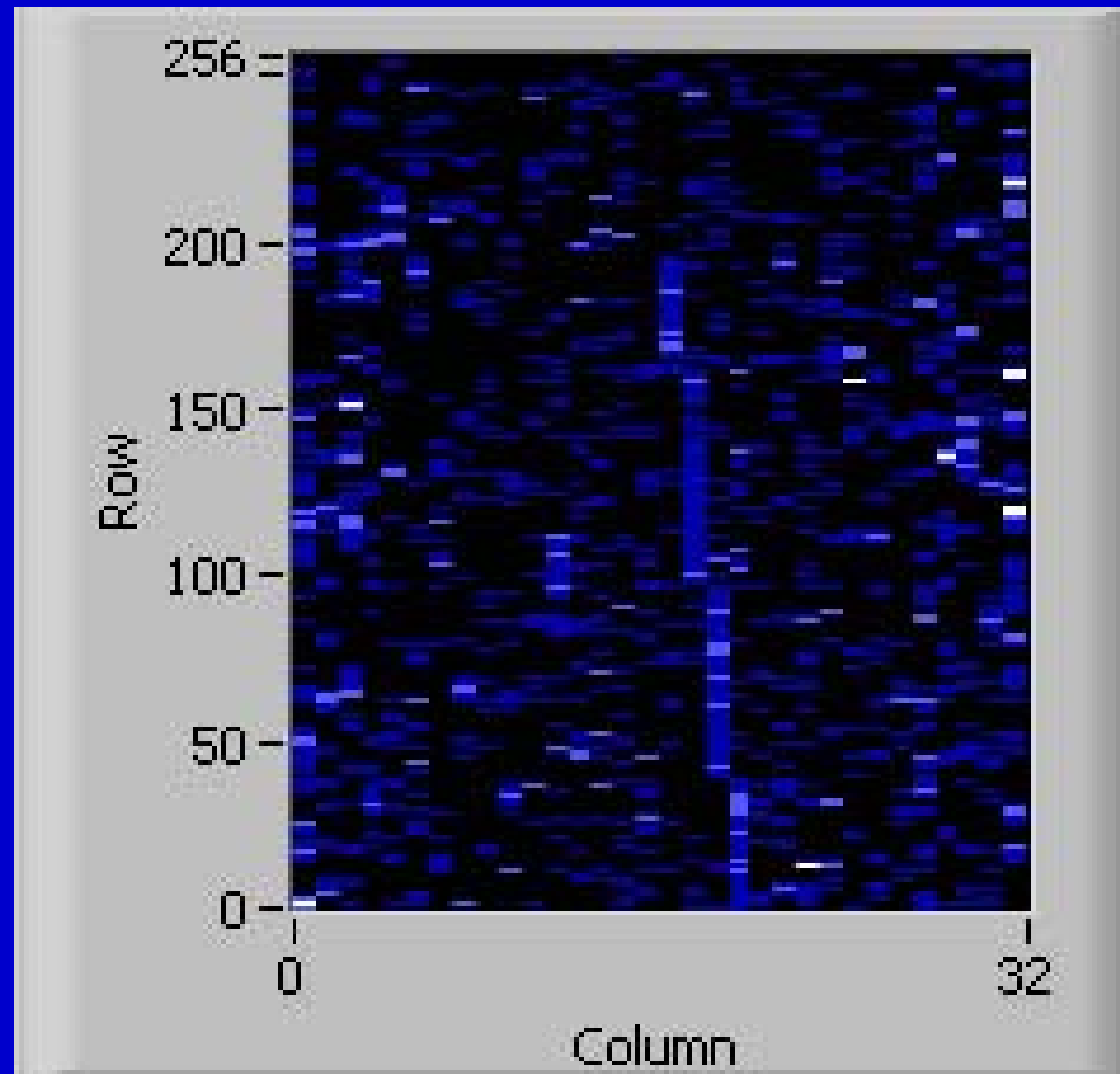
Test beam

HOW?



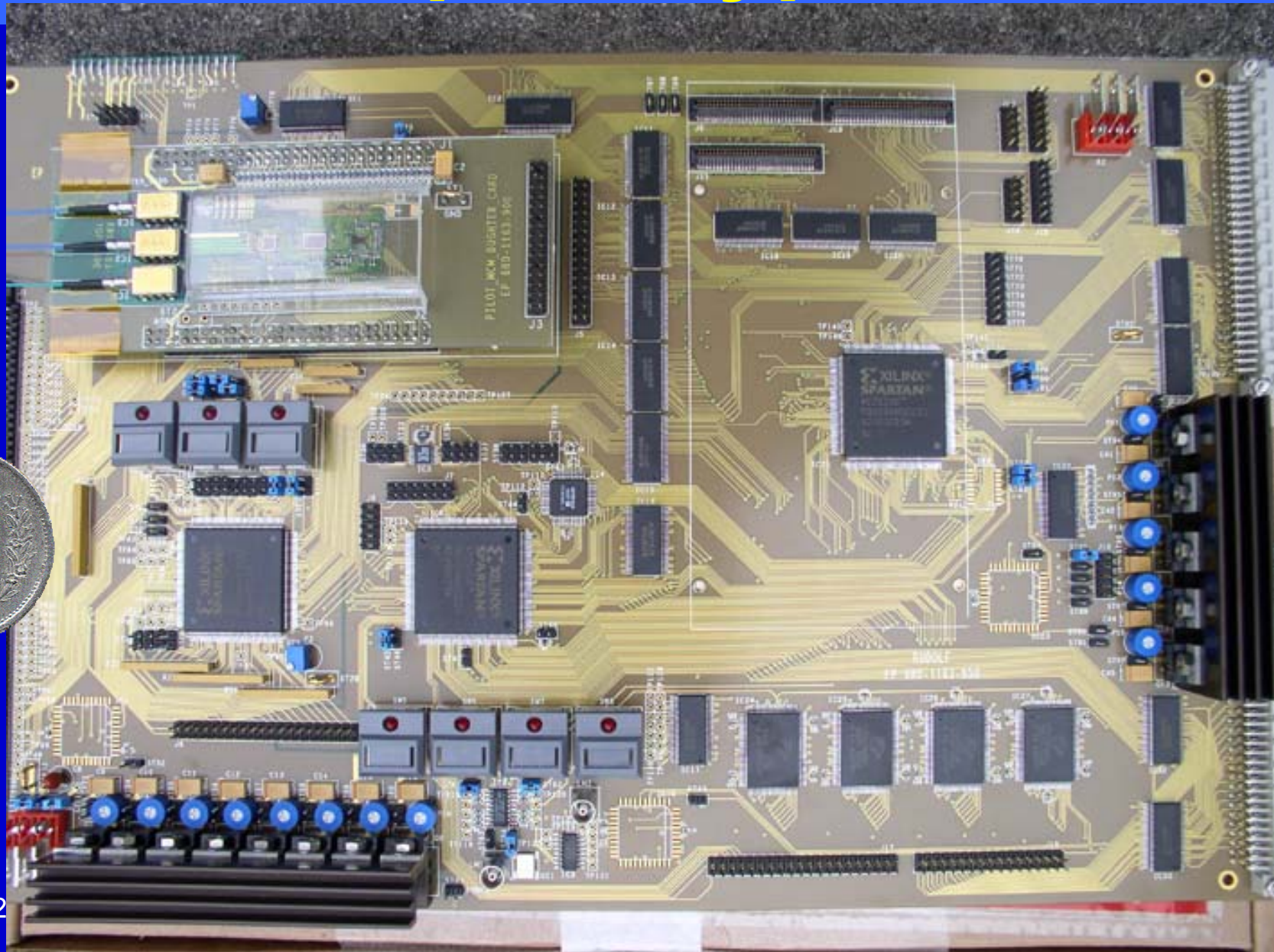
Test beam

HOW?



Router prototype Rudolf

HOW?

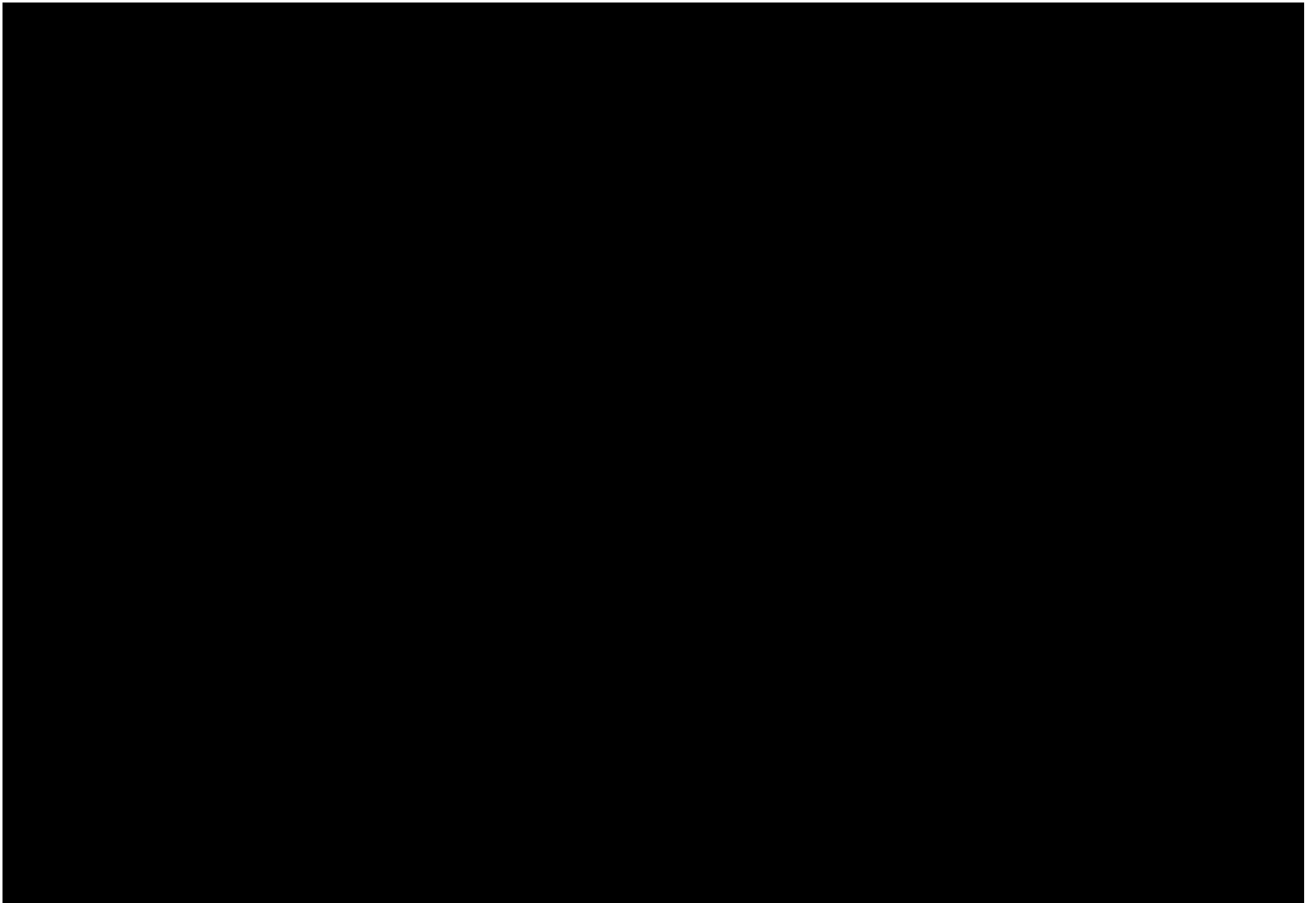


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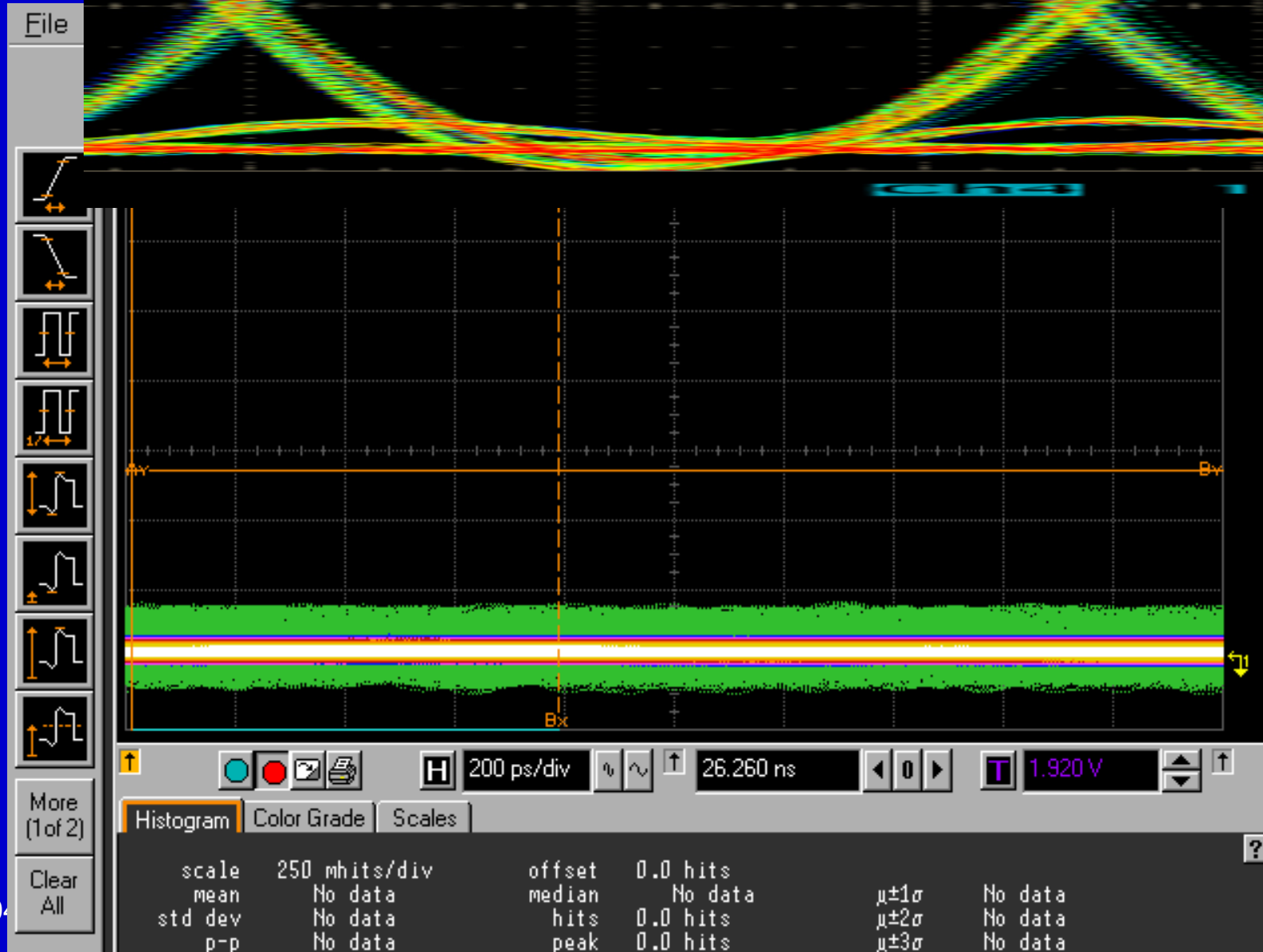
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Conclusion

- **New technologies applied in Research Phase**
 - Detector developments
 - Micro electronics
 - Micro cabling
 - Fiber optics
- **Prototypes successful**



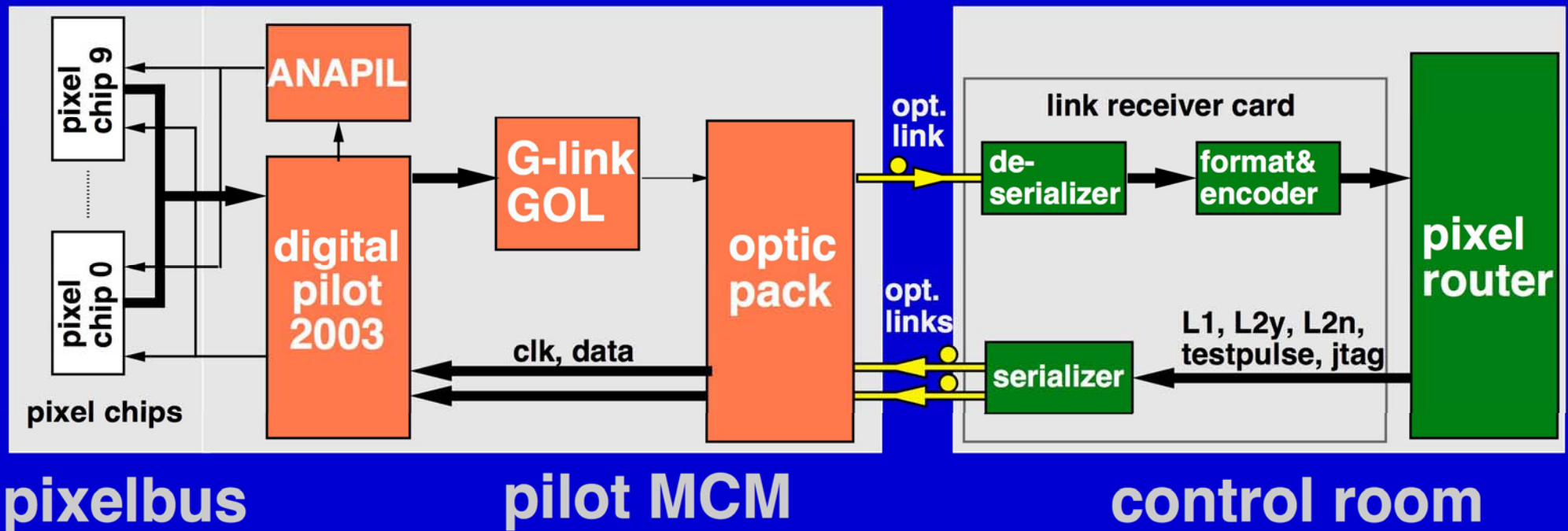
XILINX VIRTEX II 840 Mb/s LVDS



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Pixel read out system



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6 mm

Digital Pilot chip

HOW?

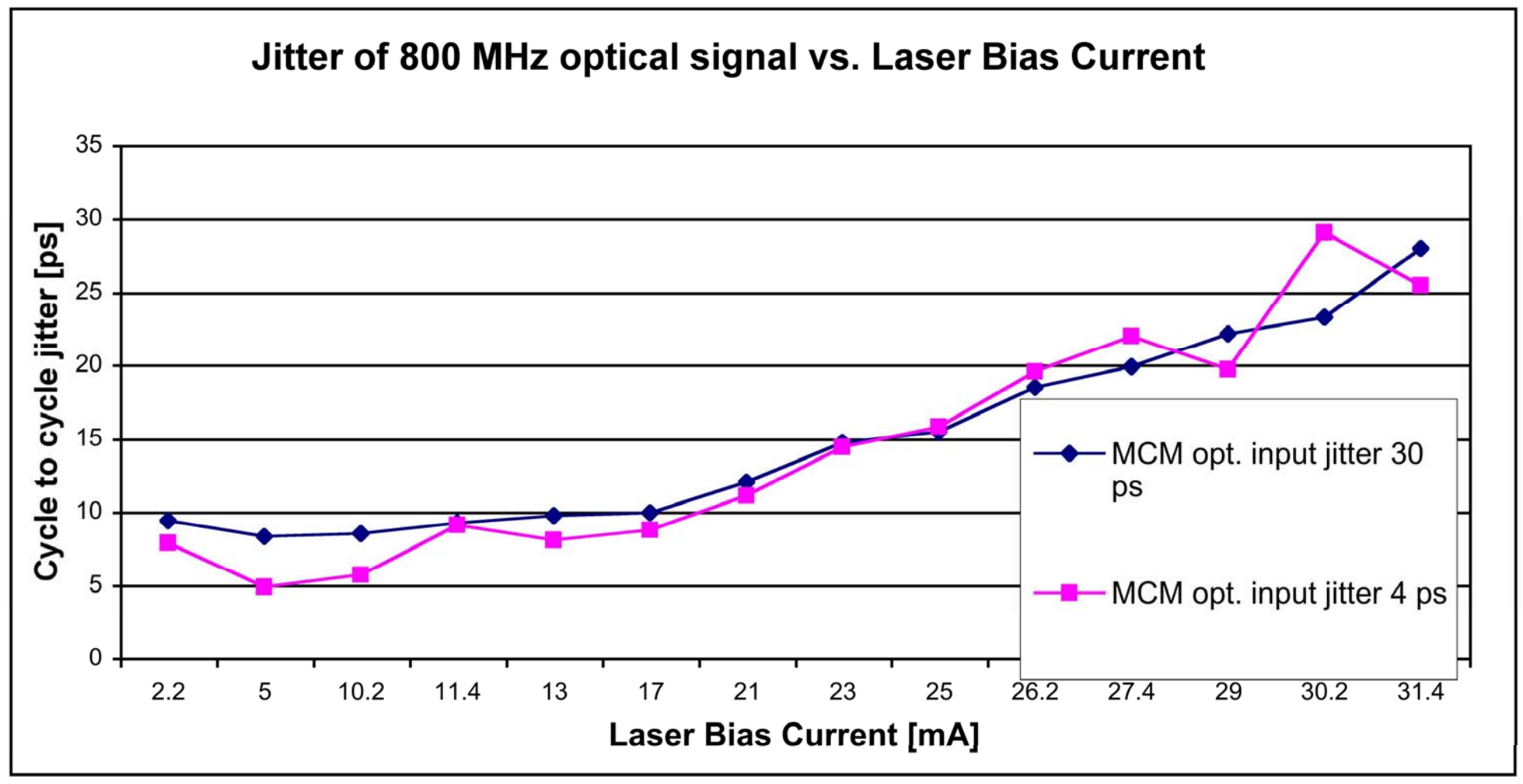
4 mm

136 pins/9000 gates

No memory -> SEU!

Architecture ->
reprogrammable
functionality in control
room

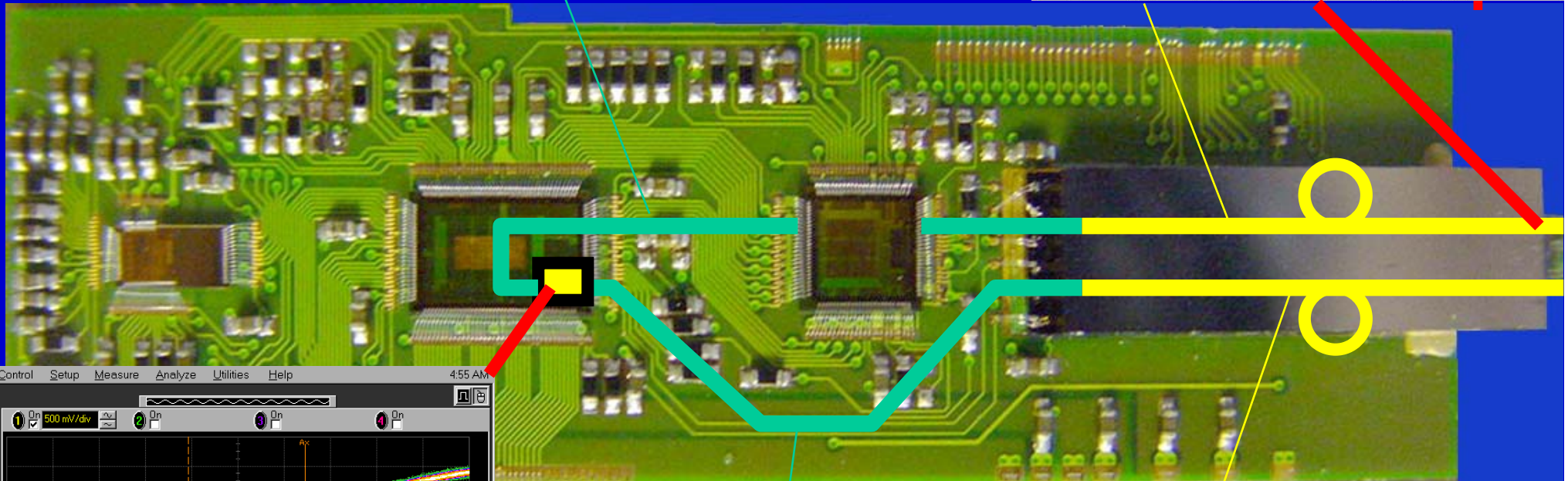
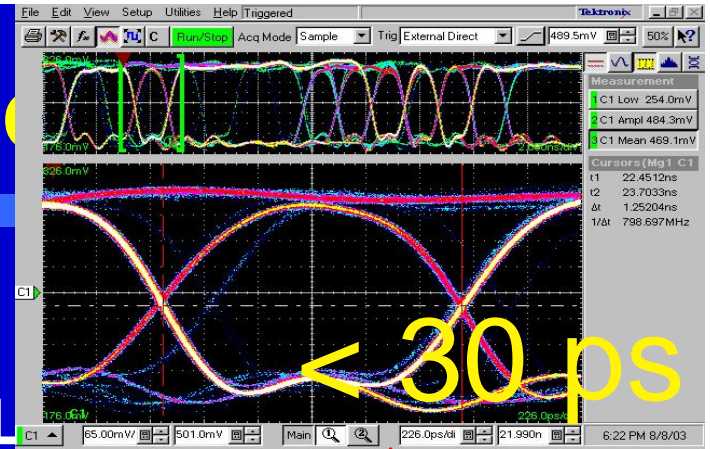
Jitter after transmission



MCM Functional test and

Jitter after PILOT **23 ps**

Jitter after GOL



Optical clk jitter < 10 ps
Jitter after PIN < ? ps

