Radiation-Hard ASICs for Optical Data Transmission in the ATLAS Pixel Detector

Amir Rahimi
The Ohio State University

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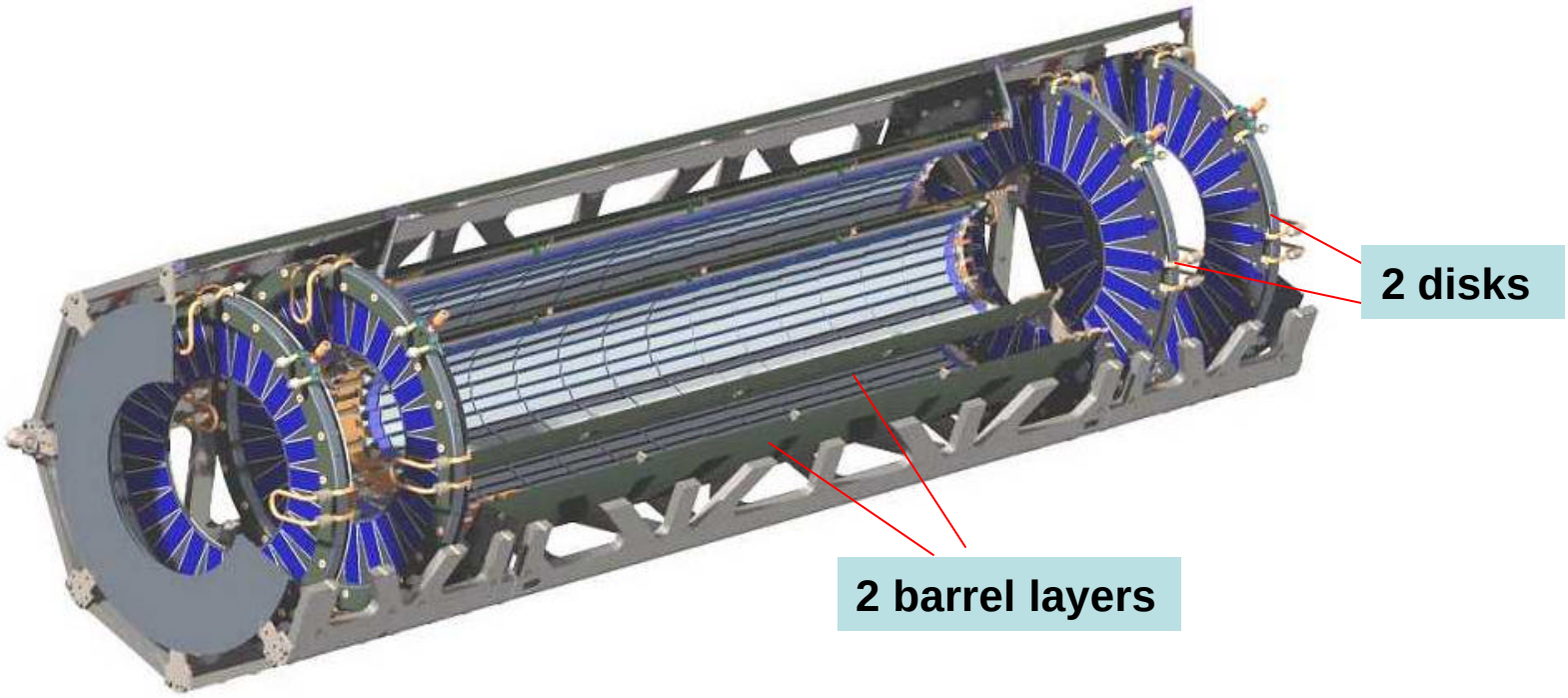
K.E. Arms, K.K. Gan, M. Johnson, H. Kagan, R. Kass, A. Rahimi,
C. Rush, S. Smith, R. Ter-Antonian, M.M. Zoeller
The Ohio State University

A. Ciliox, M. Holder, S. Nderitu, M. Ziolkowski
Universitaet Siegen, Germany

Outline

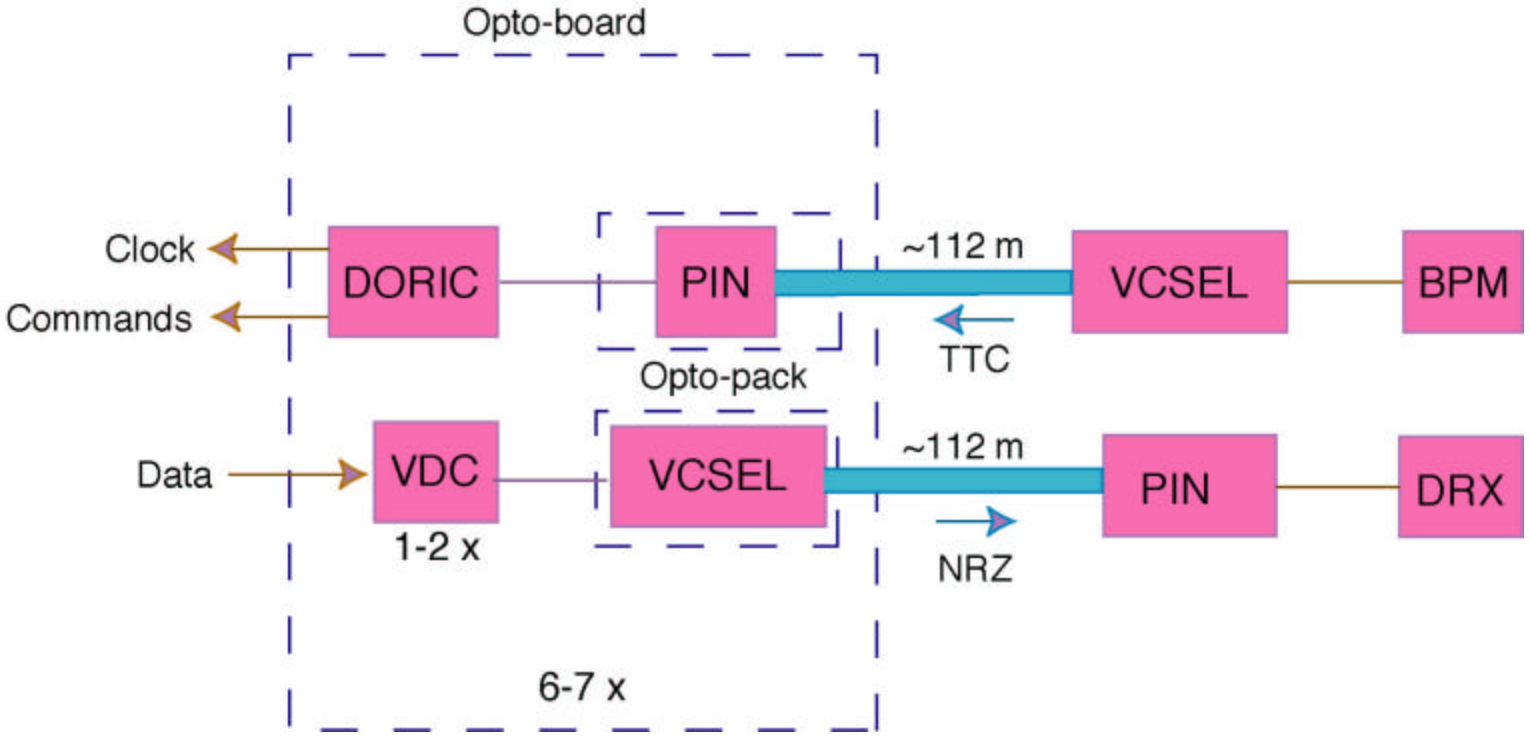
- Introduction
- ASIC description
- Opto-board prototype results
- Proton irradiation results
- Summary

ATLAS Pixel Detector



- Inner most charged particle tracking
- Pixel size 50μm by 400 μm
- Over 100 million sensors
- Barrel layers at r = 5.1 and 12.3 cm
- Disks at z = 50 and 65 cm
- Dosage after 10 years:
  - optical link 30 Mrad or 6 x 10^{14} 1-MeV n_{eq}/cm^2

ATLAS Pixel Opto-link



VCSEL: **V**ertical **C**avity **S**urface **E**mitting **L**aser diode

VDC: **V**CSEL **D**river **C**ircuit

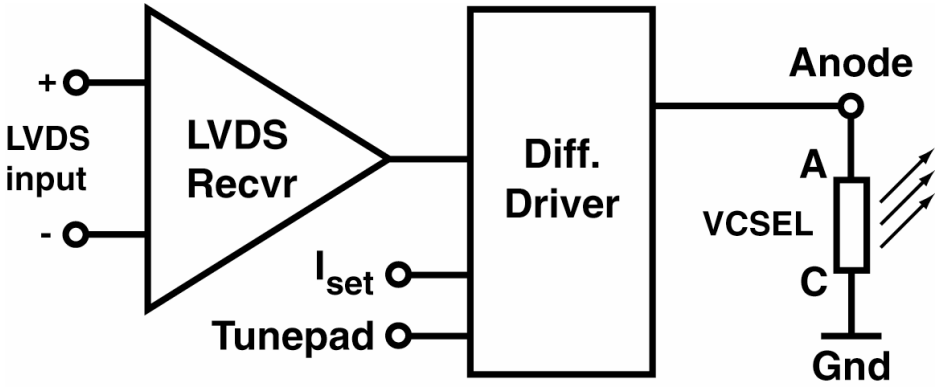
PIN: **PiN** diode

DORIC: **D**igital **O**ptical **R**eceiver **I**ntegrated **C**ircuit

Opto-board: Holds VDCs, DORICs, PINs, VCSELS

VCSEL Driver Circuit Specs

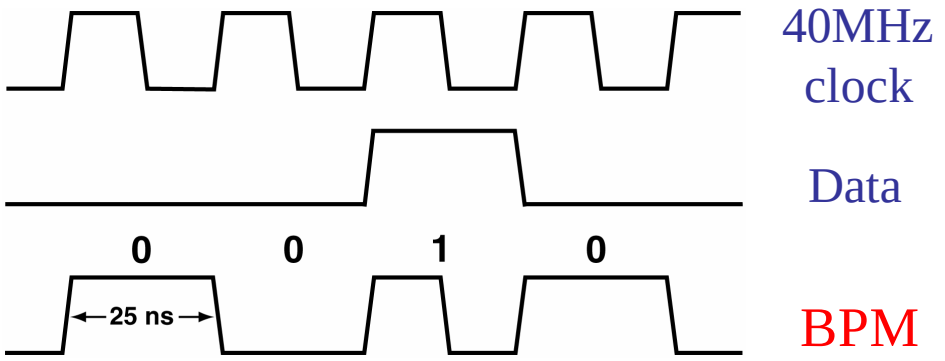
- Convert LVDS input signal into single-ended signal appropriate to drive the VCSEL diode
- Output (bright) current: 0 to 20 mA, controlled by externally controlled current I_{set}
- Standing (dim) current: ~ 1 mA for fast off-to-on switching of VCSEL
- Rise & fall times: 1 ns nominal (40 MHz signals)

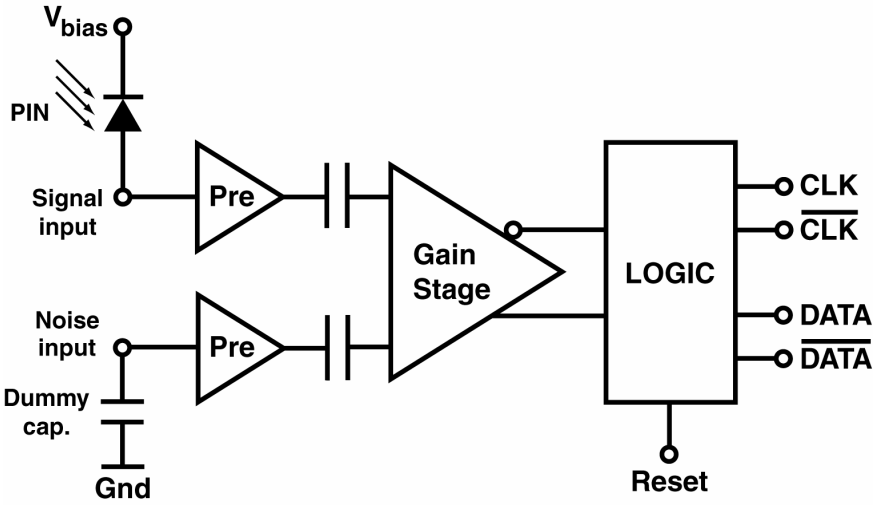


- Duty cycle: (50 ± 4)%
- "On" voltage of VCSEL: up to 2.3 V at 20 mA for 2.5 V supply
- Constant current consumption balanced between ON and OFF state
- Current design uses TRUELIGHT "high power oxide" VCSELs

Digital Optical Receiver IC Specs

- Decode Bi-Phase Mark encoded (BPM) clock and command signals from PIN diode
- Input signal step size:
  40 μA to 1000 μA
- Extract 40MHz clock
- Duty cycle: (50 ± 4)%
- Total timing error: < 1ns
- Bit Error Rate (BER):
  $< 10^{-11}$ at end of life
- Compatible with common cathode PIN array





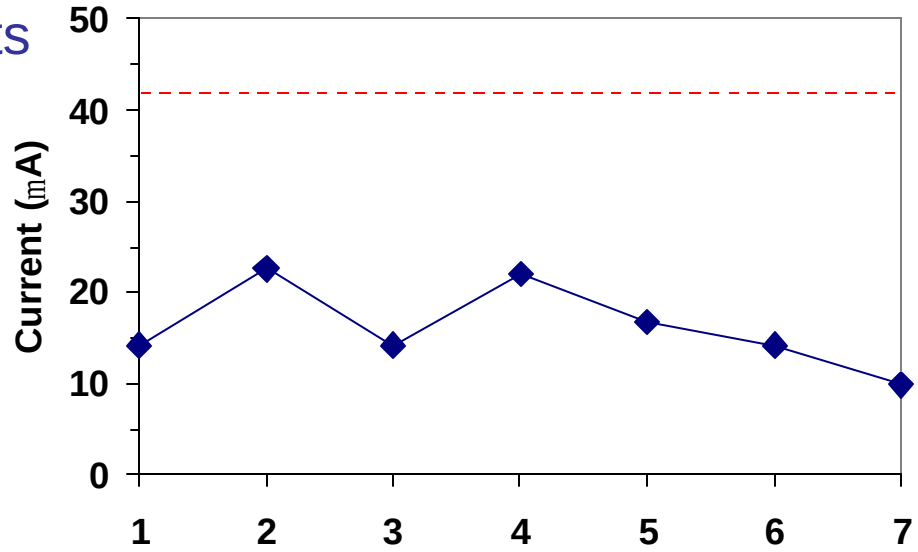
Status of VDC & DORIC

- Original design for ATLAS SemiConductor Tracker (SCT)
  - AMS 0.8 μm BiPolar in radiation tolerant process (4 V)
- DMILL #1-3: Summer 1999 - May 2001
  - 0.8 μm CMOS rad-hard process (3.2 V)
  - VDC & DORIC #3: meet specs
  - severe degradation of circuit performance in April 2001 proton irradiation
- IBM #1-5: Summer 2001 - Dec 2002
  - 0.25 μm CMOS rad-hard process (2.5 V)
  - enclosed layout transistors and guard rings for improved radiation hardness
- IBM 5e: April 2003 engineering run
  - convert 3-layer to 5-layer layout for submission with pixel Module Control Chip (MCC) for cost saving

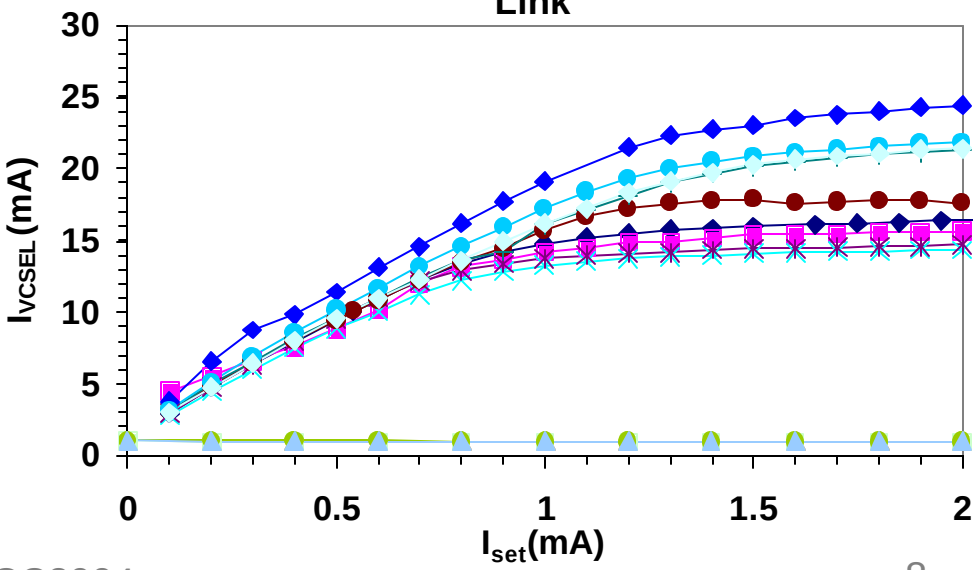
  ⇨ this is the production run since chips meet specs and sufficient quantity of chips were produced

VDC/DORIC-I5e Measurements

- Detailed measurements of electrical parameters including rise/fall times, duty cycle, PIN current thresholds, VCSEL drive current …
- Satisfy all Pixel detector requirements
- DORIC: Minimum PIN current for no bit error significantly better than spec: 40 μA



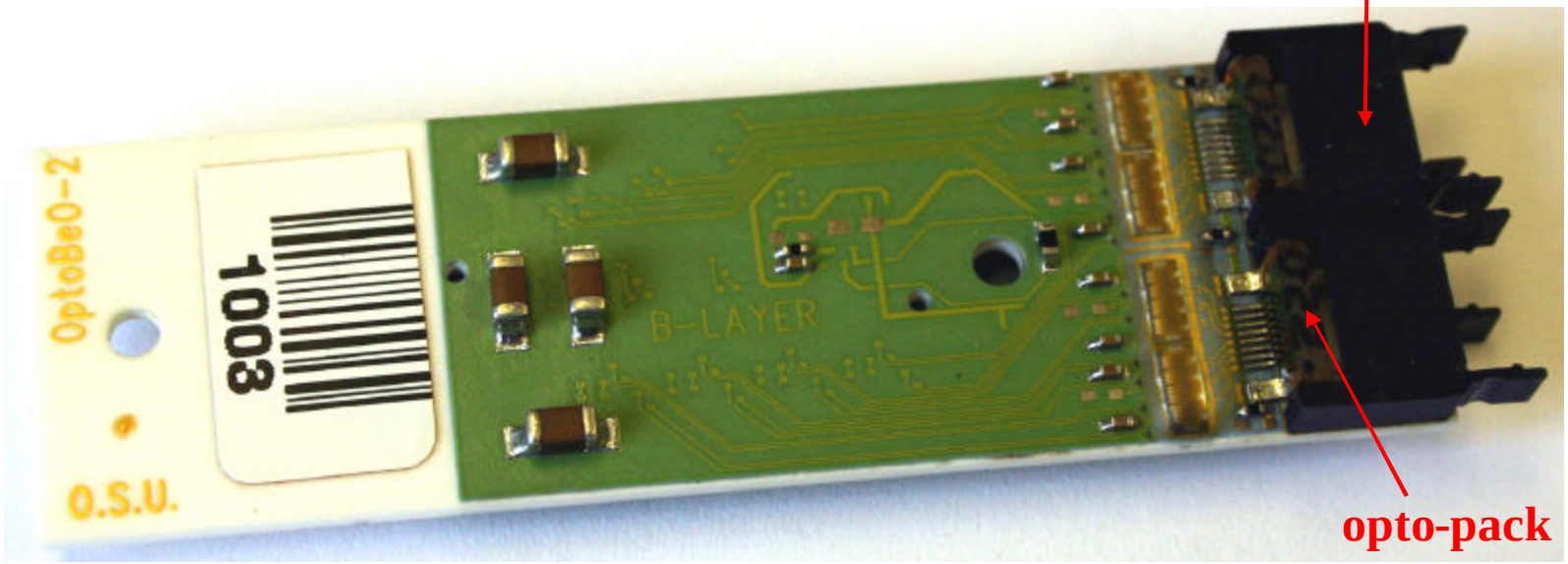
- VDC: dim current is ~ 1 mA as expected
- Bright current saturates ≥ 14 mA.
  - Varies depending on VCSEL V-I characteristics
  - Target is 20 mA, but 14 mA is enough for annealing to recover from irradiation damage

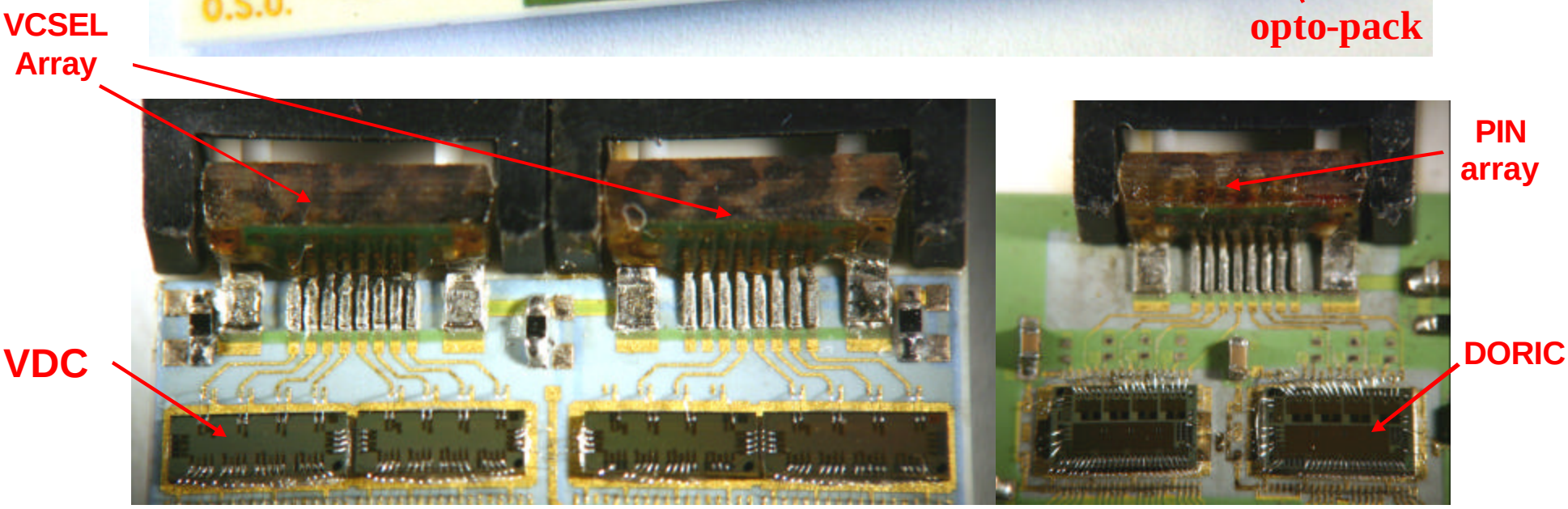


Opto-board

- Converts optical signal ⇔ electrical signal
- Contains seven optical links, each link serving one Pixel module
- Fabricated in two flavors
  - Layer B: for inner barrel, two data link per module to accommodate for high hit occupancy(80 boards)
  - Layer D: for outer barrel and disks 1 and 2 (430 boards)
- Fabricated with BeO for heat management
  - initial prototype with FR4 for fast turn around and cost saving
- 1st BeO prototype
  - Many open vias due to insufficient gold filing by the vendor
  - Opto-links work after via repair
- 2nd BeO prototype
  - Recycled BeO boards with open vias
  - Many shorts due to over filling by the vendor
- 3rd BeO prototype
  - Use more experienced/expensive vendor
  - Produced opto-boards of high quality

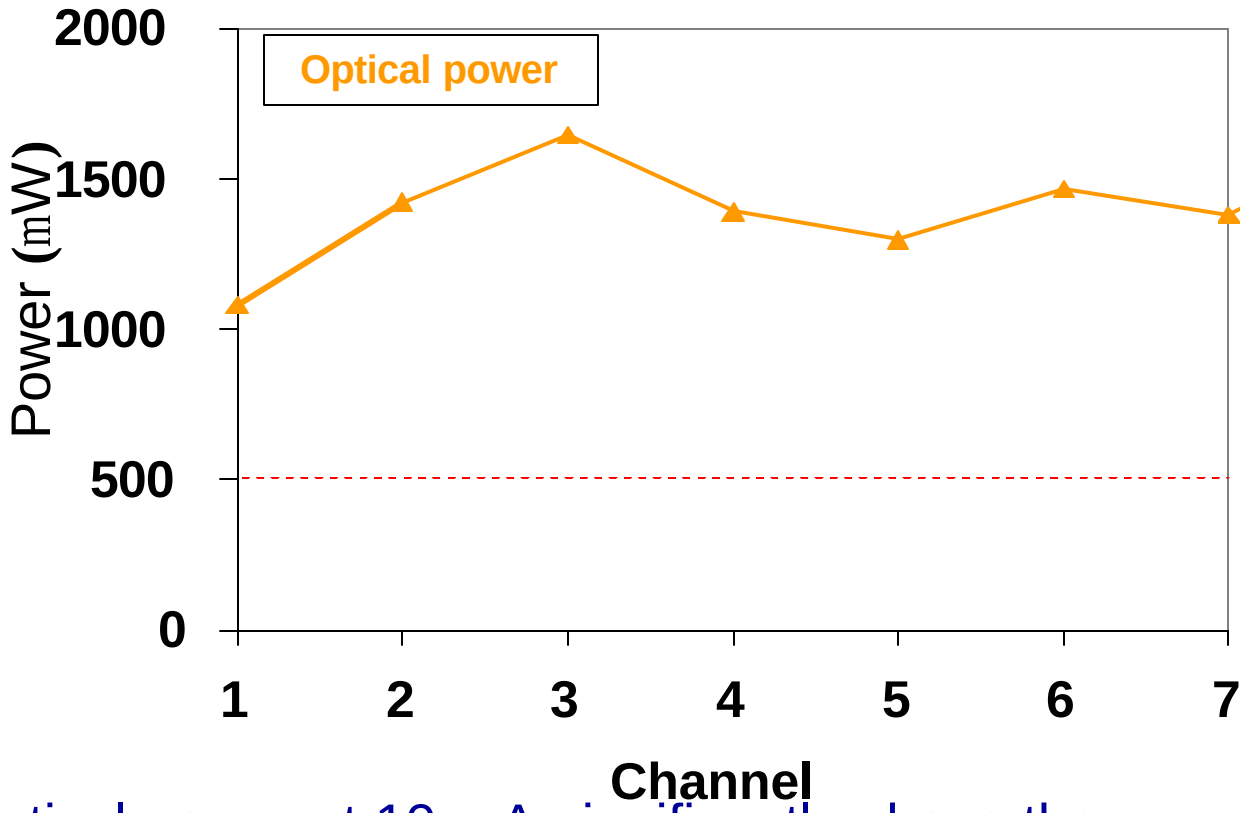
BeO Opto-board





Opto-board Performance

- Detailed measurements are done on all critical electrical and optical parameters to check performance/quality
  - LVDS rise/fall times, jitter…,
  - Optical power, optical rise/fall times, duty cycle…
  - The opto-boards meet or exceed all the pixel detector requirements



- Optical power at 10 mA significantly above the spec

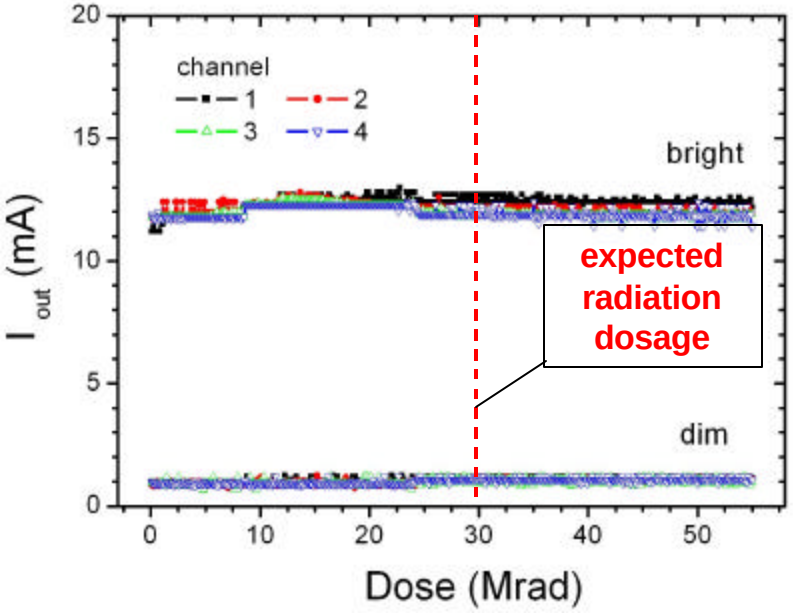
Status of Opto-board

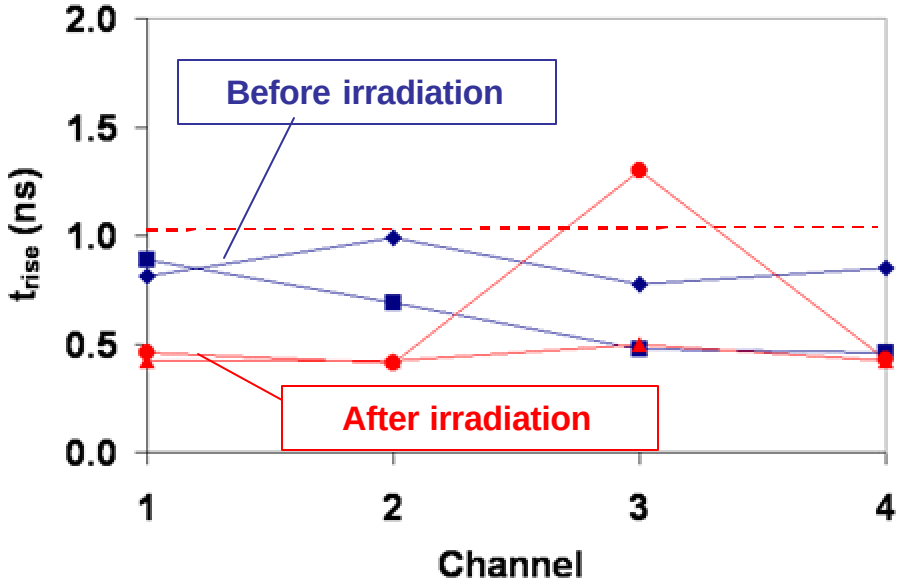
- 28 boards were delivered
  - Equal number of layers B and disks
  - Populated opto-boards have low noise and good optical power
    - no known circuit design error
  - A few SMD's detached from three boards
  - Ordered 80 B-layer opto-boards with layout changes to improve adhesion
    - Expected delivery in September
    - If new opto-boards are satisfactory, produce 430 boards for the outer barrel and disks

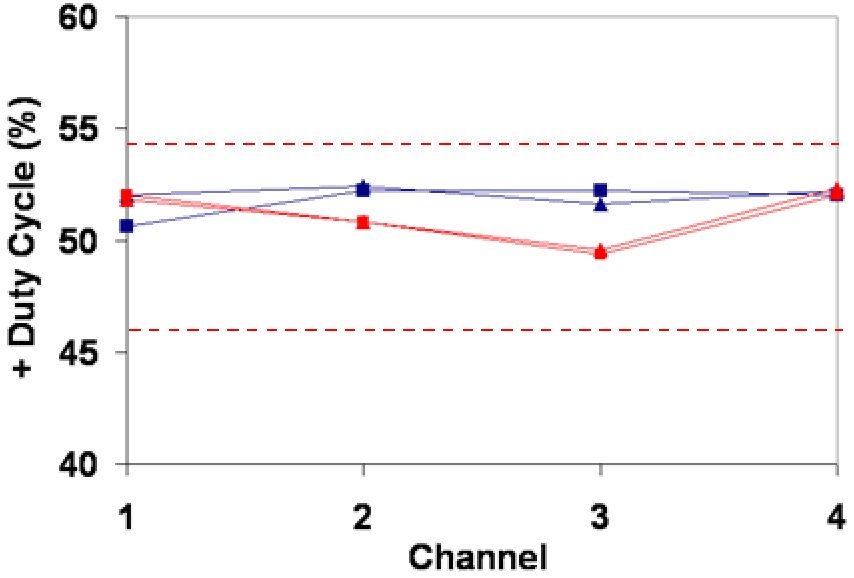
Radiation Hardness Measurements

- Important to measure/certify radiation hardness of ASICs and opto-board and its components:
  - VCSEL and PIN arrays
  - VDC and DORIC chips
  - Encapsulant, fibers, glues, etc.
- Use CERN's T7 beam (24 GeV Proton) for radiation hardness
  - Cold box setup: electrical testing of DORIC and VDC
    - Up to 62 Mrad
  - Shuttle setup: testing of optical links on opto-boards using DORIC and VDC
    - Can be moved in and out of beam remotely for annealing
    - Up to 32 Mrad

VDC Performance

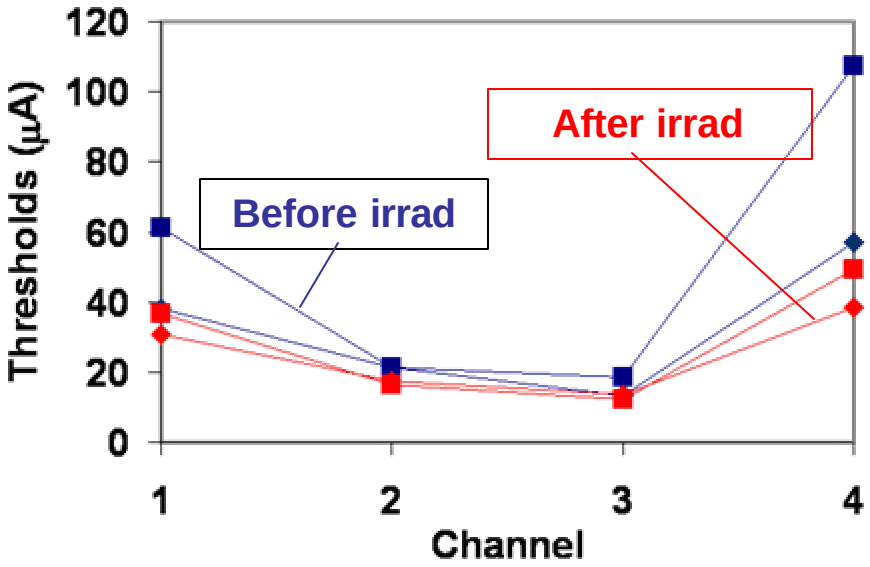


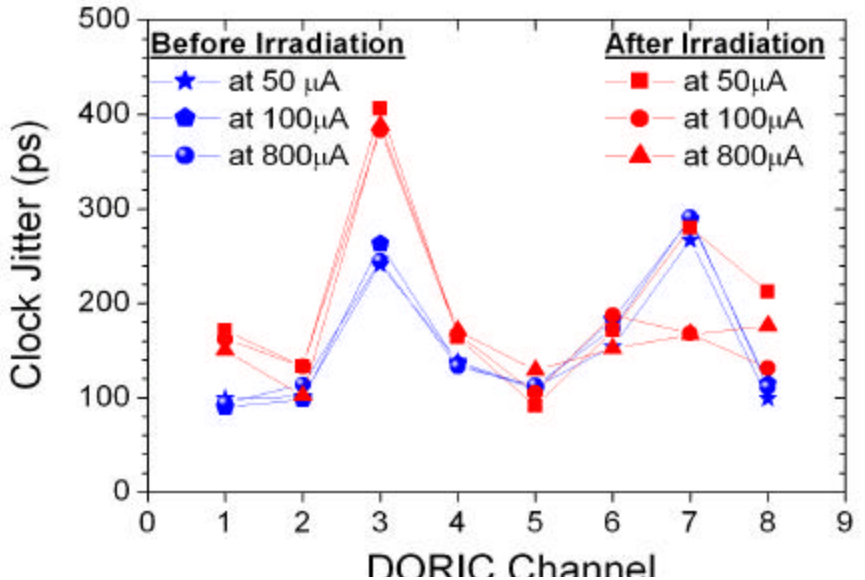




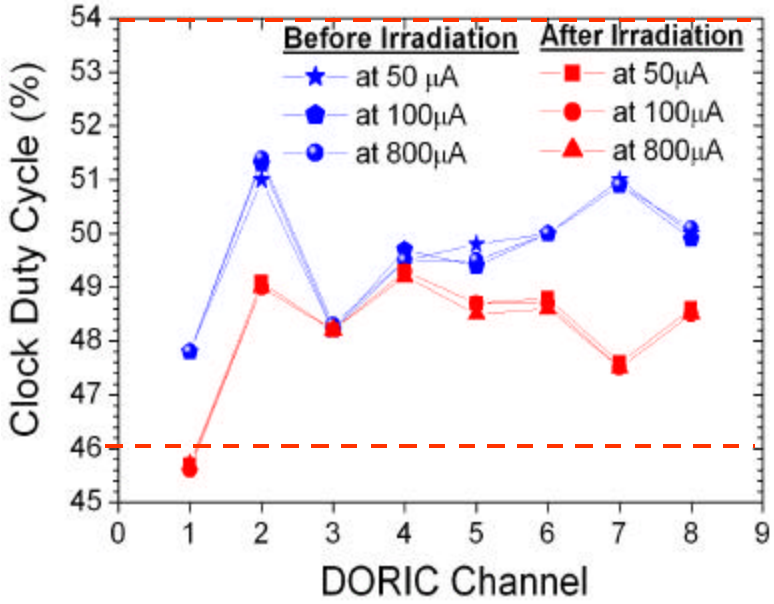
- Current output is constant vs. dosage
- Duty cycle and rise/fall times consistent before and after irradiation
  - Better rise and fall times on the opto-board due to shorter wire bonds and traces

DORIC Performance



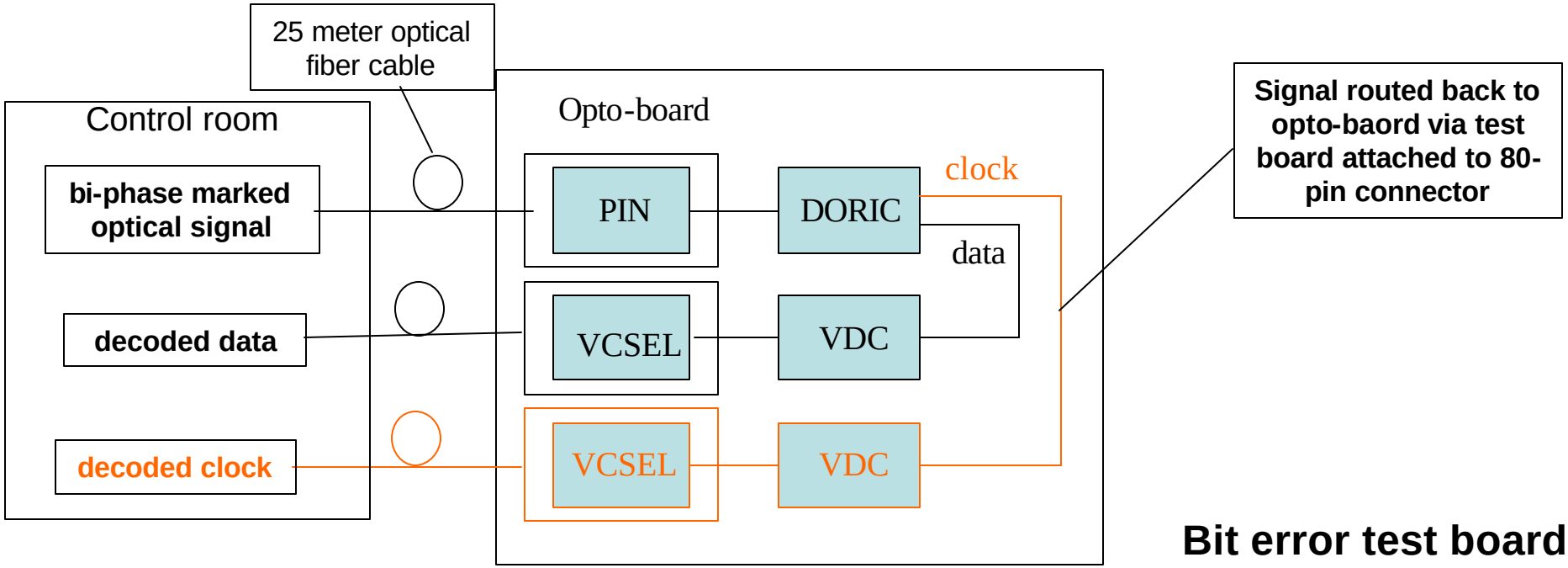


- Threshold for no bit error unchanged after irradiation
- Jitter consistent before and after irradiation
- Clock duty cycle slightly out of spec after irradiation
  - Minimum 45.5% (spec 46%)
- Threshold and duty cycle improve with shorter wire bonds and traces

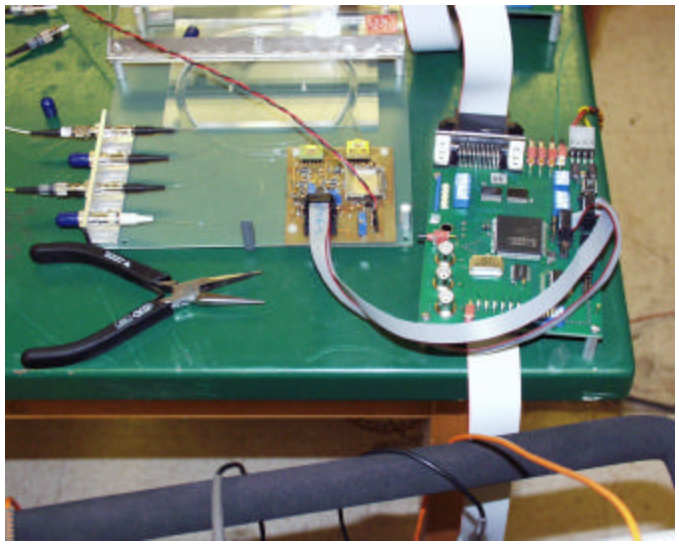


Real Time Monitoring

- Real time testing of opto-board system using loop-back setup



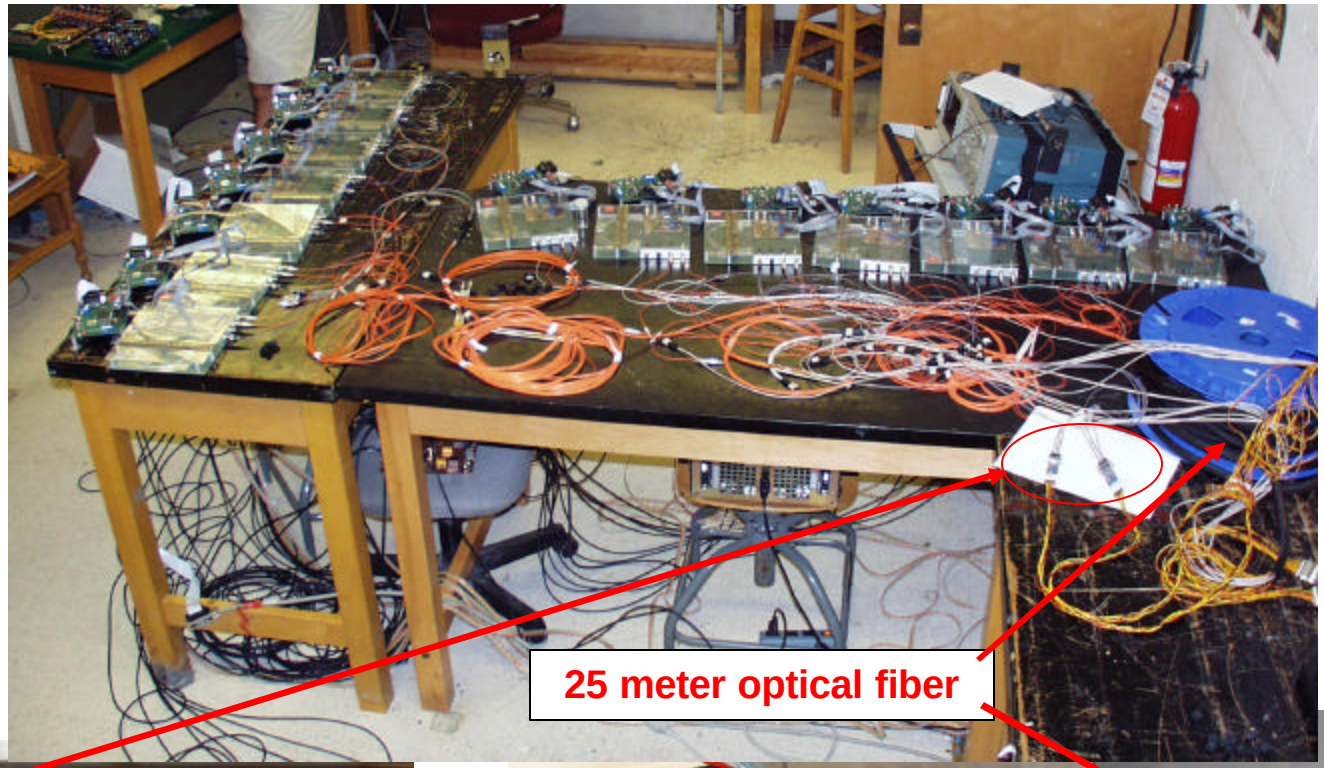
Bit error test board



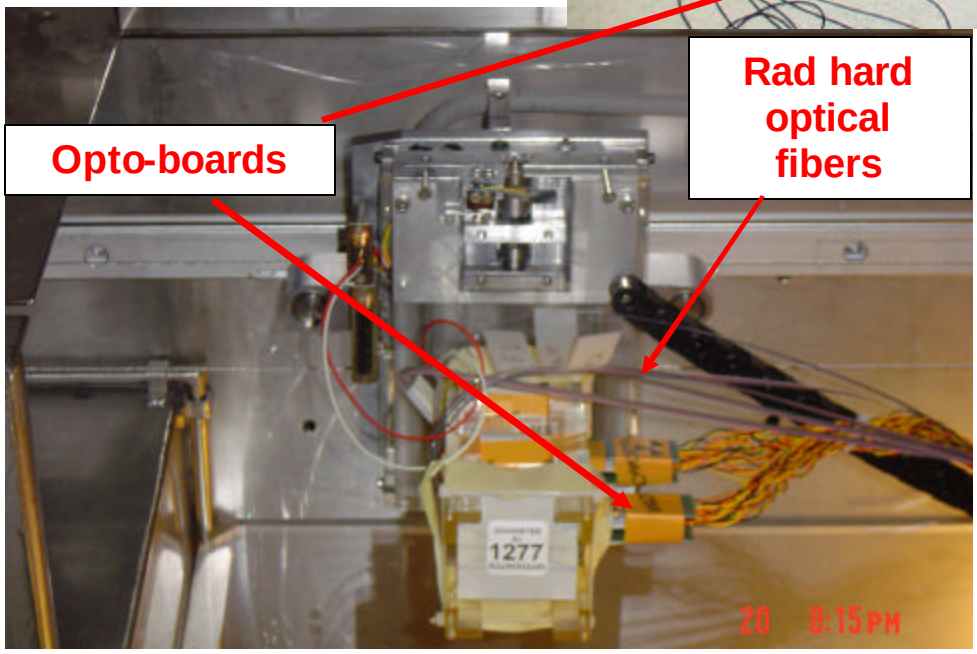
- Compare transmitted and decoded data
  - measure minimum PIN current for no bit errors
- Measure optical power

Setup for Irradiation in Shuttle at CERN

Shuttle test electronics prior to shipping to CERN

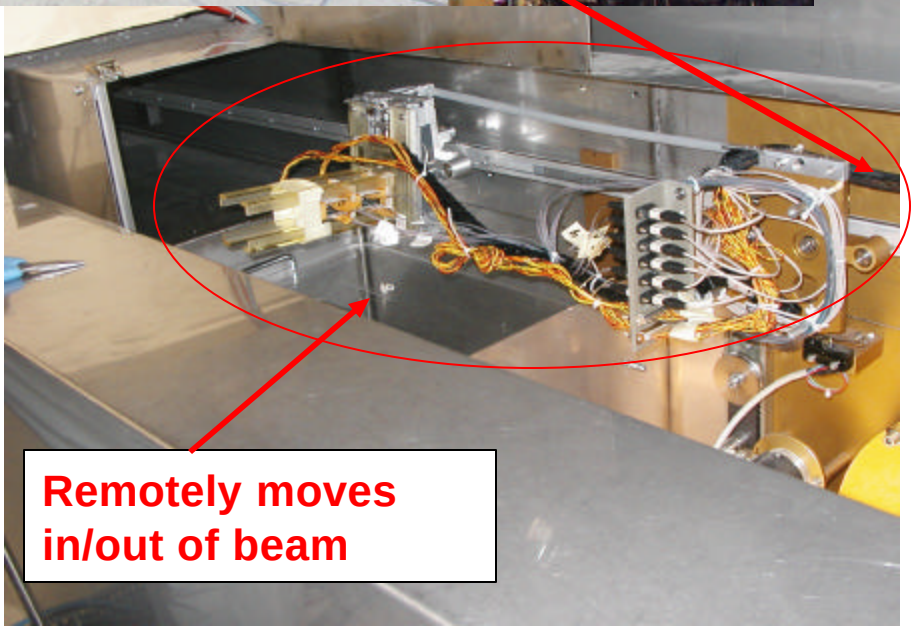


25 meter optical fiber



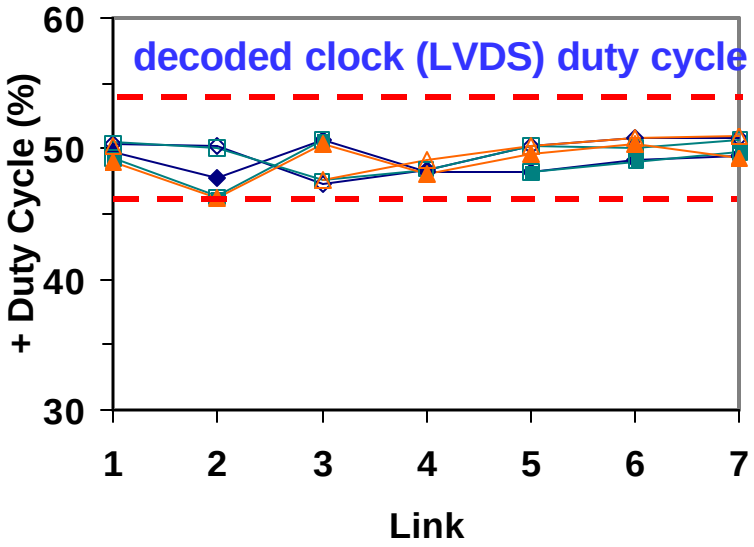
Opto-boards

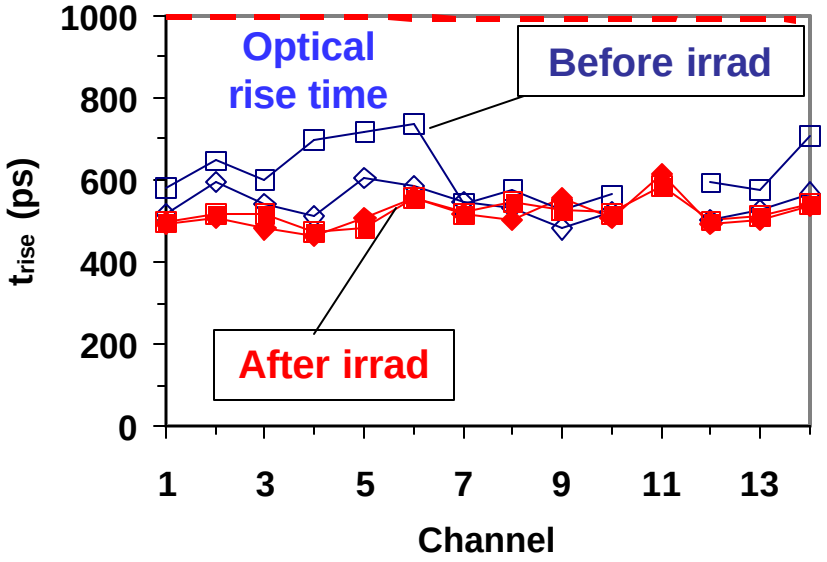
Rad hard optical fibers

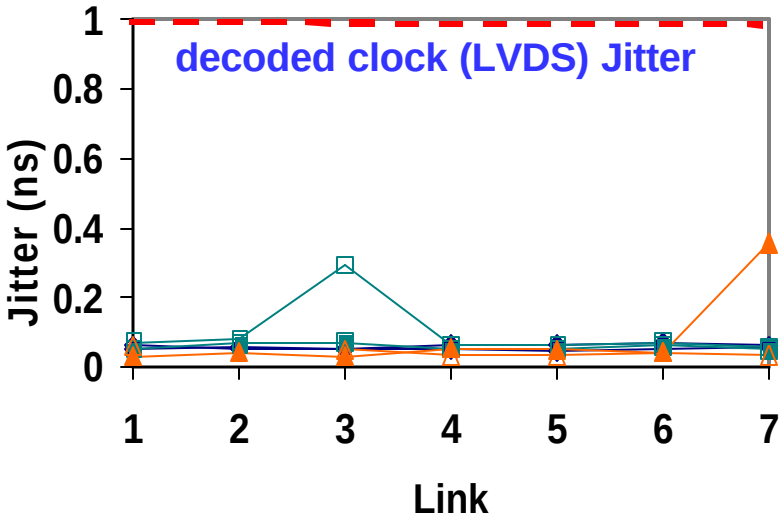


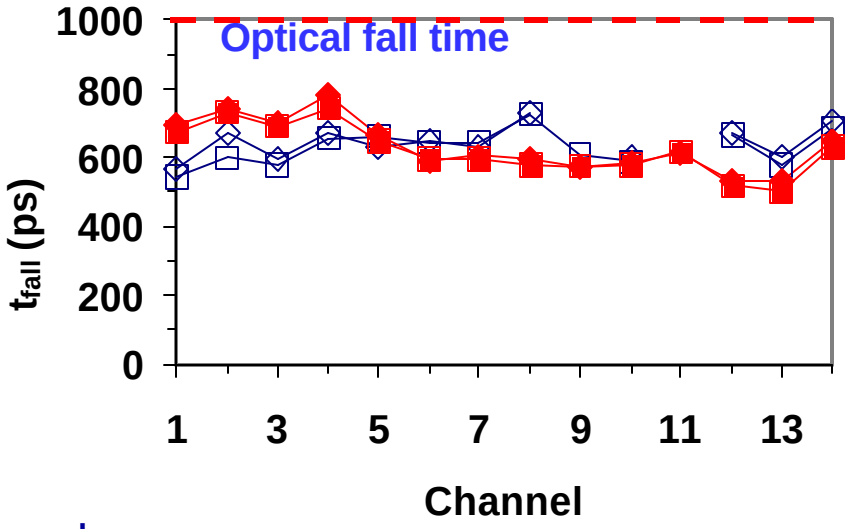
Remotely moves in/out of beam

Rise/Fall times, Jitter, and Duty Cycle



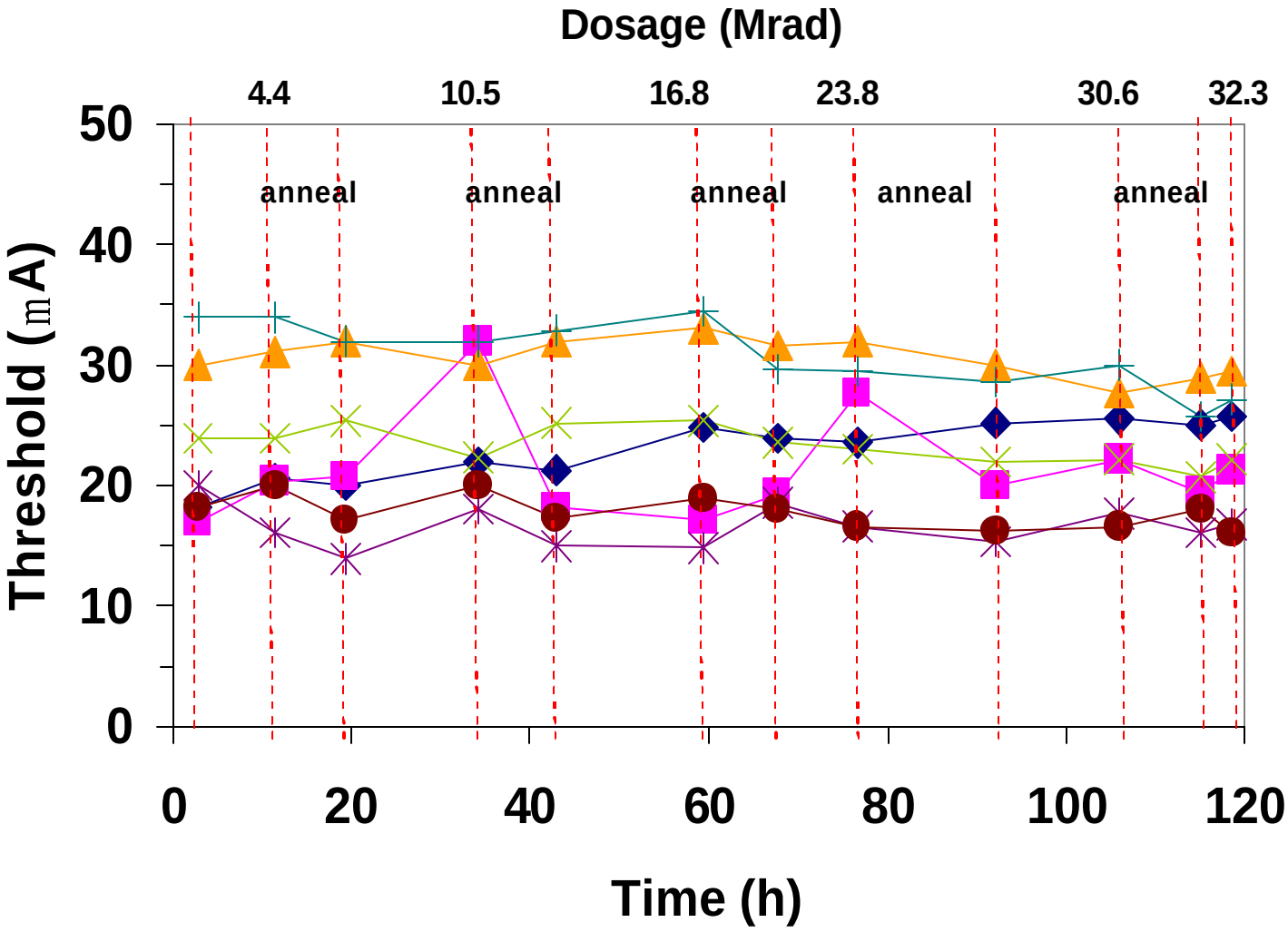






- Each plot shows the results for two opto-boards
- No degradation in rise/fall times
- Decoded clock duty cycle and jitter within the limits after irradiation

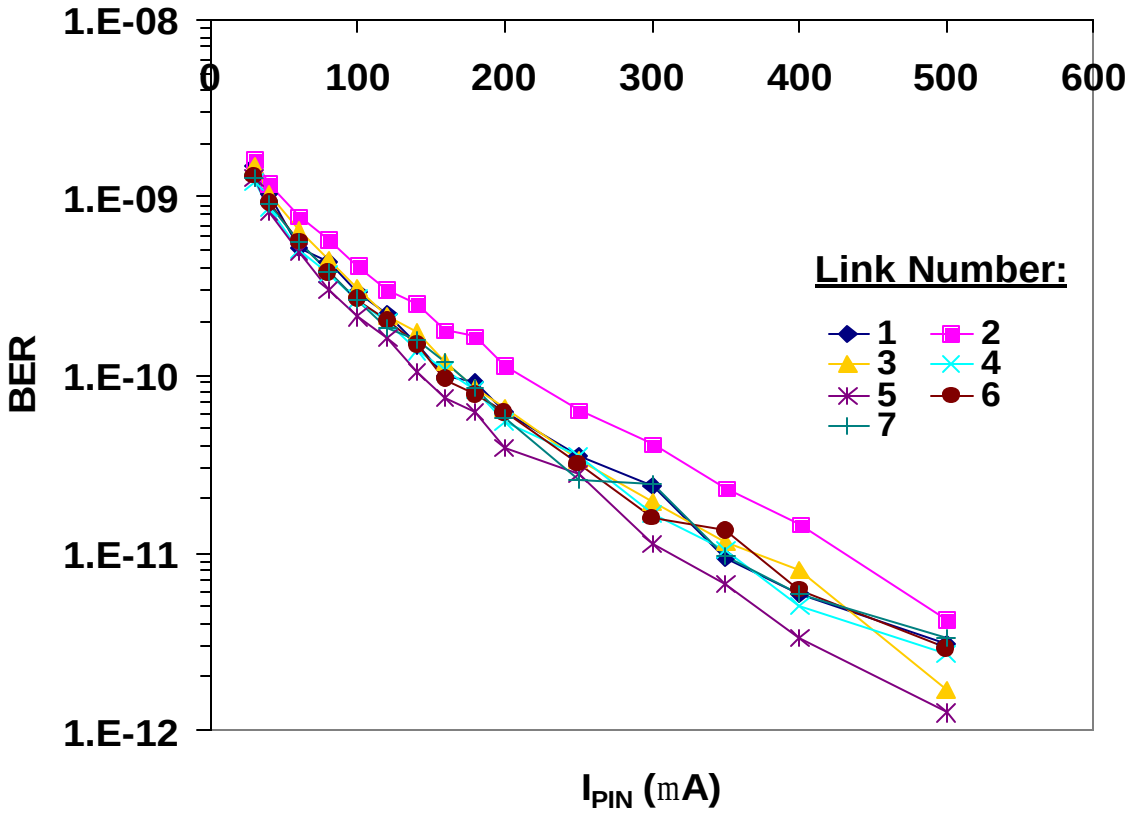
PIN Current Threshold vs Dosage



- PIN current thresholds for no bit errors remain constant

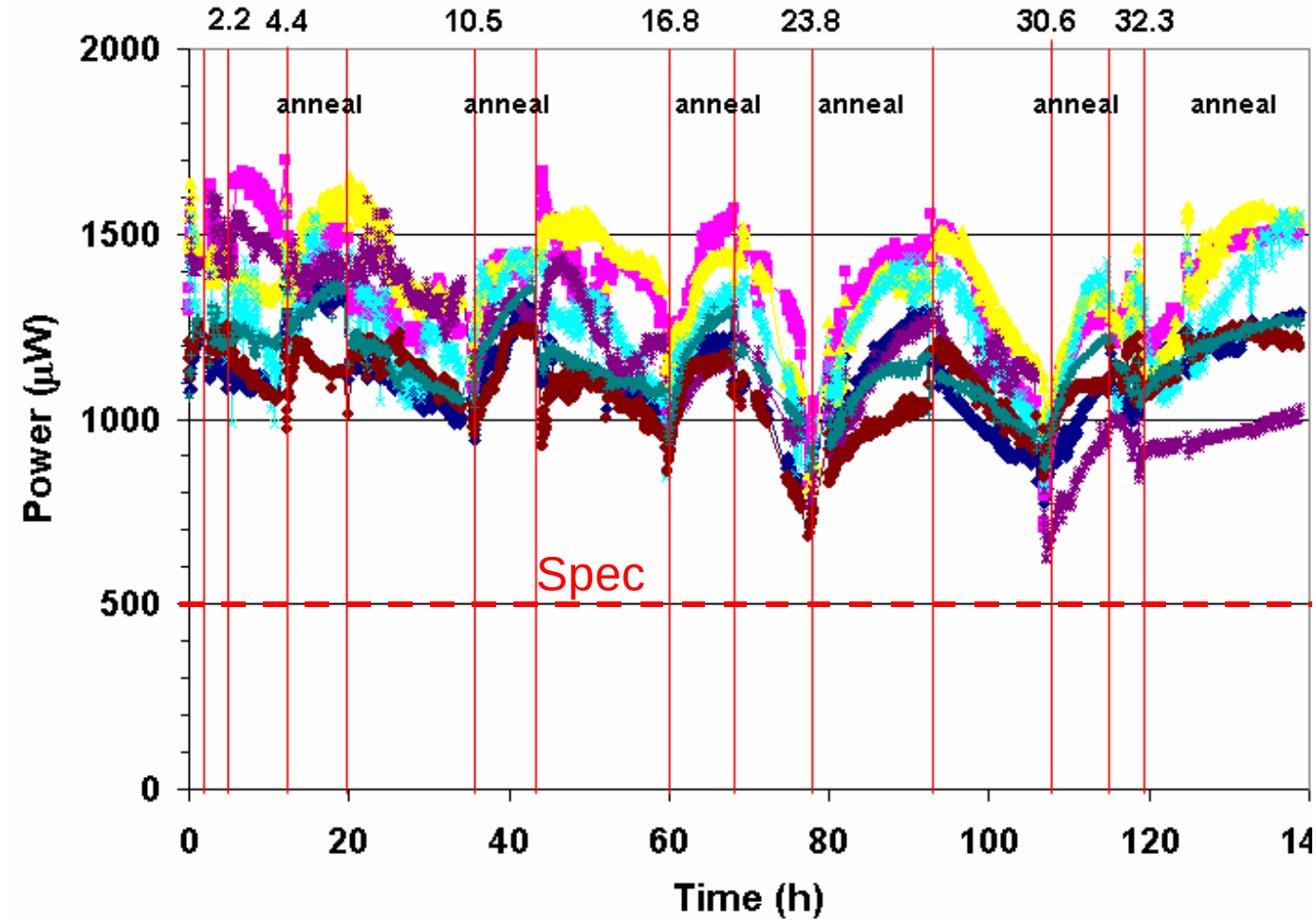
Proton Induced Bit Errors in PIN

- Convert bit errors to bit error rates at opto-link



- Bit error rate decreases with PIN current as expected
- Bit error rate: ~3 x 10^{-10} at 100 mA (1.4 errors/minutes)
  - DORIC sepc: 10^{-11}
  - Opto-link error rate is limited by SEU

Optical Power vs. Dosage



- Irradiation procedure ~5 Mrad/day (10 hours) with annealing rest of the day
- Optical power decreases with dosage as expected
- Limited annealing recovers some lost power
- Still good power after 30 Mrad

Summary

- VDC-I5e and DORIC-I5e meet all the specifications
  - Production is completed
- Radiation hardness of DORIC and VDC is adequate for the PIXEL detector
  - Circuits continue to perform well after up to ~62 Mrad of 24 GeV protons
- Several pre-production opto-boards have been fabricated
  - Meet all the pixel detector requirements
  - Excellent optical power
- No degradation in performance with up to 32 Mrad proton irradiation
  - Low PIN current for no bit error
  - Annealing recovers most of the lost power
- Start opto-link production in September 2004
  - Complete production by September 2005