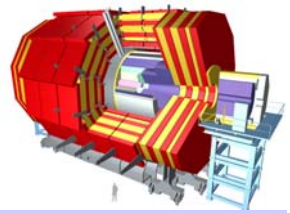

Production testing and quality assurance of CMS silicon microstrip tracker readout chip

Pierre BARRILLON - Imperial College London

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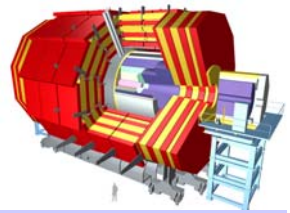
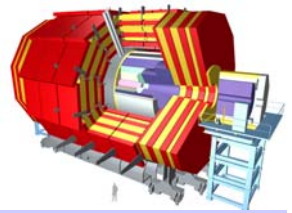
Boston, 14th September 2004

Outline

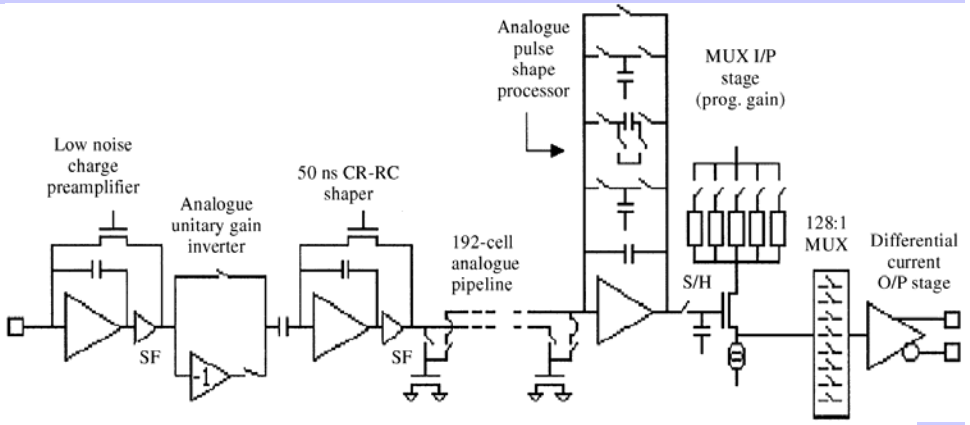


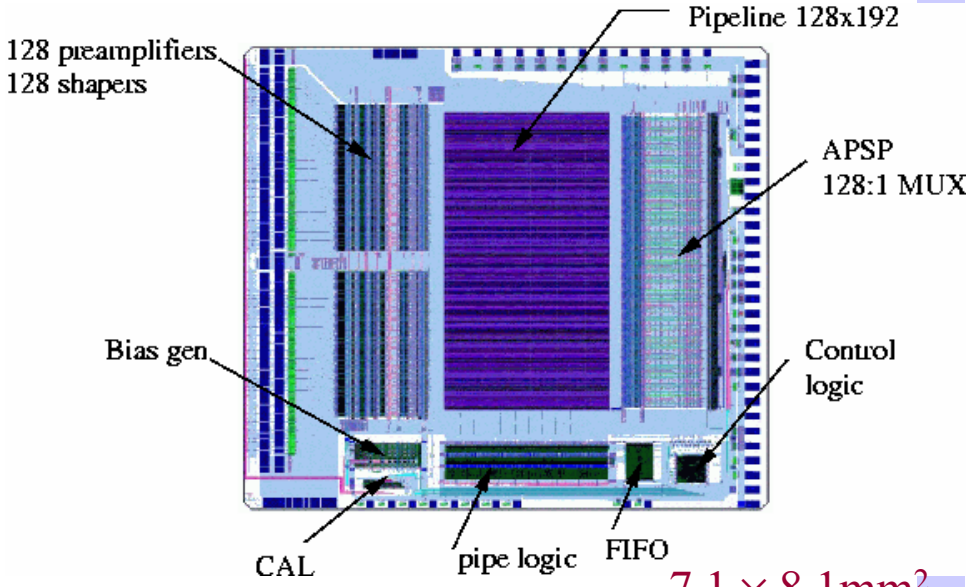
- APV25 chip description
- APV25 production
- Wafer probing:
  - Set-up and tests
  - Yield problem
  - Final results
- Quality Assurance tests:
  - Set-up and tests
  - Main results
- Conclusion

APV25 Description



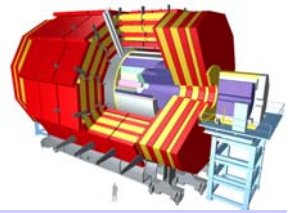
- Readout chip for the CMS silicon detector (75,000 needed + spares)
- 0.25 µm technology
- Read signal from 128 channels
- 50 ns CR-RC shaper
- 192-cell pipeline (up to 4 µs latency + buffering)
- 2 modes:
  - Peak (1 sample)
  - Deconvolution (weighted sum of 3 samples)
- I²C slow control interface (bias registers, …)
- On-chip calibration: amplitude and delay programmable
- Radiation hardness > 10Mrads



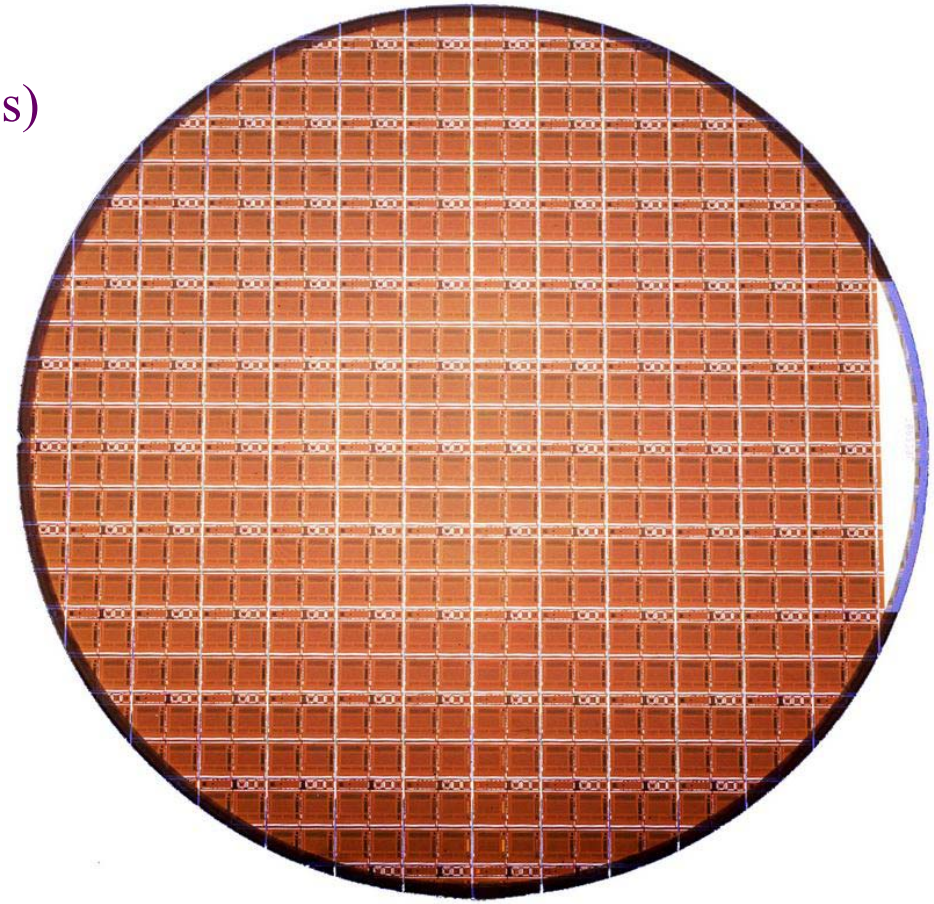


$7.1 \times 8.1 mm^2$

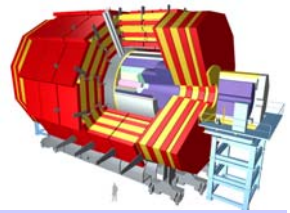
APV25 Production – Wafer testing



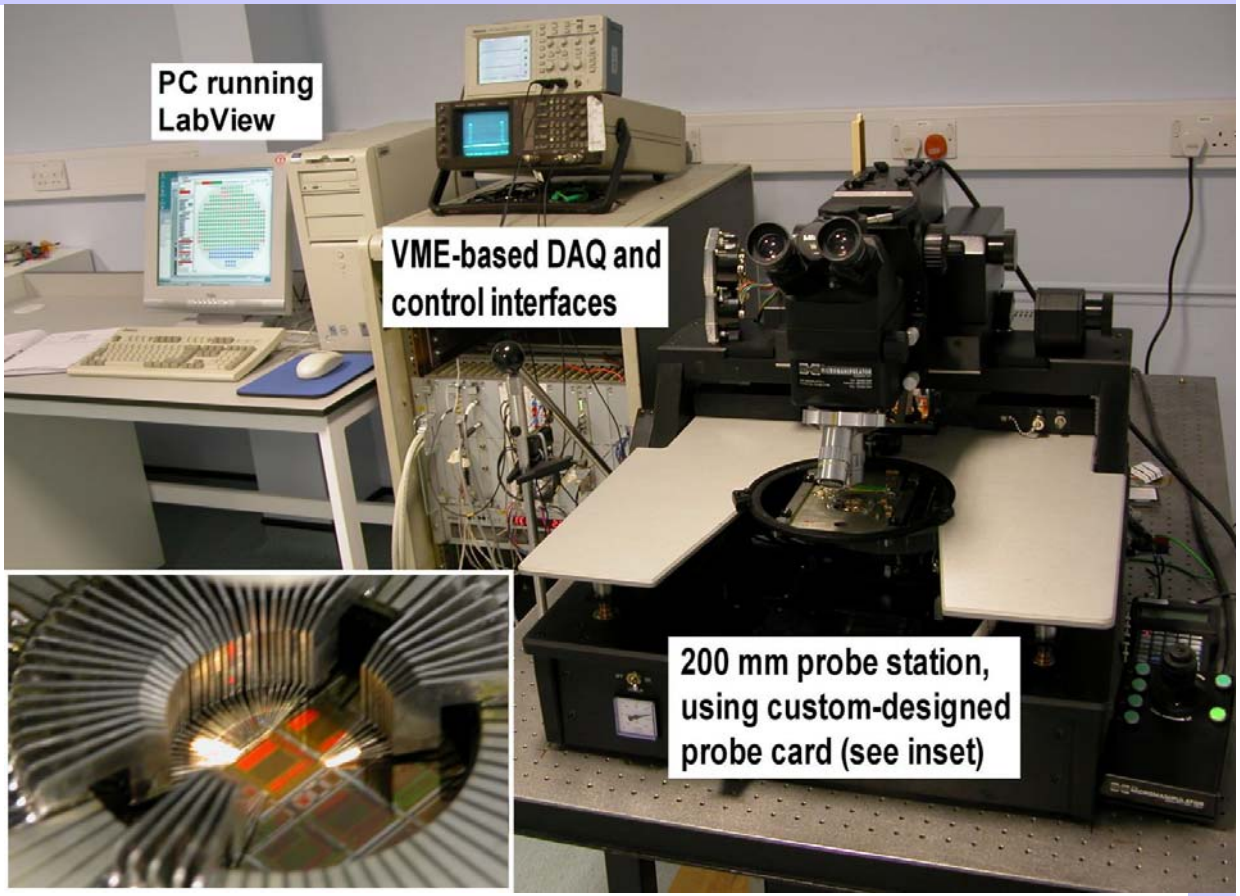
- 8 inch wafer (IBM Microelectronics)
- 360 APV chips per wafer
- Wafers delivered by lot of 25
- Automatic test needed to select the good dies (KGD) before cutting (map generated for each wafer)
- Number of wafers depends on the average yield (~ 300 wafers for a mean yield of 70 %)
- 2 wafers/day throughput required to follow the production



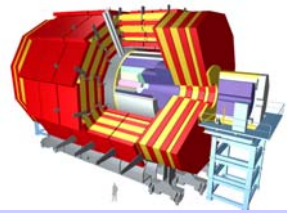
Wafer Probing: set-up



- Probe station (semi-auto)
- VME-based DAQ and control interfaces (8 bits ADC, VI2C, SeqSi)
- Computer (labview software) controls probe station (RS232) and DAQ (VME)



Wafer Probing: tests

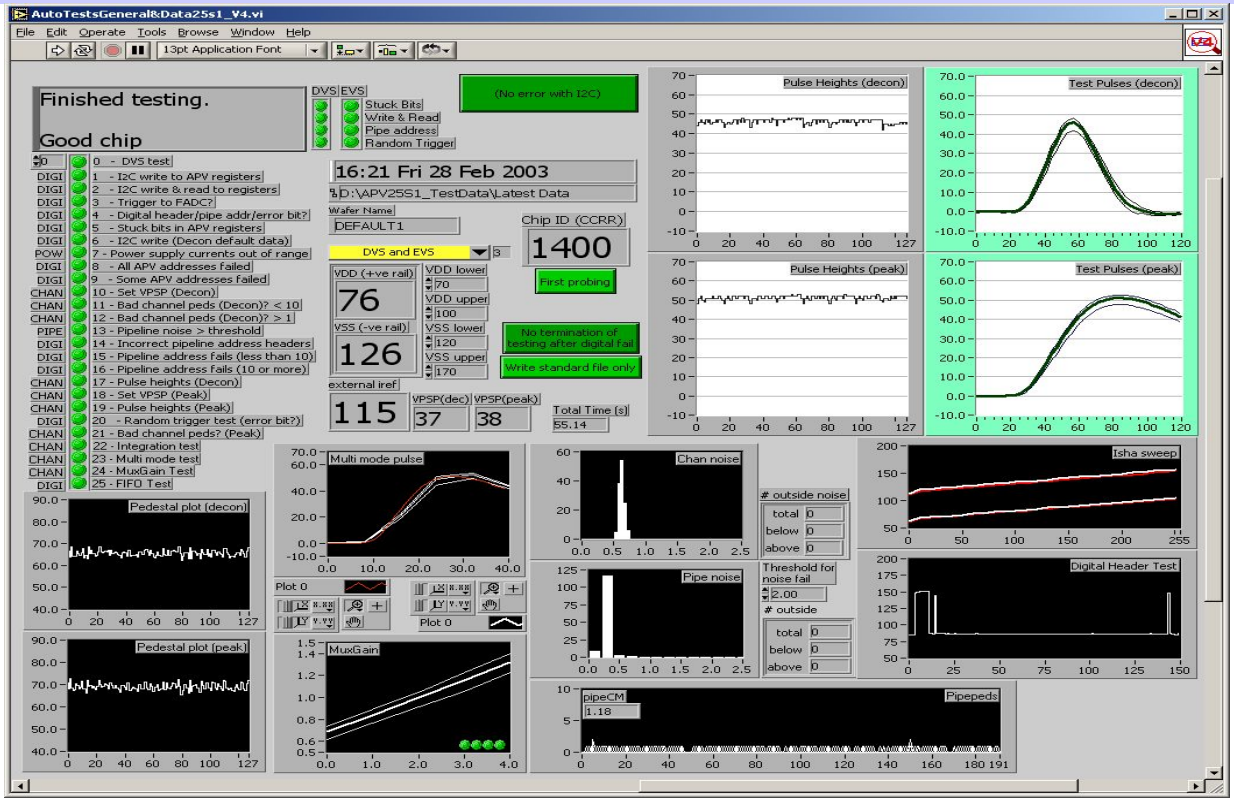


2 types of tests:

– Digital (chip addressing, pipeline control logic, …)

– Analogue (supply currents, pulse shapes, noise, …)

All results are summarized on the main window of the labview soft (VI)

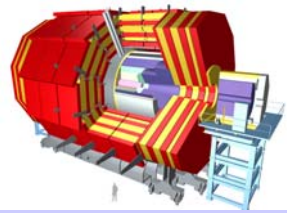


~ 70 sec are needed for the test of a chip

→ ~ 7h/ wafer → 2 wafers/day (as required)

Yield = nb KGD/360

Wafer test: first lots

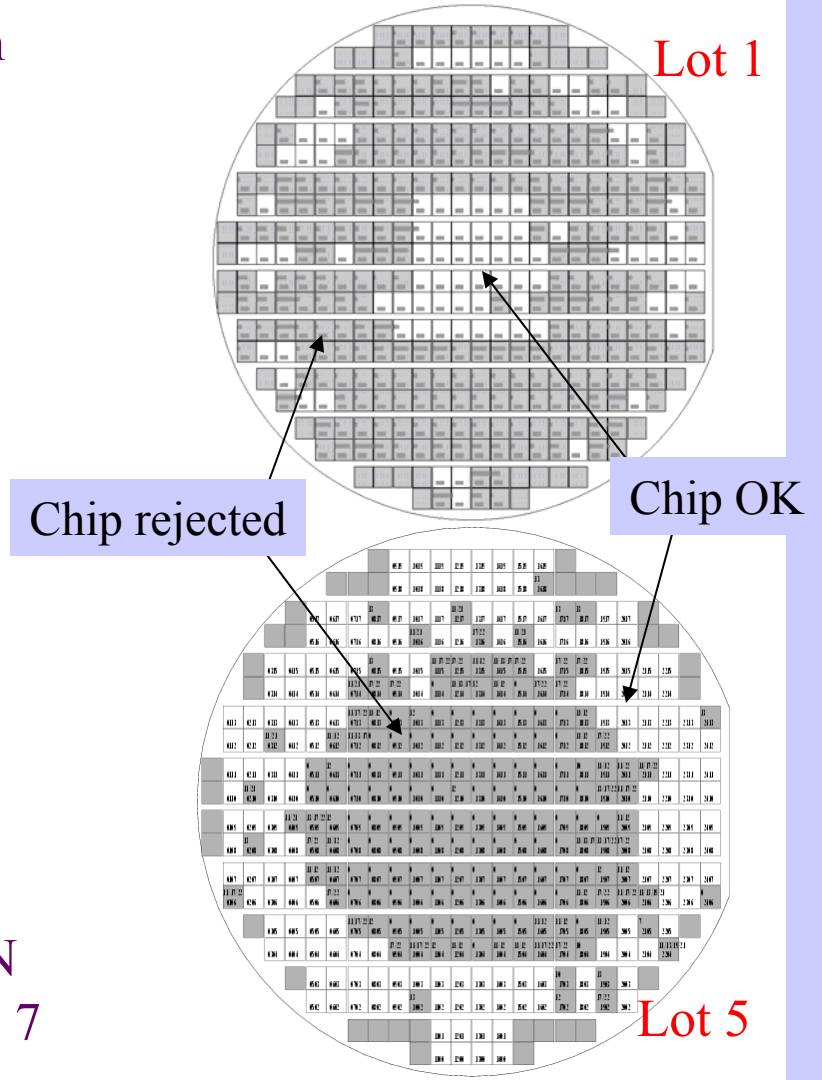


- Low yield observed for the first production wafers:
  - Lots 1 (30%) and 2 (10%)
- Similar circular patterns observed
- Investigations showed few defects in the silicide layer → lots replaced
- Following lots also exhibited low average yield with a different pattern

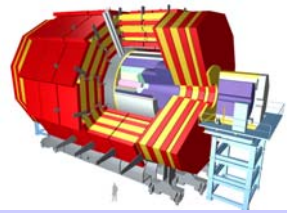
Lot Nb	3	4	5	6	7	8
<Yield> %	79	28	42	~ 0	37	58

March-May 02 | Jan-April 03

- Major investigation was launched in collaboration with manufacturer and CERN (Feb 2003) → Failure Analysis on lots 4 to 7

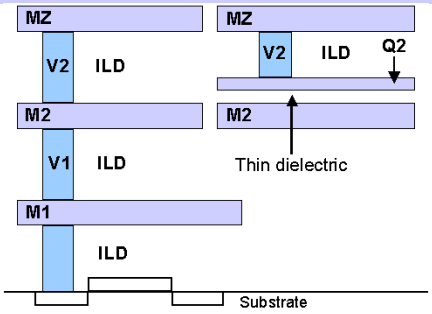


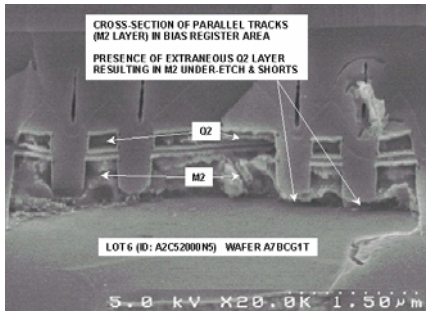
Failure Analysis results

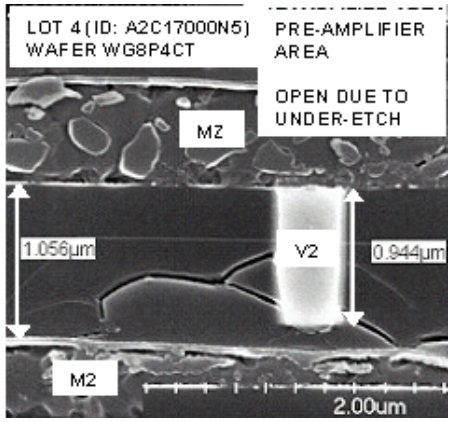


- Investigation of suspect locations performed thanks to top-down layering of the wafer or by cross-sectioning through the wafer + electron microscope inspection.
- APV25 contains 3 layers of metal tracks (M1, M2 and MZ). Vias (V1 & V2) insulated by an inter-level dielectric (ILD) connect them. Intermediate layer (Q2) allows to realize metal-insulator-metal capacitors.
- Lot 6: shorts were found. Due to extraneous Q2 metal located in areas where it should have been removed.
- Lots 4, 5 & 7: open circuits were found between layers (MZ and M2). Interconnecting vias (V2) were not fully penetrating the ILD. High ILD thickness was the reason for the bad contact to M2 layer.

  ⇒ Process has been slightly changed since lot 9

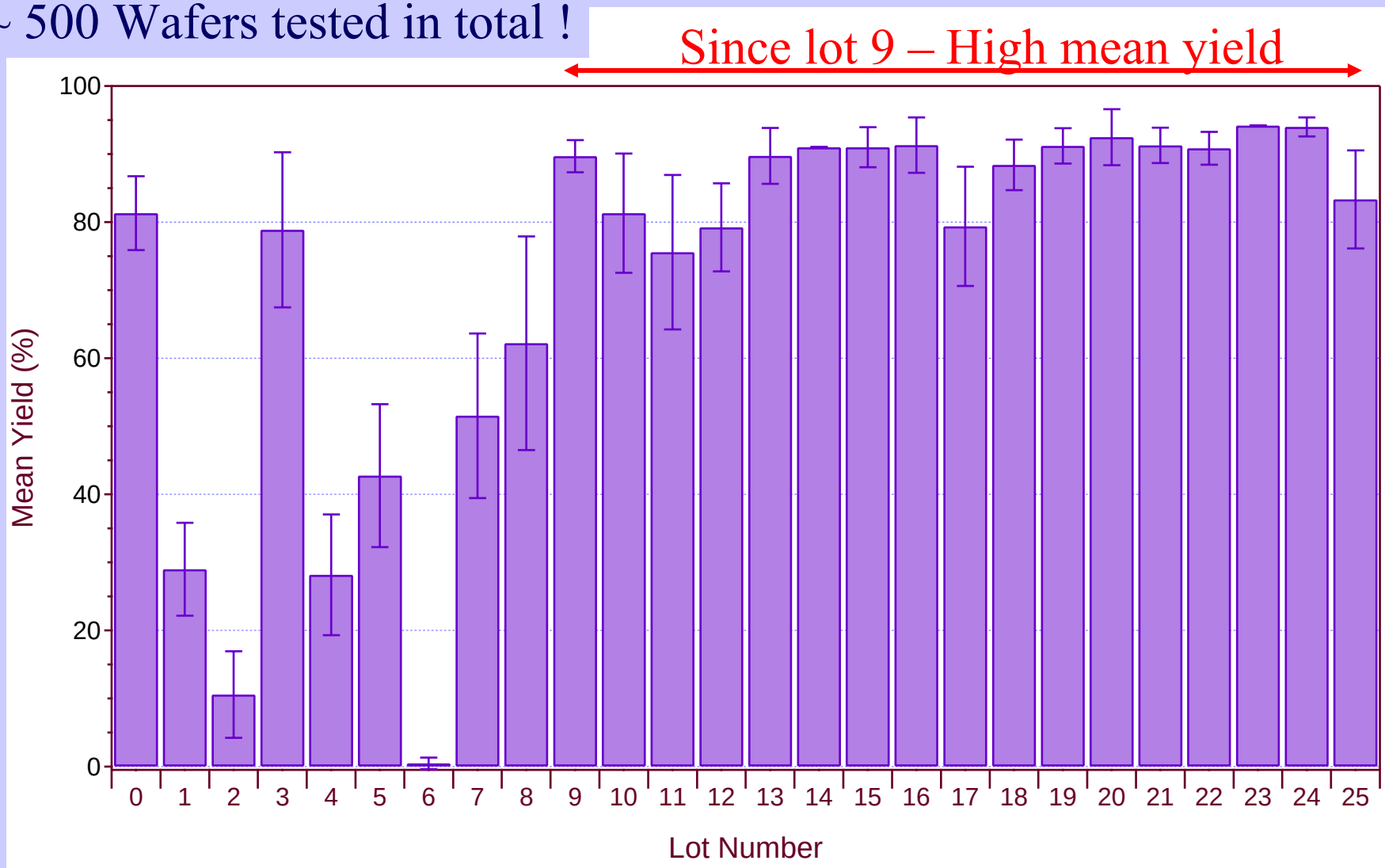




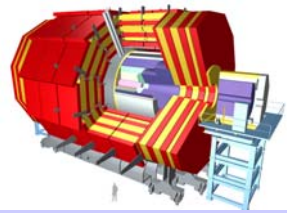


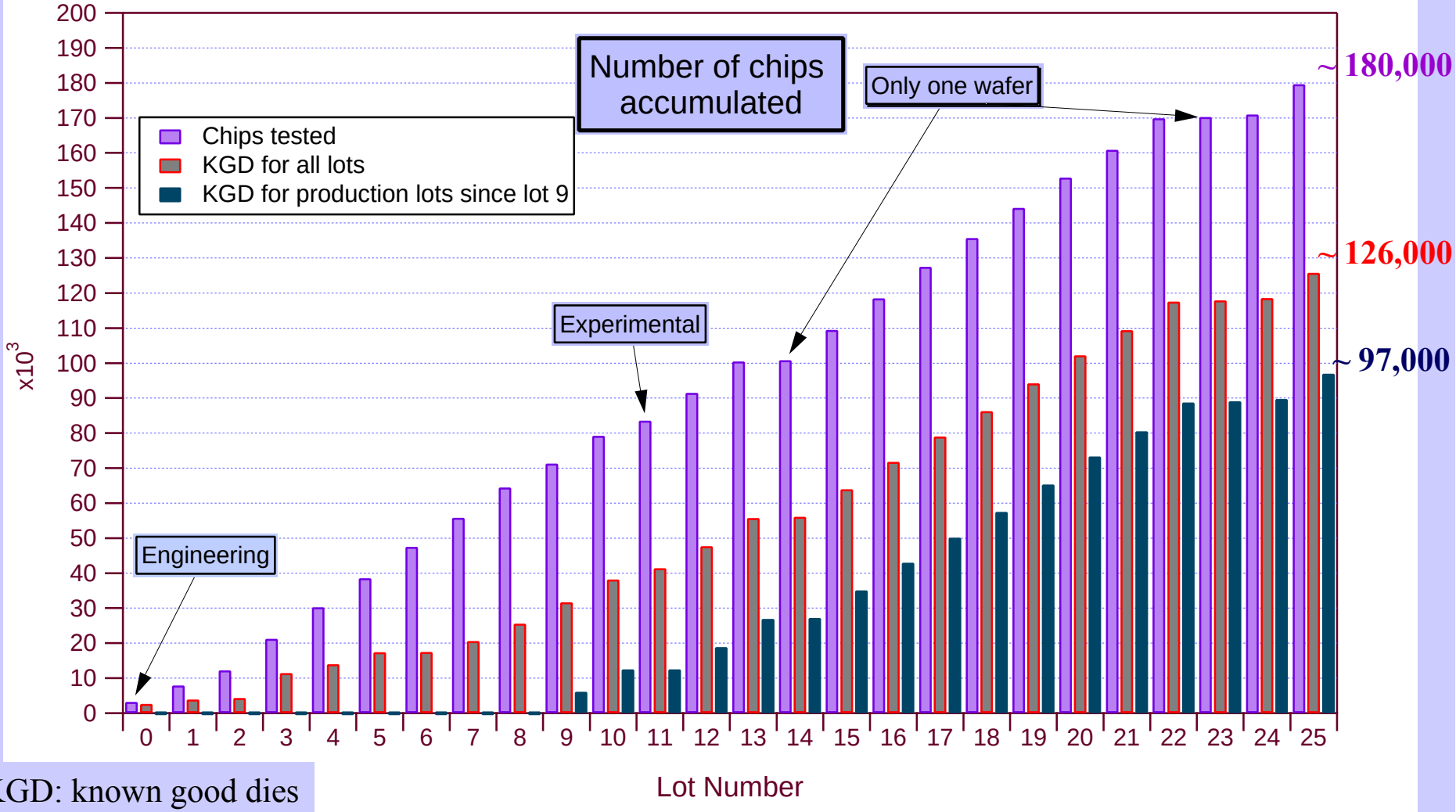
Wafer Probing: mean yield

~ 500 Wafers tested in total !



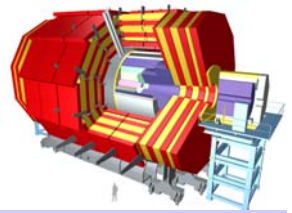
Wafer Probing: Number of chips



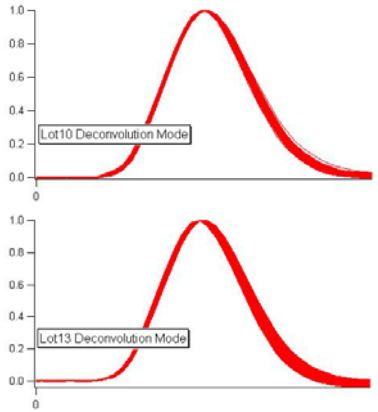


KGD: known good dies

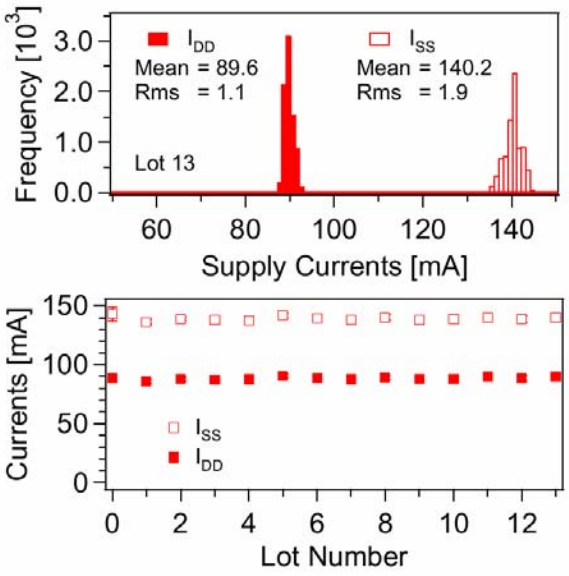
Wafer Probing: Results



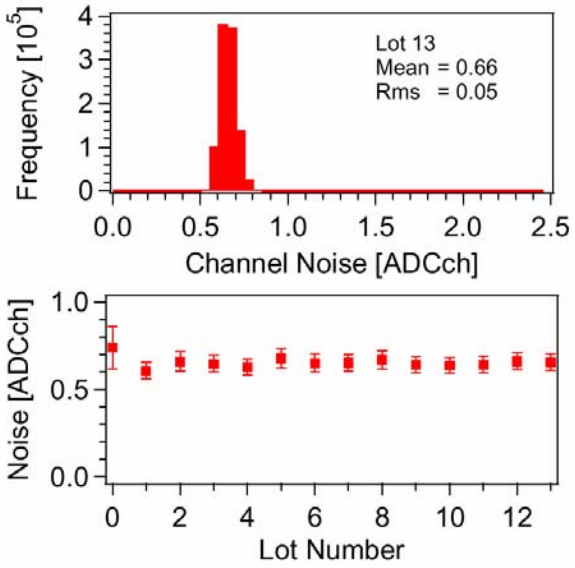
- Results from all KGD merged lot by lot
- Good pulse shape matching for both modes from wafer to wafer and lot to lot
- **Similar results → <u>no wafer or lot dependence</u>**



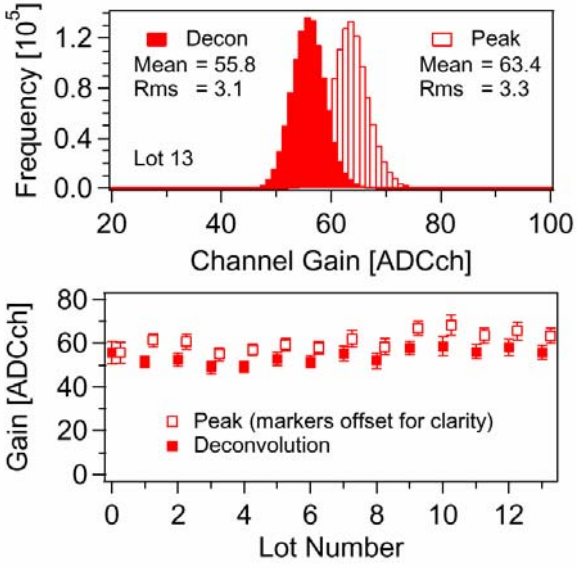
Supply Currents



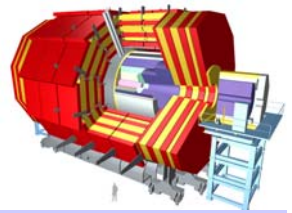
Channel Noise



Channel Gain

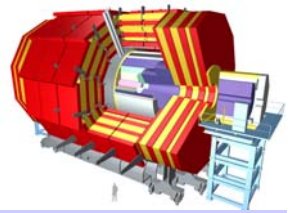


Wafer probing: summary

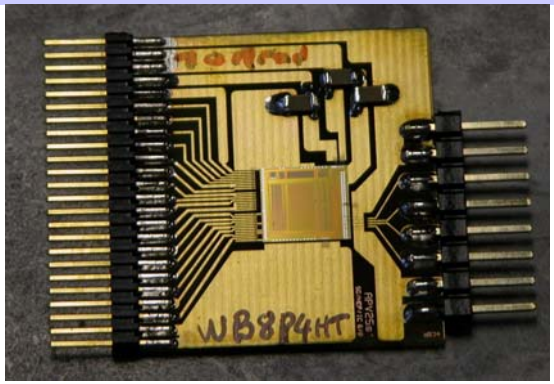


- Yield problem solved thanks to an important collaboration work with manufacturer and CERN people
- Yield stayed at a high level since lot 9 (87 %)
- Wafer probing results showed a nice agreement between wafers and lots
- Final number of chips: ~ 118,000 (97,000) since lot 3 (9)
- Enough chips to build the tracker + a lot of spare ones in case of problem during the construction of hybrids and/or Silicon detectors

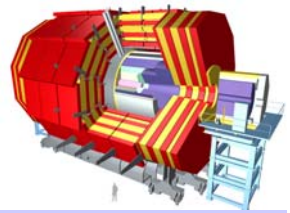
Quality Assurance: set-up

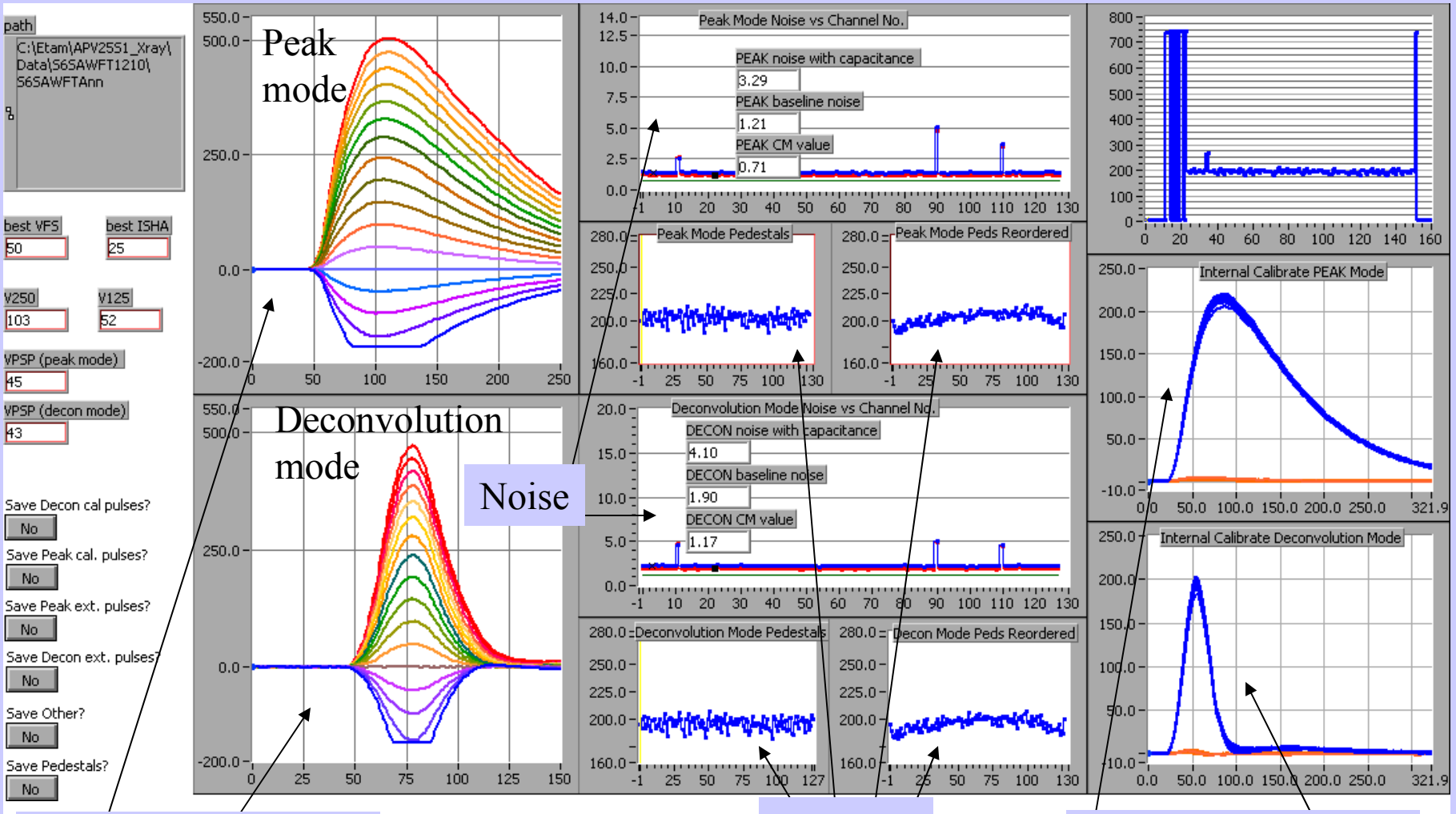


- QA tests:
  - Performed before and after irradiation at IC and Padova on KGD selected (1/wafer)
  - APV mounted on a daughter board
  - VME-based DAQ + computer (labview)
- Irradiation:
  - Irradiation chamber (X-ray)
  - 10 Mrad (accuracy of 10%): ~13h
  - Chip randomly triggered
- Annealing:
  - Environmental chamber
  - One week at 100°C
  - Chips (8) randomly triggered

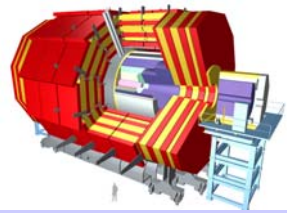


QA: results example



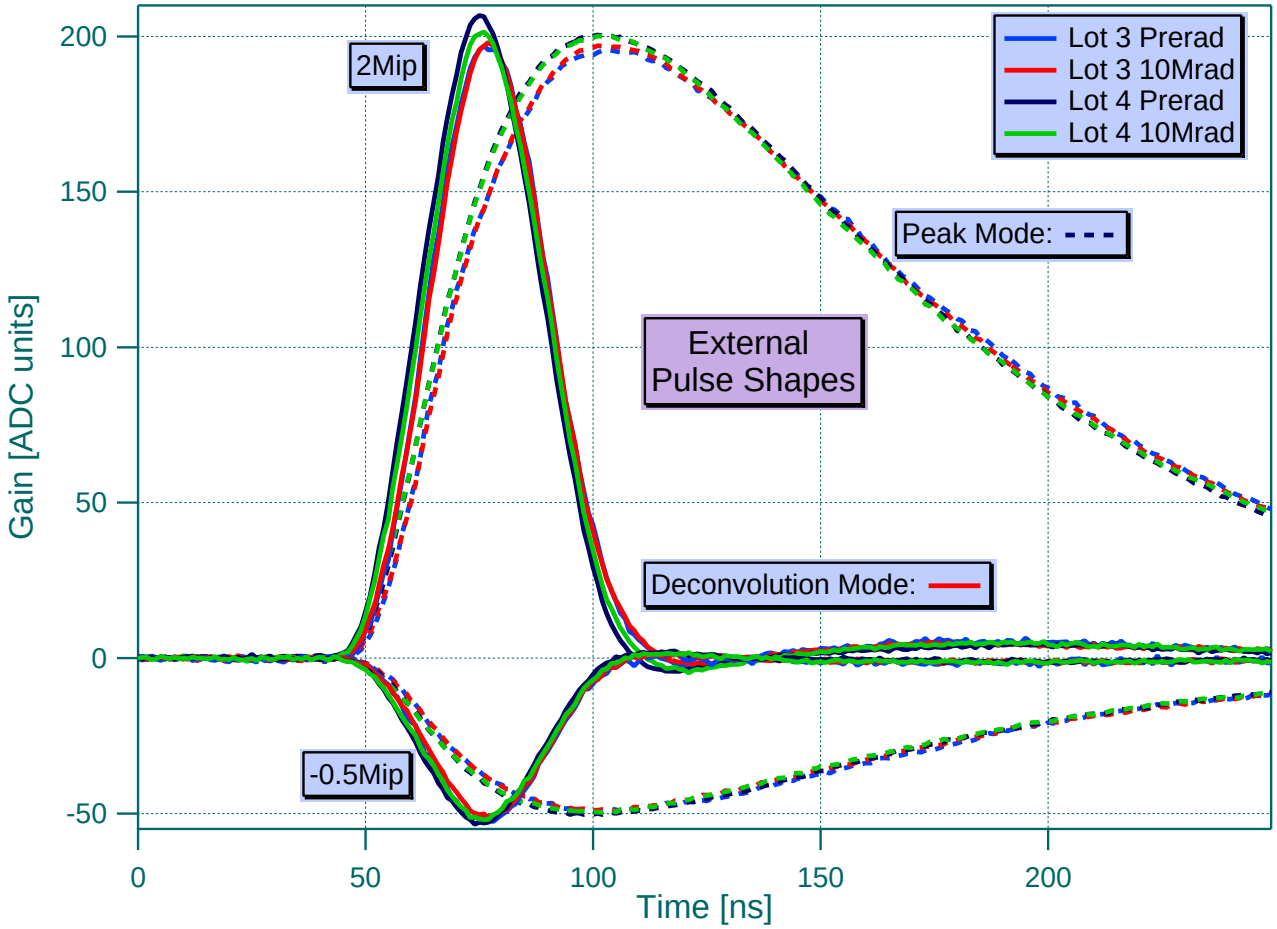


Quality Measurements: shapes

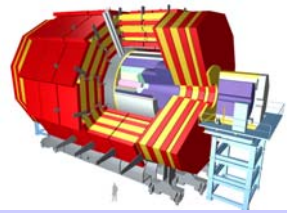


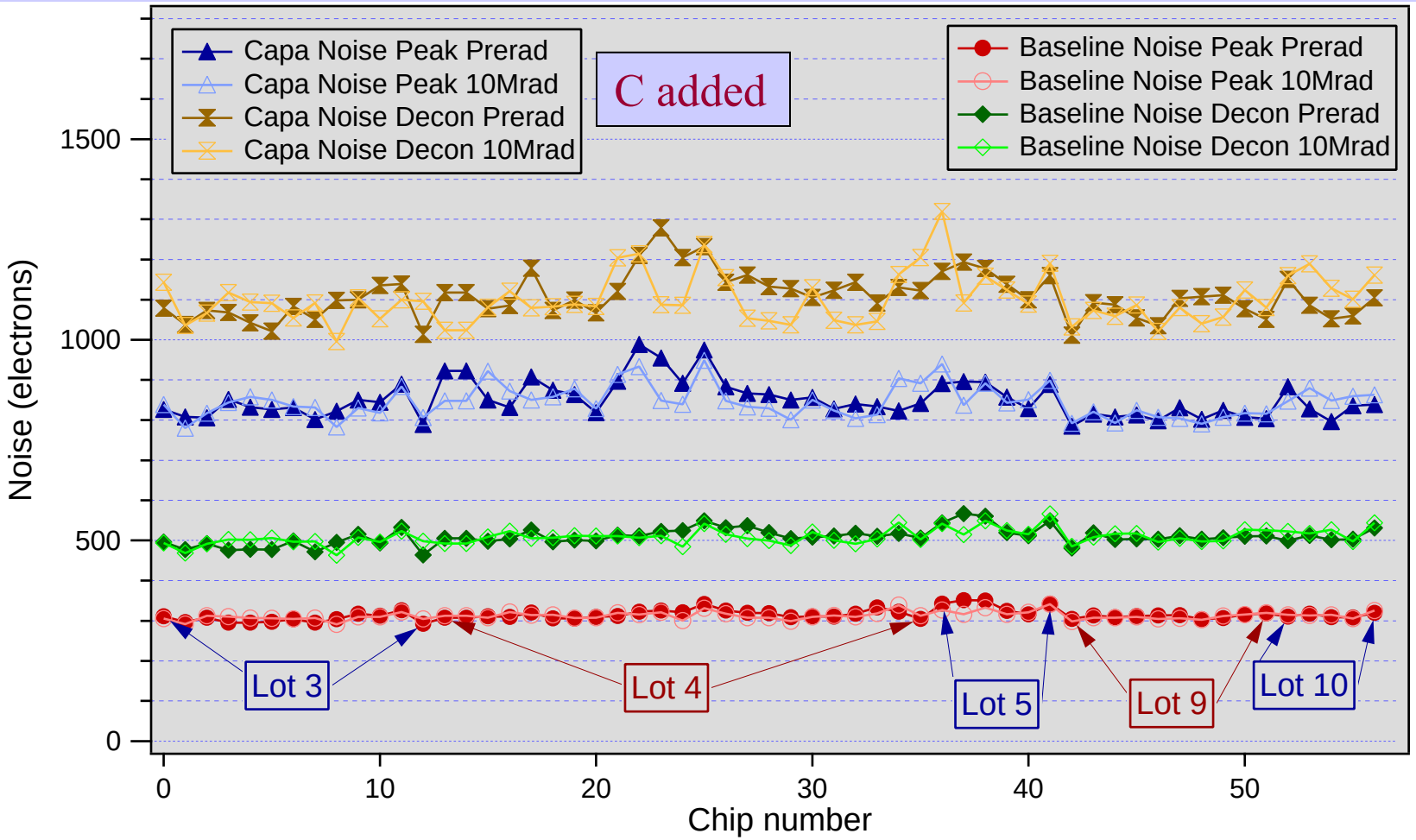
Nice pulse shape matching:

- for both modes
- before and after irradiation
- between lots



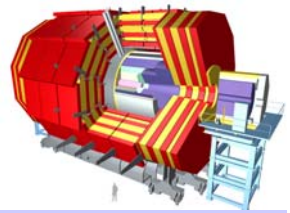
Quality Measurements: noise





No noise variation from chip to chip and lot to lot

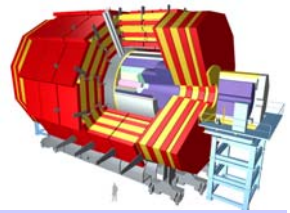
Quality Assurance: summary



- More than 100 chips have been irradiated and half of them annealed
- The results have not showed strange behavior after irradiation or annealing.
- Radiation tolerance of the APV25 is proved

  → Since lot 10, only 4 chips per lot are tested

Conclusion



- APV25 Wafer probing is finished (last wafer tested in June 2004)
- Yield problem for the first lots has been understood and solved thanks to a dedicated failure analysis (detailed and comprehensive work performed by IBM and the ALTIS foundry in collaboration with IC, RAL and CERN)
- Since (lot 9) the yield has been high (> 80%)
- 97,000 good dies have been selected since lot 9
  → Enough for the CMS silicon tracker (~75,000 + spares)
- Quality Assurance tests have showed that the APV25 chips are radiation tolerant up to 10 Mrad