10th Workshop on Electronics for LHC Experiments, September 2004, Boston

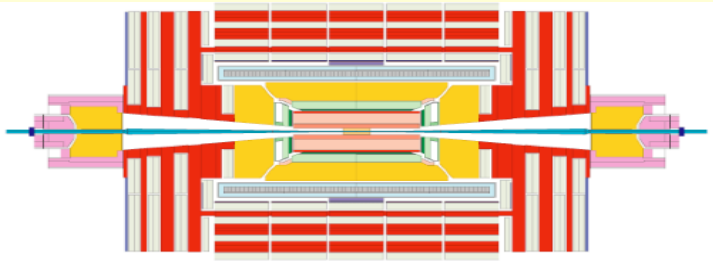
CMS ECAL Trigger Primitives: Tests of the boards

M.Bercher, P.Busson, M.Cerutti , C.Collard, A.Debraine, L.Dobrzynski, Y.Geerebaert, J.Gilly , A.Karar, P.Paganini, N.Regnault, T.Romanteau, L.Zlatevski

Outline

- Overview of the ECAL Trigger Primitives
- The Front-End board
  - Brief overview
  - XFEST: the eXtended Front-End System Test
- The Trigger Concentrator Card
  - Brief overview
  - TCC24: the prototype
    - Tests of the TCC24
  - Test bench for production

The ECAL Trigger Primitives



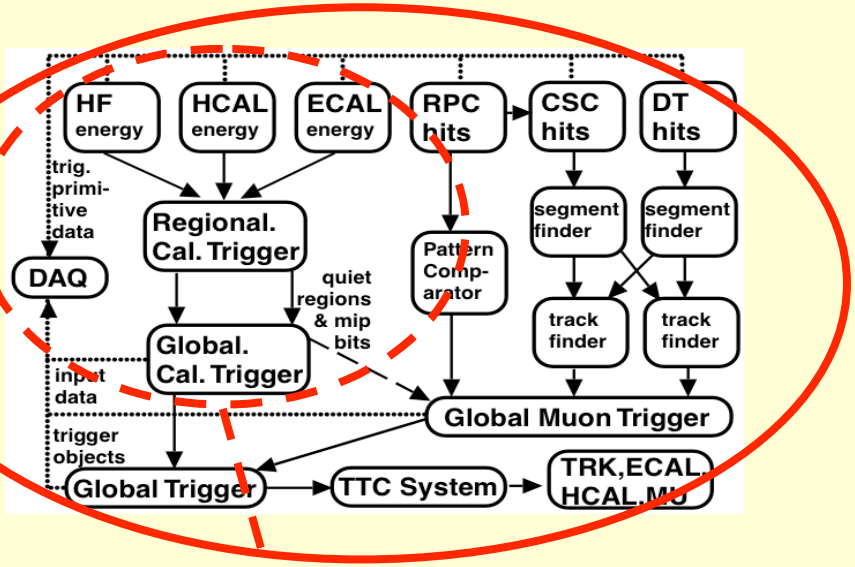
40 MHz (1000 TB/s)

Level 1 Trigger (dedicated hardware)
(e, gamma, mu)

100 KHz

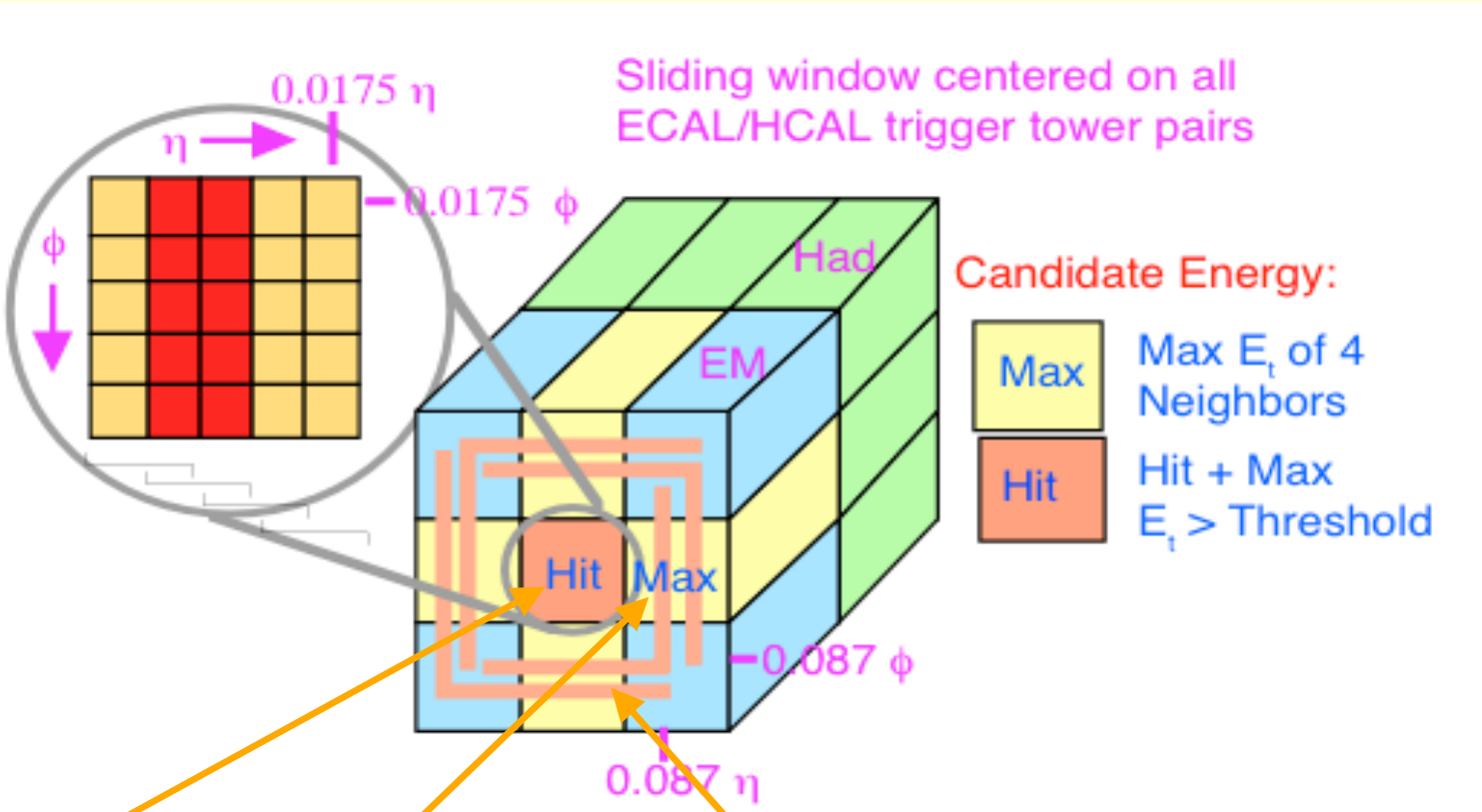
High Level Trigger (software)

100 Hz (100 MB/s)



ECAL Trigger Primitive (TP) 40 MHz pipeline :
- 8 bits: Energy sums of a trigger tower + Bunch crossing assignment
- 1 bit: ECAL Fine Grain bit

The ECAL Trigger Primitives and e/γ trigger



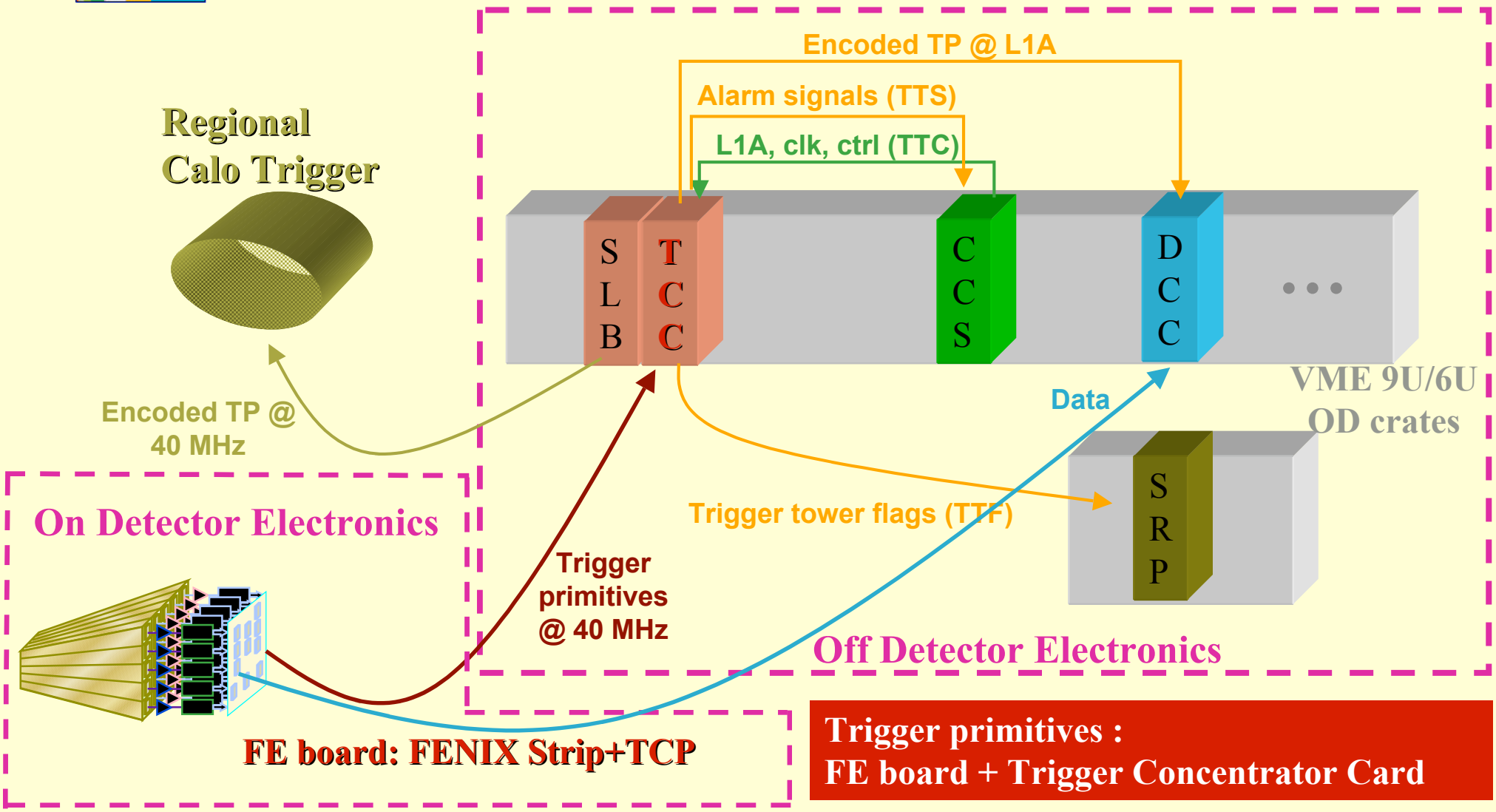
Electron:

1. E_T "Hit tower" + "Max tower" > threshold
2. Fine Grain (FG) veto: highest energy adjacent strip pair ≈ large fraction of total (e.g. 90%)
3. H/E veto (e.g. 5%)

Isolated Electron:

1. 8 neighbours towers with FG veto and H/E veto
2. 1 group of 5 "corner towers" with E_T < threshold

The ECAL Trigger Primitives Path

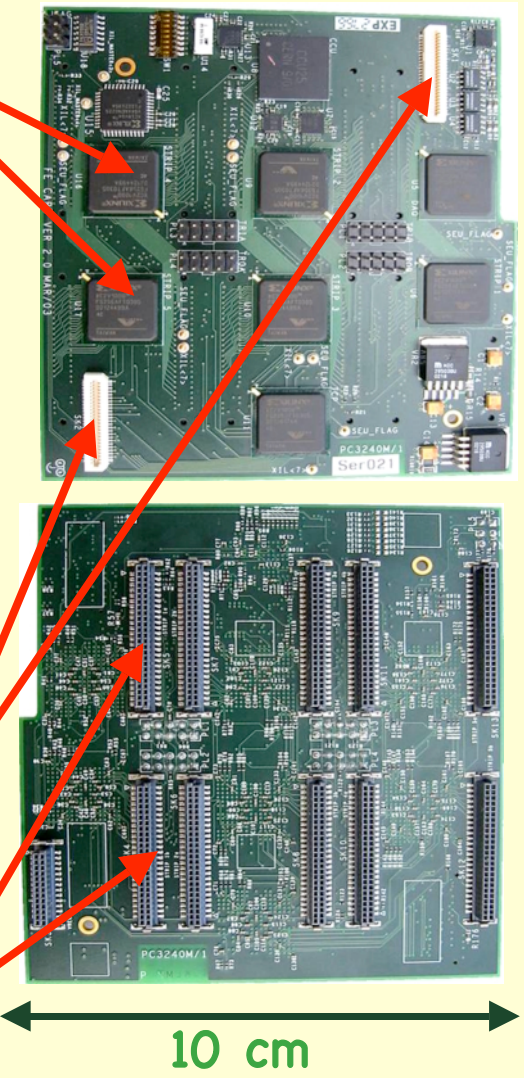


The Front End Board

Brief overview of the Front End board

- The FE board:
  - receives signals from a trigger tower (25 crystals of 5 VFE)
  - stores the data during the L1 latency
  - performs the Trigger Primitive calculations
  - formats and sends the data (via GOH: Giga Optolink Hybrid) to the DAQ (DCC board) when L1 accept signal.
  - sends the Trigger Primitives to the TCC @40 MHz (via GOH)

For details, see M. Gastal's talk

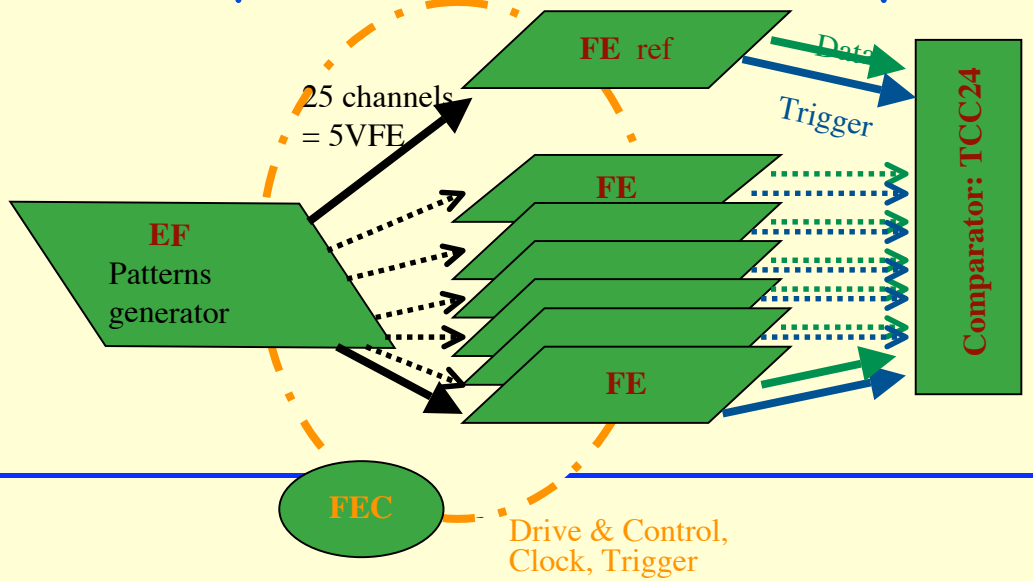


XFEST: eXtended Front-End System Test

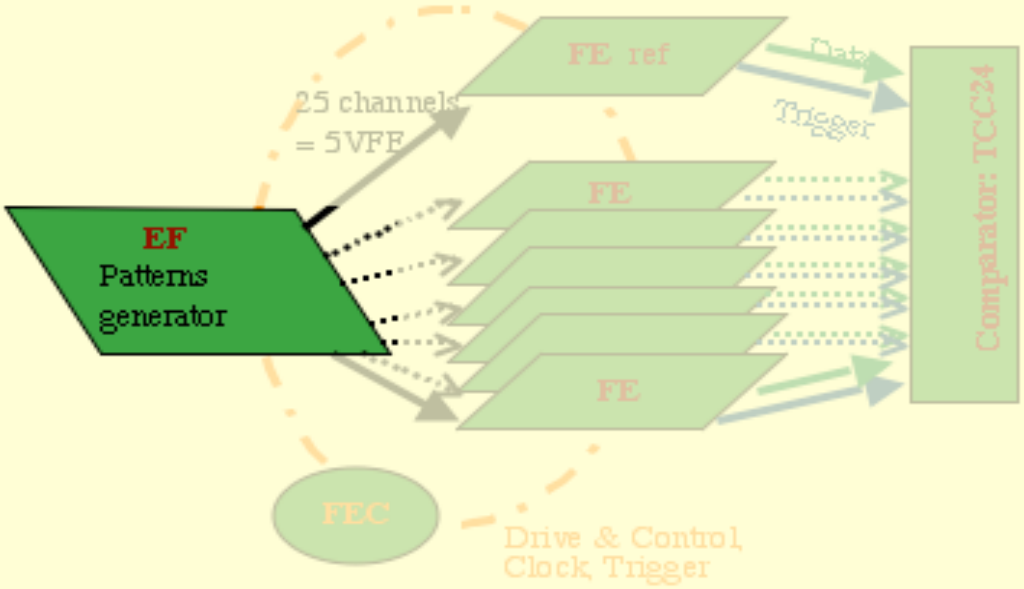
XFEST: System Test for FE board production

- 3200 boards to be tested, 80/week until mid-2005
  1. Short tests: just after burn in to reject quickly dead boards (see M. Gastal's talk)
  2. XFEST: Long tests (several hours) with lots of patterns
- 1 FE board : inputs 25 x 16 bits @ 40 MHz, outputs 2 x 800 Mbits/s ⇒ impossible to cover all patterns in a reasonable time
- Idea: inject same realistic inputs to several boards in parallel

Basic Synoptic :



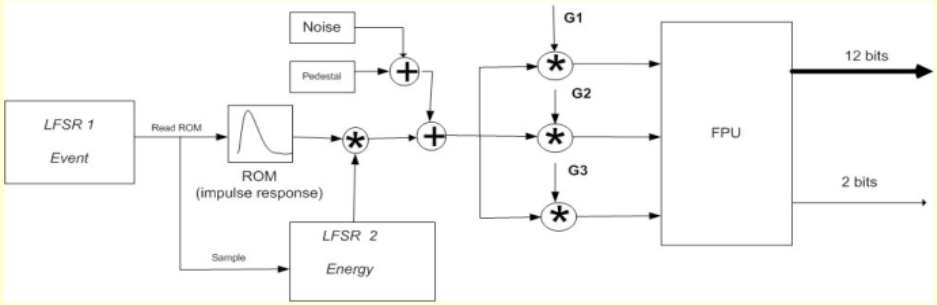
XFEST: 1) Pattern Generator



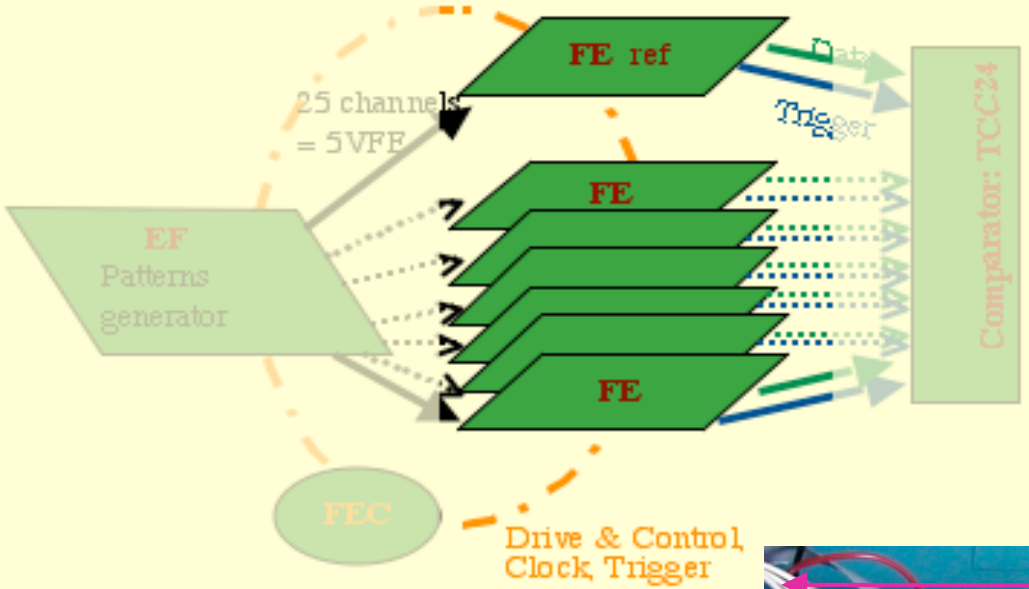
Use a FE itself: FE → EF

EF = FE prototype with FPGAs + FPGA reprogramming:

- Emulates signals from VFE:
  - MGPA multigain
  - Random noise using LFSR (40 bits)
  - Variable signal amplitude using LFSR
- Allows loading of different signal shape
- Allows superposition of signals to mimic pile-up



XFEST: 2) Mother board



Mother board:

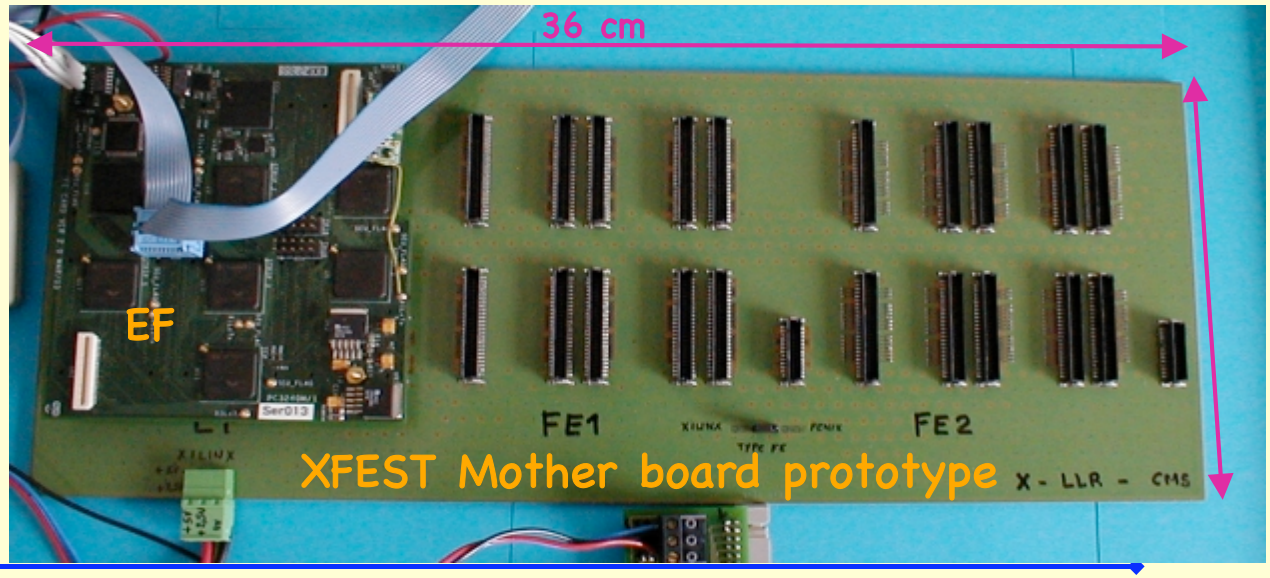
- Connect EF to several FE
- Power supply

Realisation of a prototype:

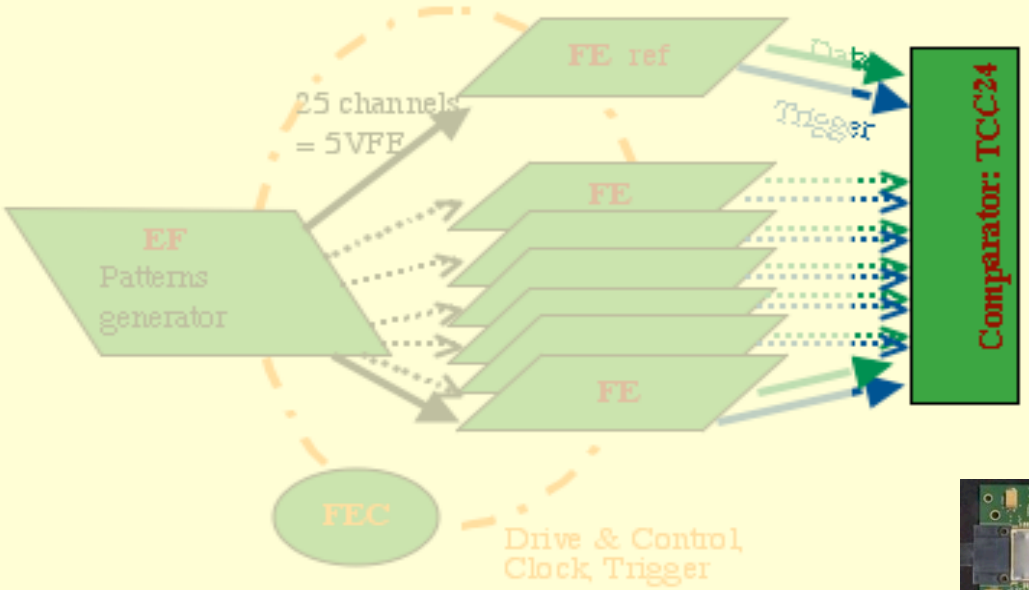
- EF + 2 FE
- 24 layers
- PCB class 6, 4.8 mm

Final version:

- EF + 4 FE
- Strong constraints to avoid cross-talk and caution on timing of signals ⇒ 400 traces with characteristic impedance 50 Ω
- PCB class 6, 4.8mm, 48cm x 35cm
- Expected by october



XFEST: 3) Comparator: TCC24



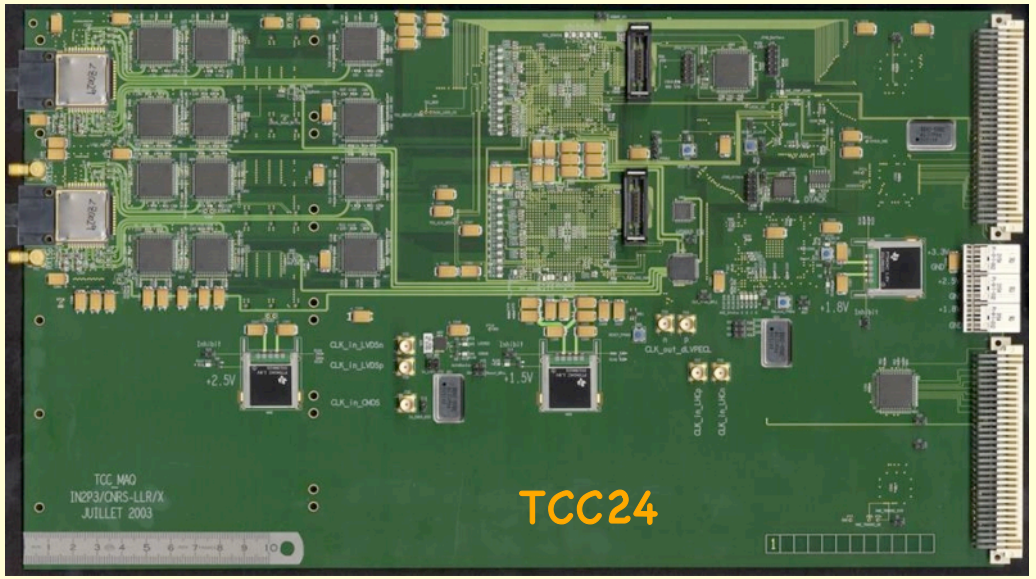
In CMS:
- FE trigger → TCC board
- FE Data → DCC board

In XFEST:
- FE trigger+Data → TCC board

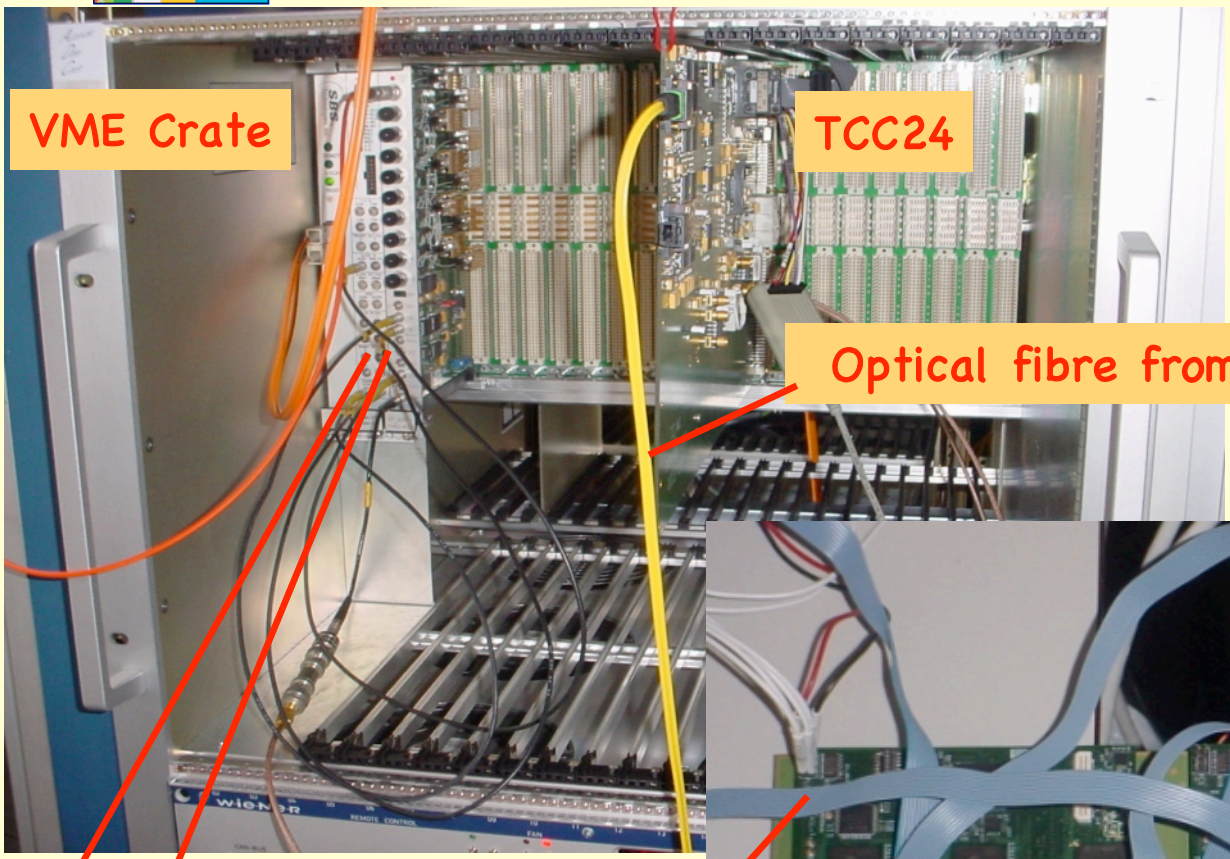
⇒ need reprogramming of TCC

⇒ Use VME6U TCC24 prototype
(see later on for details)

Reprogramming allows:
- comparison of an input signal (1 FE) to other inputs
- If discrepancy, send channels in error to VME

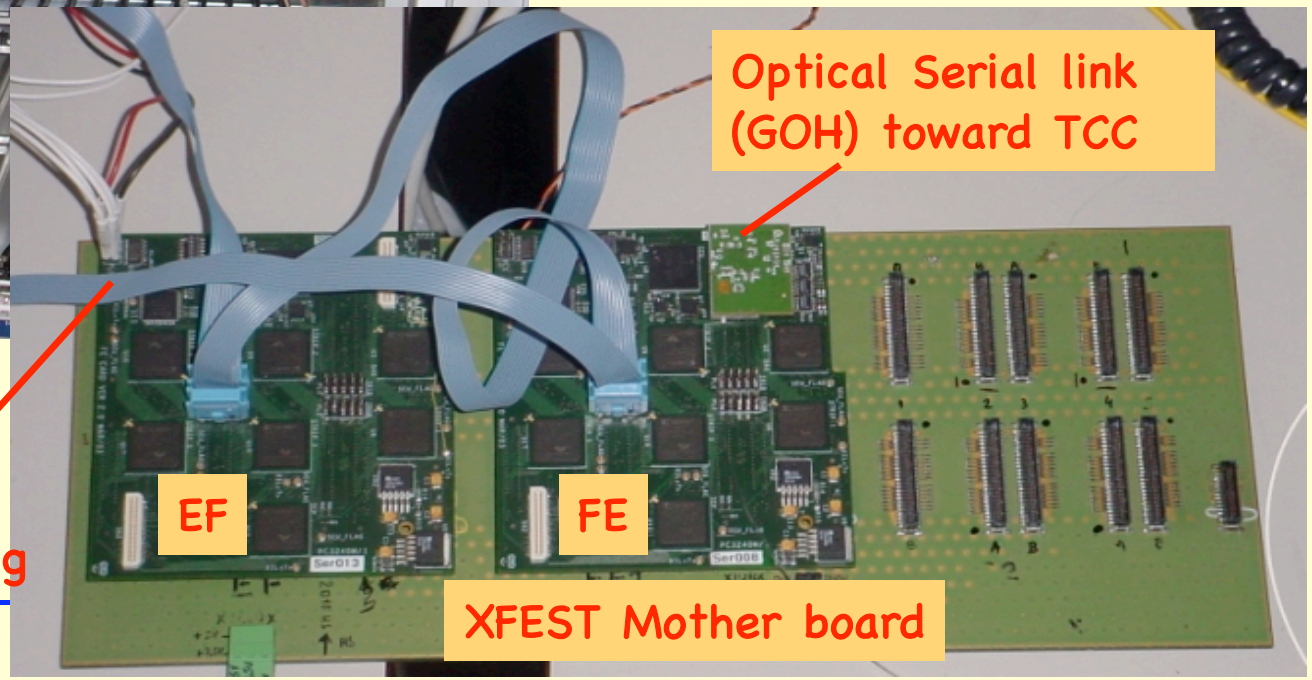


XFEST SetUp



Test bench controlled by a single PC running linux:

VME crate via XDAQ/HAL environment, FEC (token ring), RS232, GUI



TTCvi : clock, trigger (elec.)

TTCex : elec. → opt.

FEC (PCI) → Token Ring

The Trigger Concentrator Card

Brief overview of the Trigger Concentrator Card (TCC)

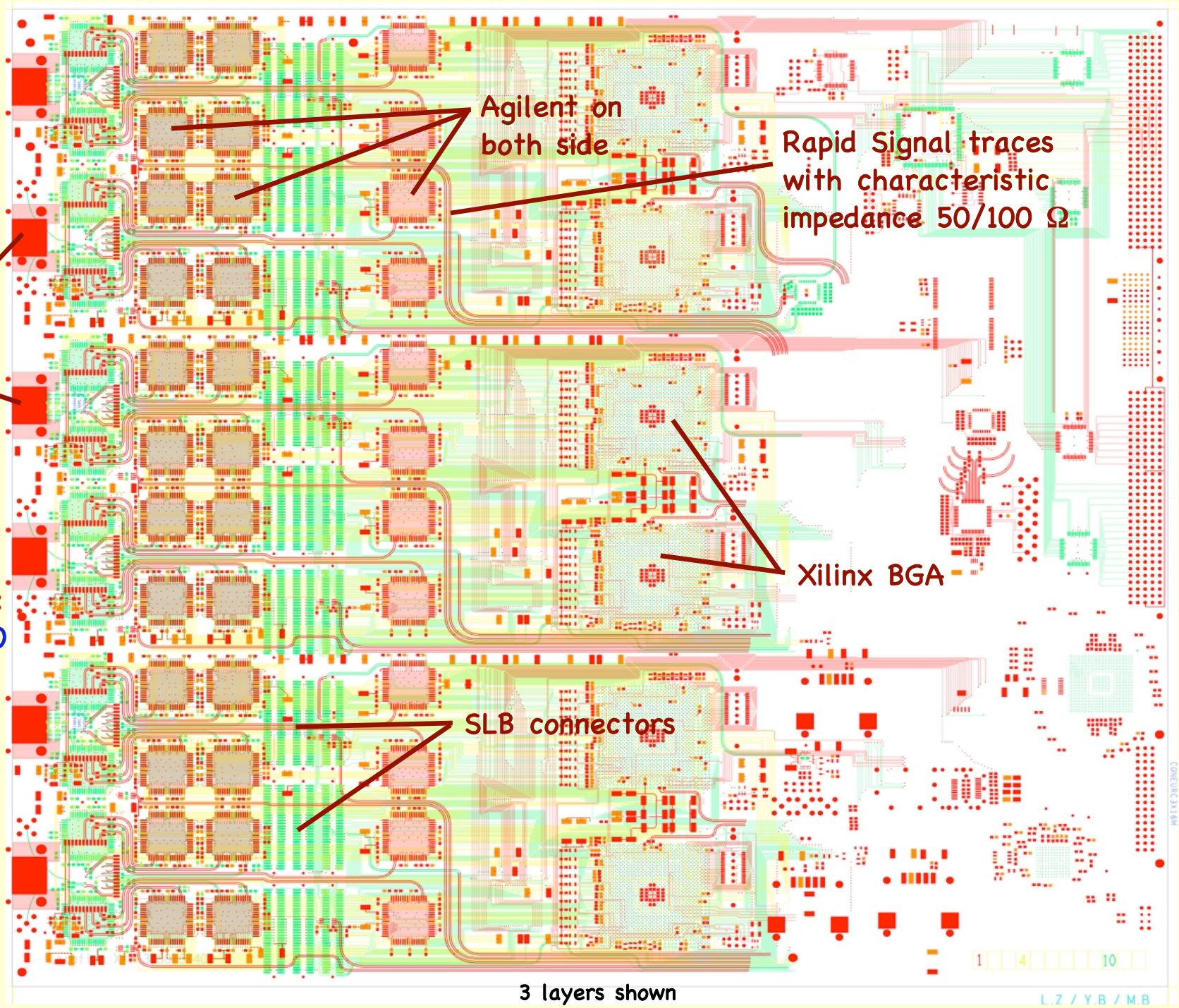
TCC Functions :

- Receives and deserializes the (optical) data from FE
- Finalises and encodes the Trigger Primitive (TP) using a non-linear scale for the total transverse energy
- Sends the encoded TP @ 40 MHz to the regional trigger through SLB (assuring time alignment between channels, see N. Almeida talk tomorrow)
- Stores the encoded TP during L1 latency and transmits it to DCC when L1A
- Computes TTF (= Trigger Tower Flags): Classifies trigger towers into high/medium/low interest and sends it to SRP when L1A

TCC in numbers (barrel version) :

- double width VME 9U module managing 72 channels (=68 trigger towers + 4 not used) ⇒ 1 whole supermodule
- Basic Components : 6 NGKs (O/E receivers 12 channels), 72 Agilent (deserializer) and 8 FPGAs (6 Xilinx virtex2, 1 Xilinx virtex2 pro, 1 Altera) + 9 SLBs boards
- Latency must be ≤ 7 Clocks ⇒ imposes Agilent choice with protocol CIMT (2.5 clocks)

PCB 10 layers
Class 6 (120 µm)



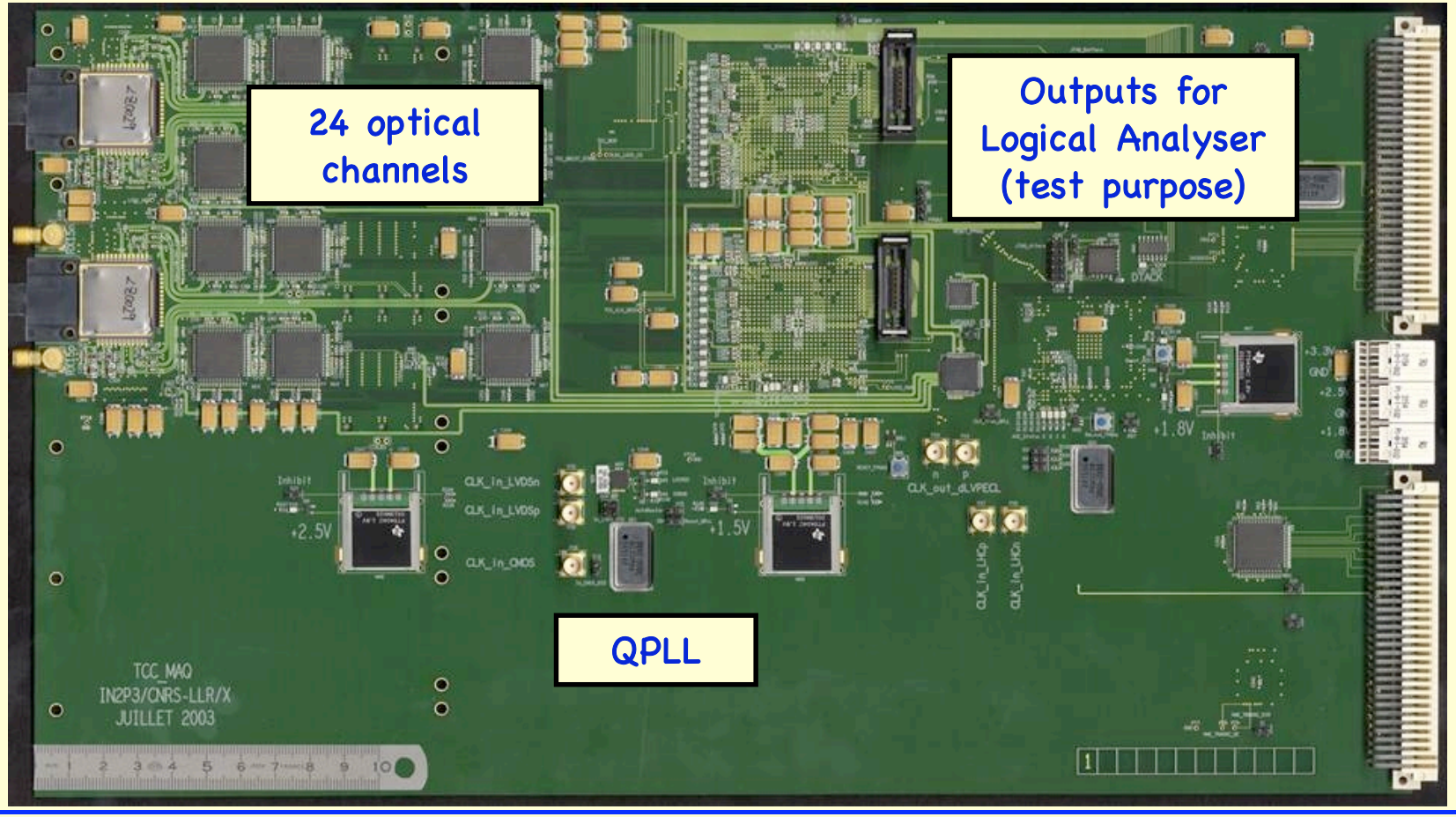
Very high density : use micro-Vias (120 µm drilled by laser) and BGA components

3 layers shown

TCC24: Prototype top view

Aims : validate the design/implementation: Agilent deserializers, μ-vias, BGA

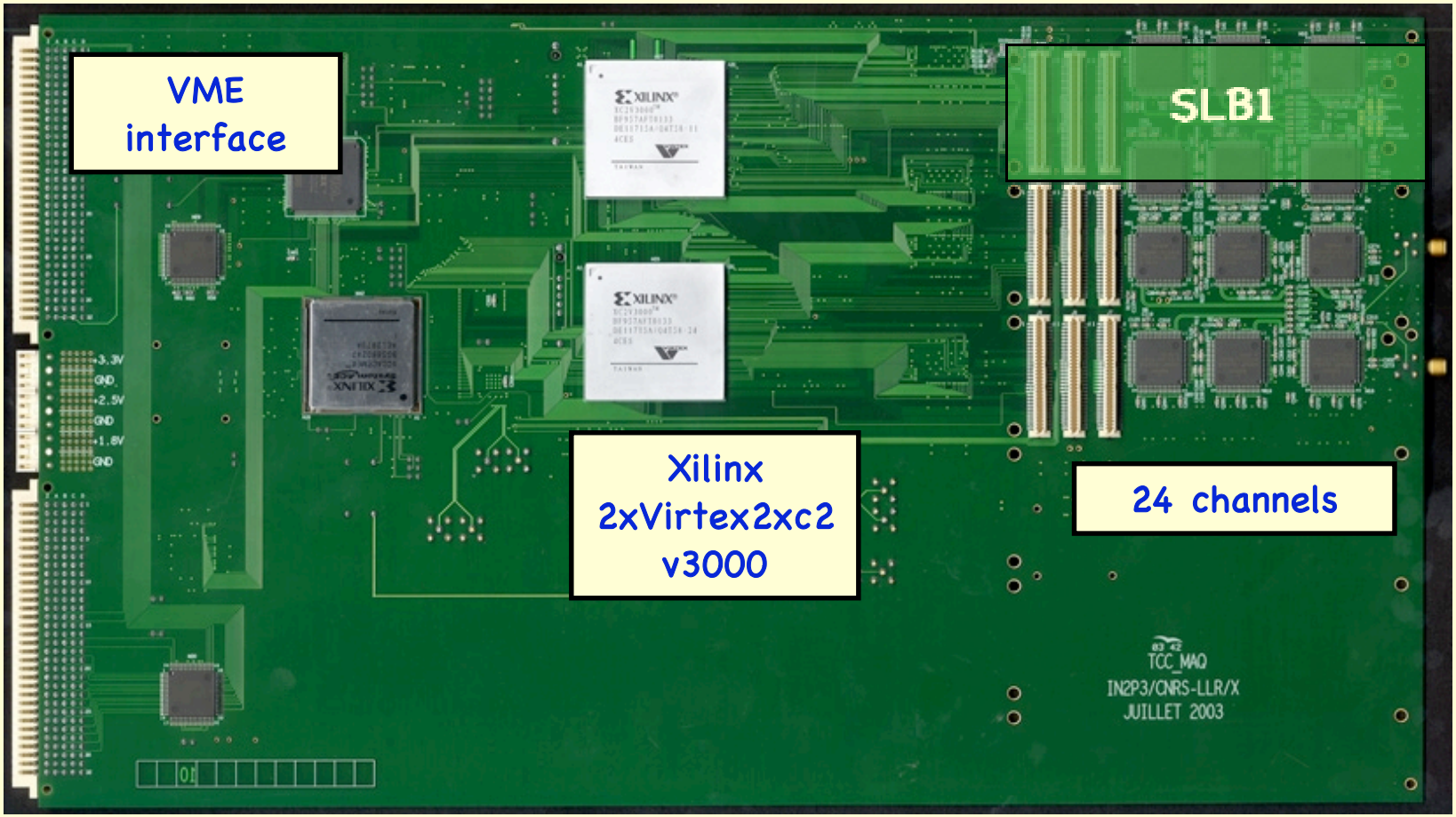
TCC24 : VME 6U board, 24 channels 1/3 of final version



TCC24: Prototype bottom view

Aims : validate the design/implementation: Agilent deserializers, μ-vias, BGA

TCC24 : VME 6U board, 24 channels 1/3 of final version

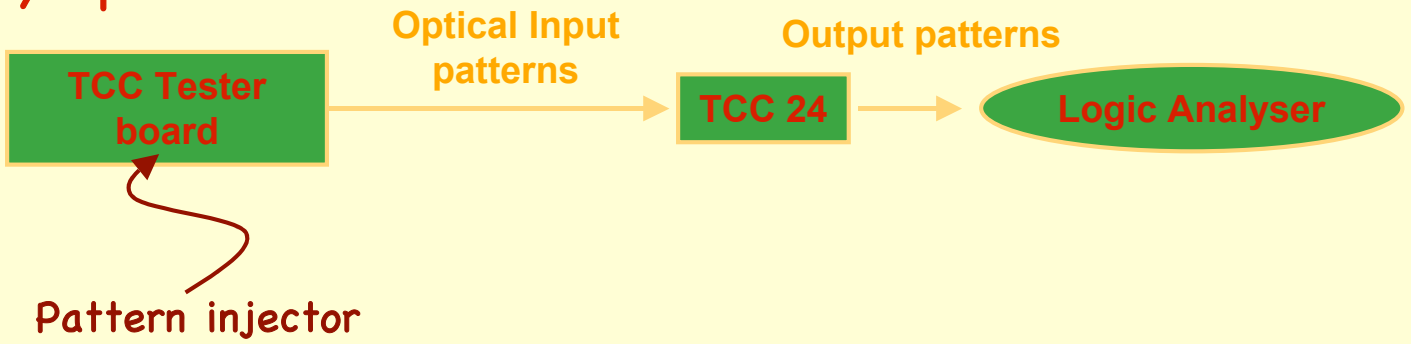


Tests of TCC24

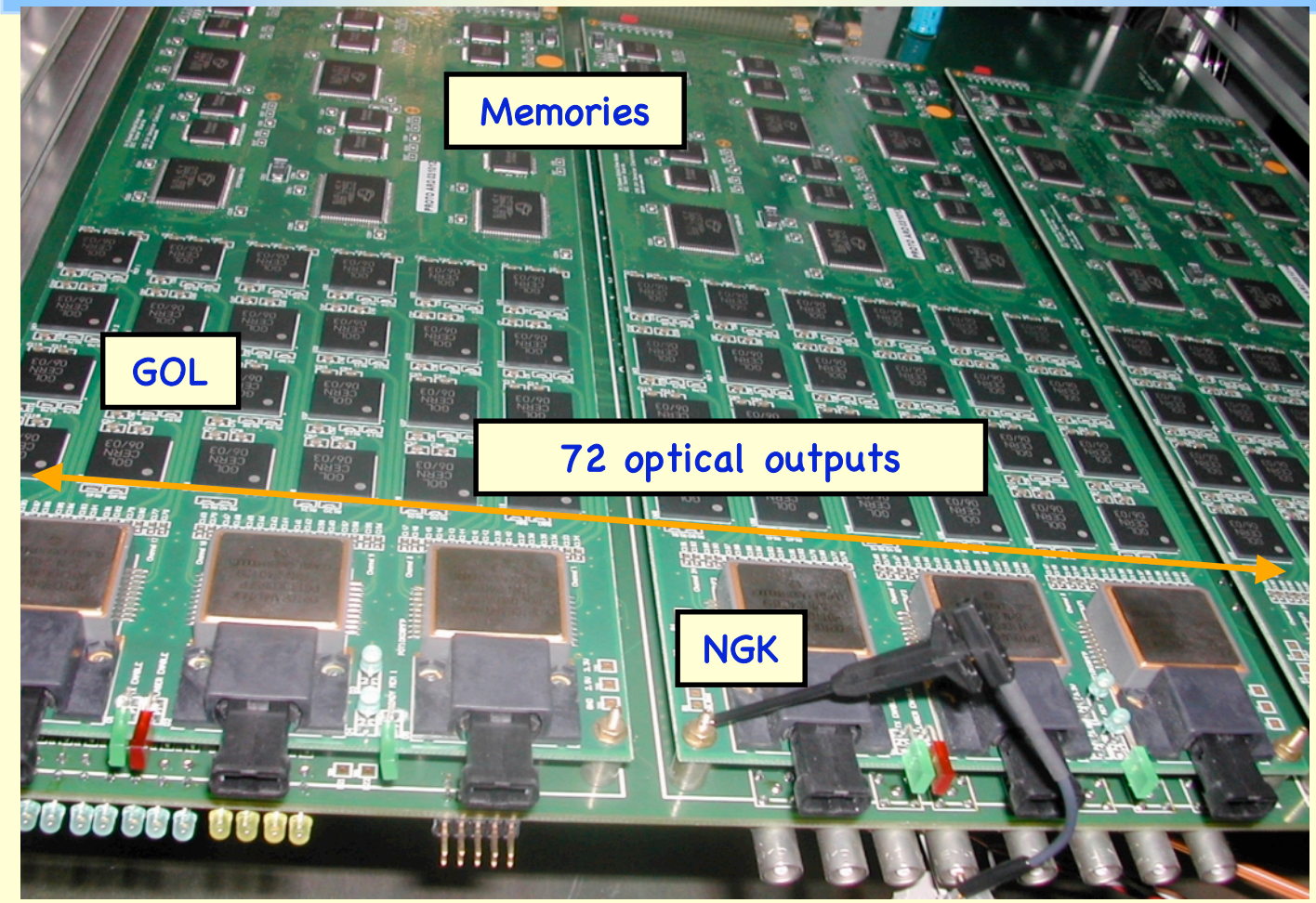
Tests performed :

1. Power consumption measurement *(not shown in this talk)*
2. Latency measurements *(not shown in this talk)* : ≤ 6 clock unit (< requirement)
3. Bit Error Rate measurements
    1. Direct measurement
    2. Indirect measurements :
        1. Eye diagram
        2. Jitter

Basic Synoptic :



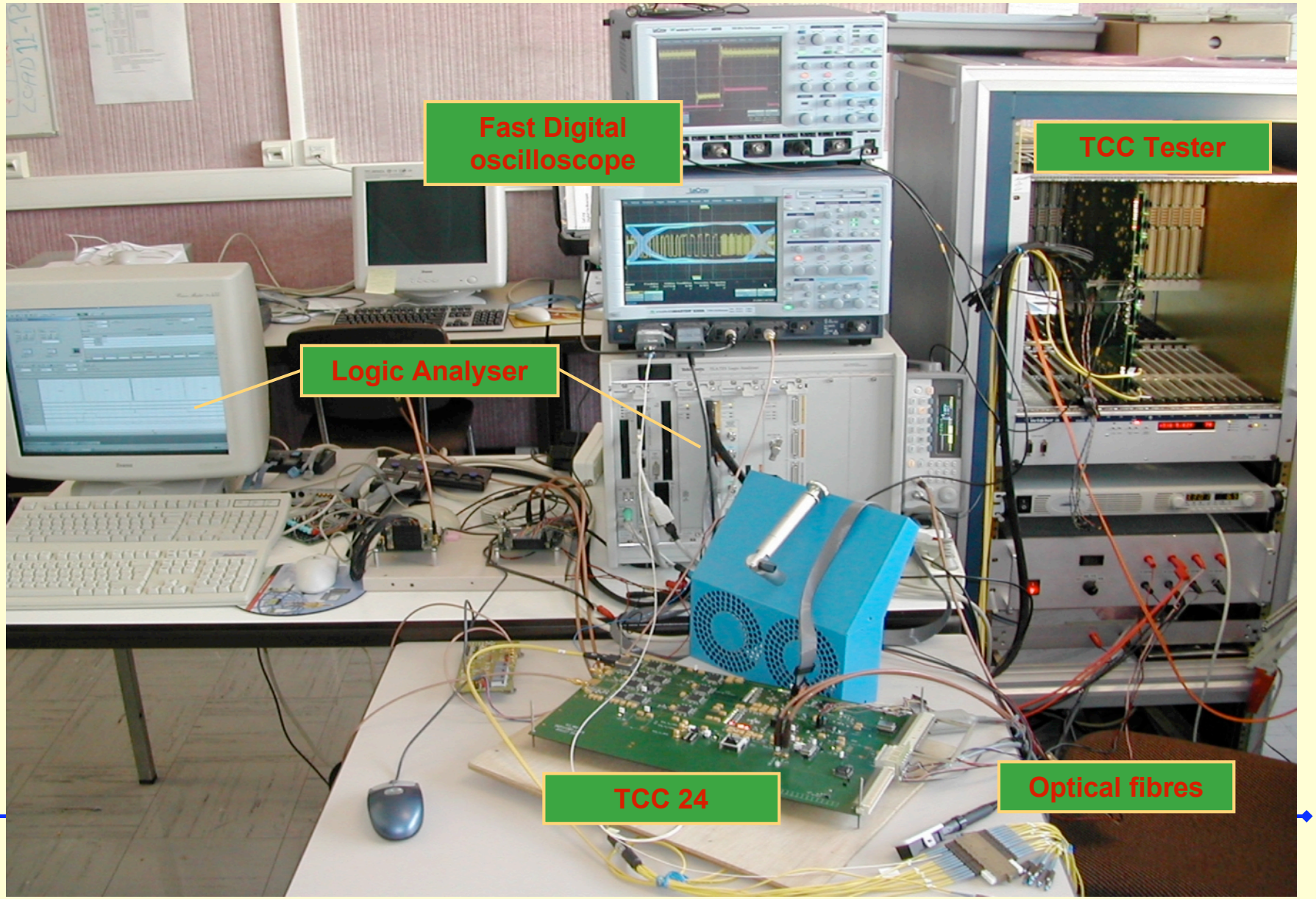
Tests of TCC24: TCCTester board



TCC Tester will be used for production test bench

- TCC Tester = clone of the DCC Tester (see J. C. Da Silva talk for details)
- Able to transmit loaded pattern (in memories) @ 40 MHz

Tests of TCC24: setup



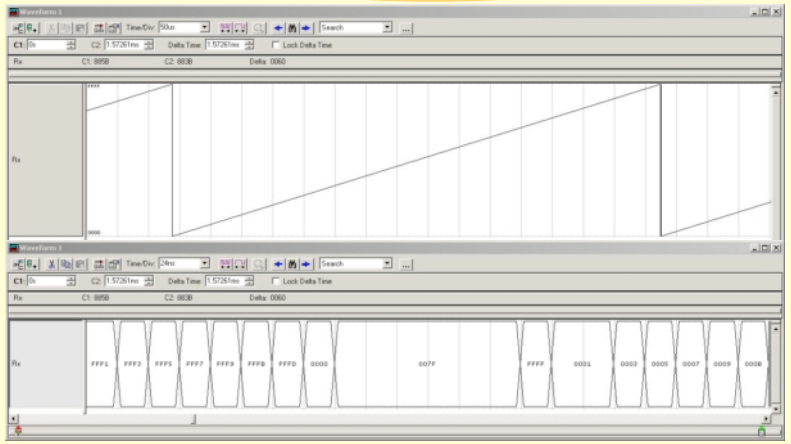
Tests of TCC24: BER direct measurement

TCC Tester

24 Optical Inputs
(patterns = counter)

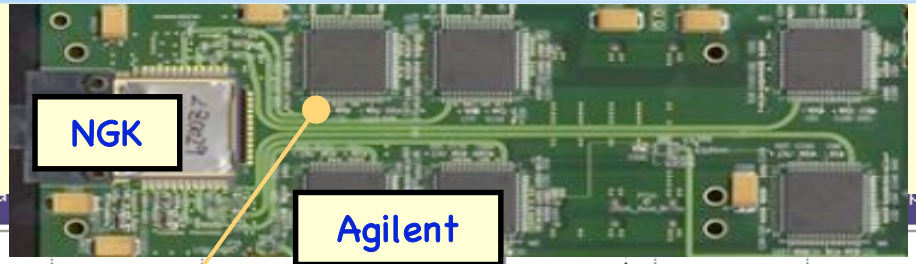
TCC 24 with FPGA doing the comparison with the expected pattern on-line
If discrepancy, error sent to Logic Analyser

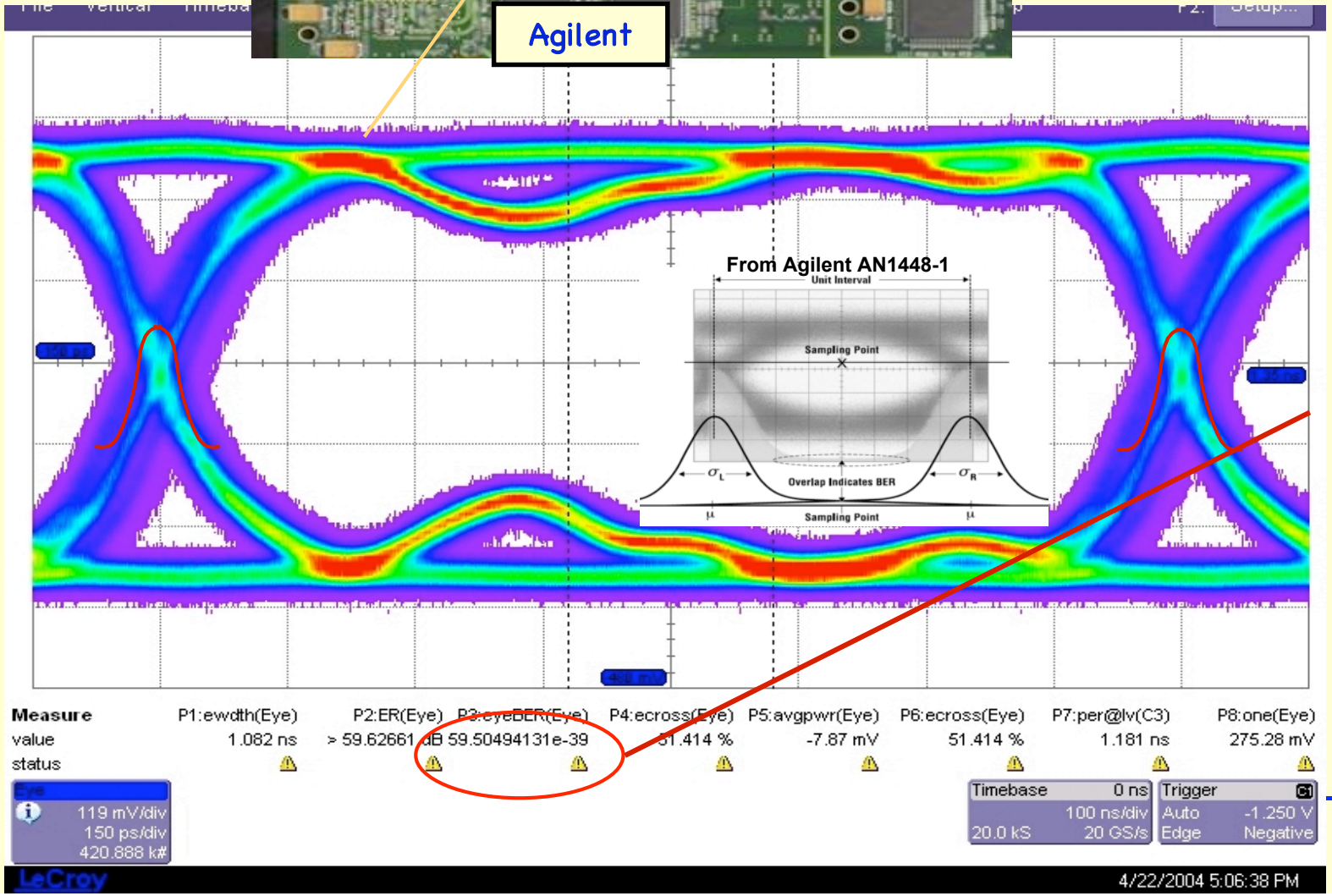
Logic Analyser
Counts number of error



1. Test continuously 1 channel during 145h (6 days) @ 40 MHz with 0 error ⇒ BER < 3.10^{-15} ⇒ less than 1 error every 1'35" in CMS
2. Test 18 channels (/24) in parallel (same pattern injected in every channel): no error during 16h10' @ 40 MHz ⇒ BER < 2.10^{-14}

Tests of TCC24: BER and Eye diagram





Eye wide open

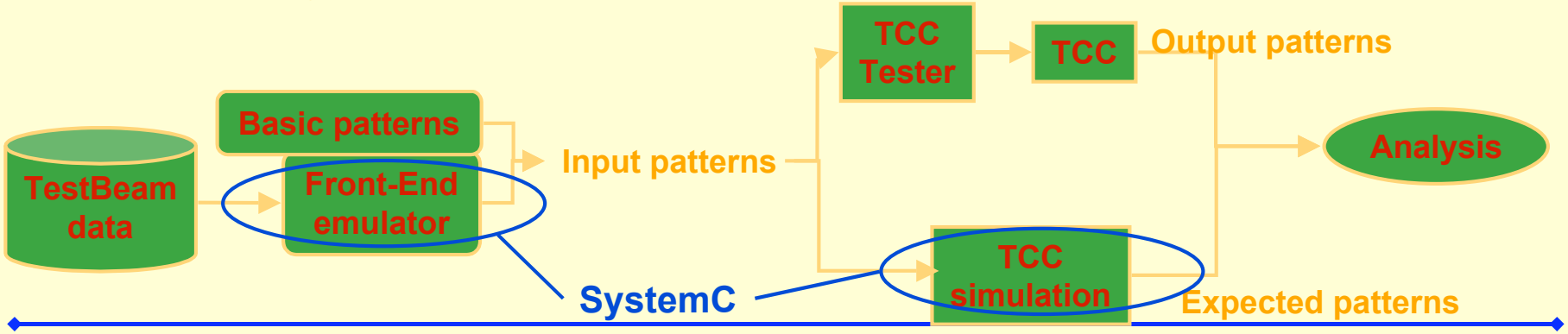
Can expect very low BER !

TCC Tests for production

First TCC barrel in october 2004, pre-production beginning of 2005, 42 boards (barrel version) to produce/test in second half of 2005

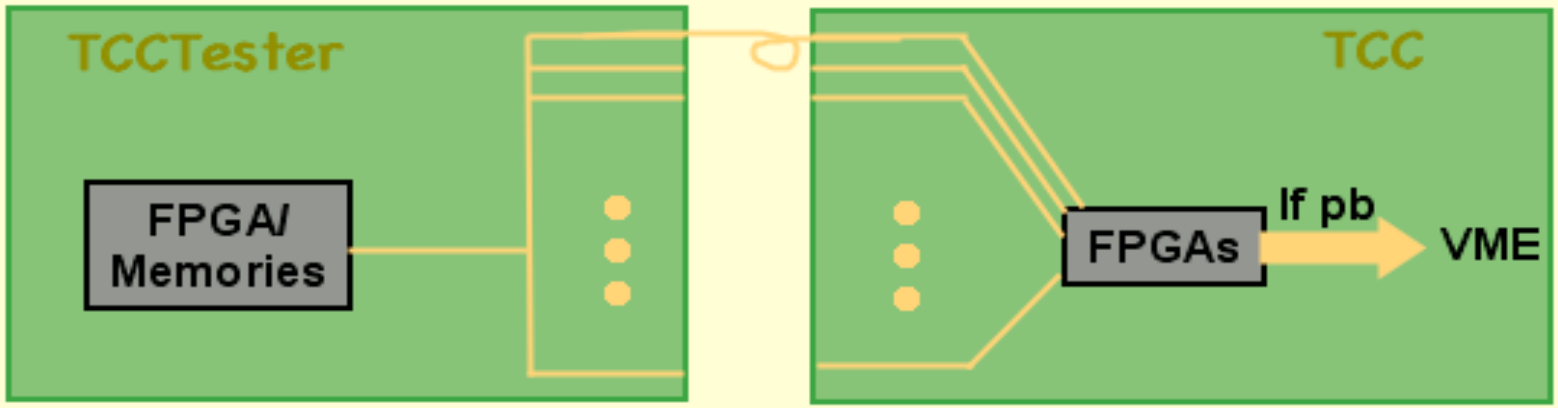
1. JTAG for boundary scan (up to SLB boards)
2. Built-in self test ⇒ check firmware:
   1. patterns auto generated by TCC
   2. Comparison to expected data in ROM
3. Short tests (fraction of seconds @40 MHz):
   1. Inject patterns (coming from testbeam, counter etc)
   2. Compare output to SystemC simulation (detailed hardware simulation, see http://www.systemc.org for details)

   ⇒ Uses Logic Analyser to read out/store output data



TCC Tests for production

4. Long tests (several hours/days):
    1. Inject
        1. pseudo-random patterns auto generated by TCCTester
        2. patterns loaded in TCCTester memories
    2. Same patterns injected in <u>all channels</u>
    3. Compare outputs in TCC FPGA itself
    4. Readout/store data only if discrepancy via VME



Conclusion

- Trigger Primitive are generated using 2 boards:
  - Front End board
  - Trigger Concentrator Card

- Both boards need test bench to validate the up-coming production

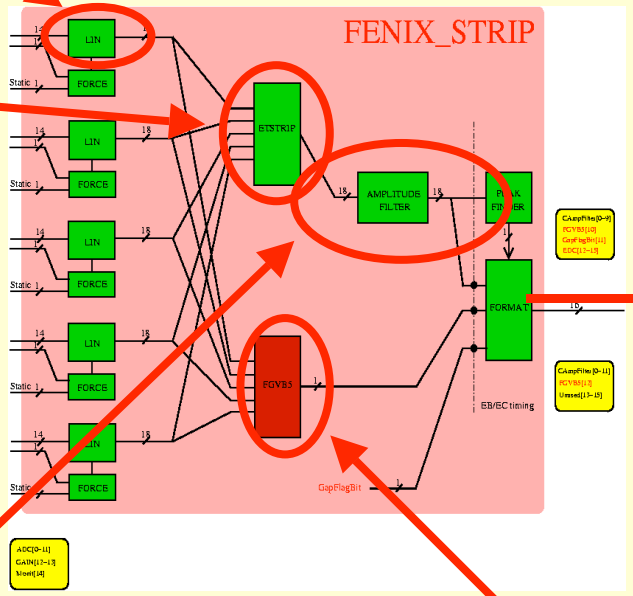
- Coherent test benches have been developed using same approach (XDAQ/HAL environment for VME, SystemC etc...) and even same hardware if possible

Back-up slides

FENIX block diagram for Trigger Primitives

linearization
from 12+2 to 18

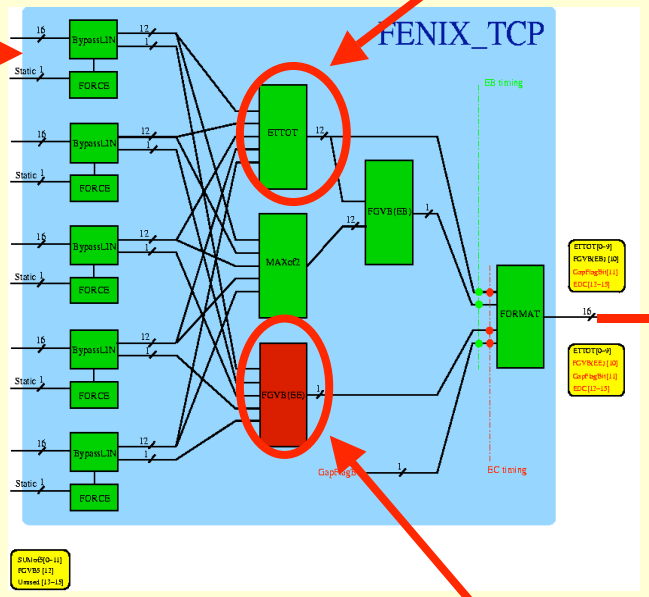
strip or
pseudo
strip
signal



BCID FIR filter +
Peak Finder

Fine Grain
Veto Bit

total E_T



TCC

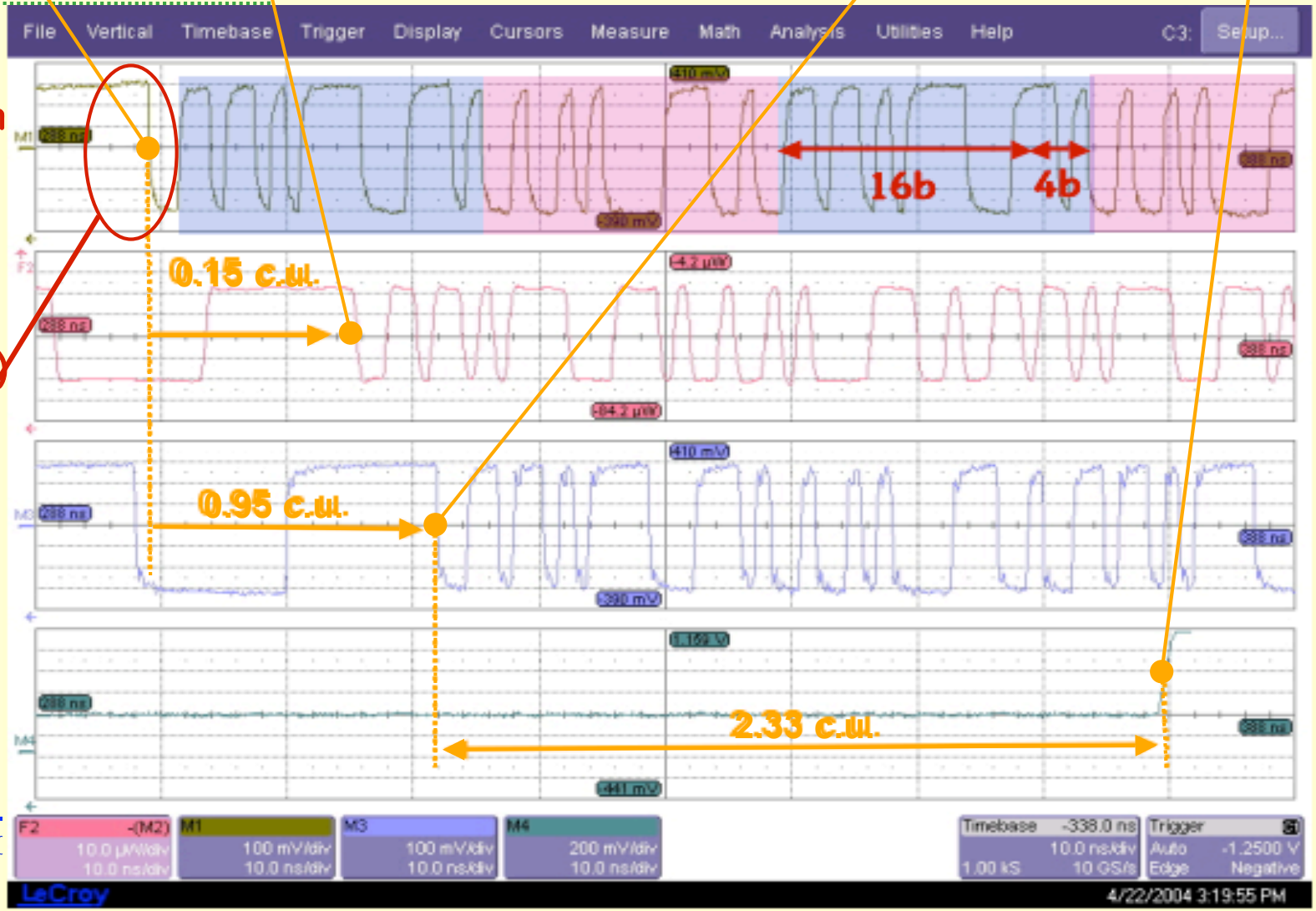
Fine Grain
Veto Bit

Tests of TCC24: Latency 1.

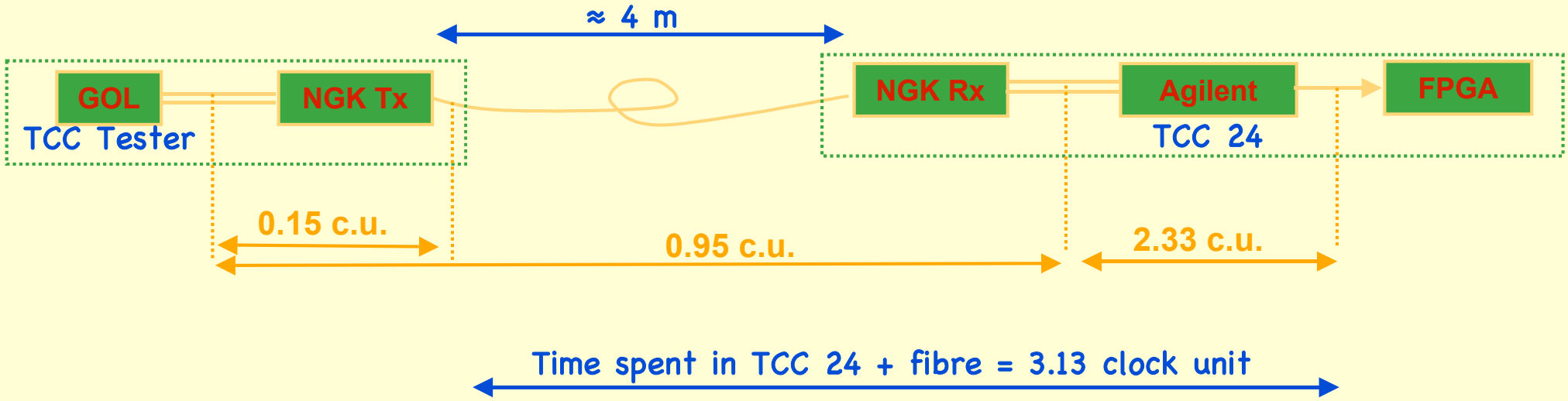
GOL
NGK Tx
TCC Tester
NGK Rx
Agilent
FPGA
TCC 24

Signal clean ⇒ Able to decode the word (8FB5 and $\overline{8FB5}$, LSB on left)

Master transition (CIMT): 1100



Tests of TCC24: Latency 2.



Latency: considering 2 c.u in FPGA + alignment ⇒ ≤ 6 clock unit
(< requirement)