

# ***Nanometers, Gigahertz, and Femtoseconds***

***Recent Progress in Field Programmable Gate Arrays***

Peter Alfke  
Xilinx, Inc  
[peter.alfke@xilinx.com](mailto:peter.alfke@xilinx.com)



# ***FPGA State of the Art 2004***

- **90-nanometer** manufacturing technology
- **Ten Gigahertz** serial I/O (SerDes) in silicon
- **0.07 femtosecond**  
asynchronous data capture window  
causes 1.5 ns metastable delay



# ***Three Sections:***

- 1. Bird's Eye View of FPGA Technology**
- 2. FPGAs in 2004: Virtex-4 Introduction**
- 3. Special Problems and Solutions**

*all in 45 minutes...*



# ***A Bird's Eye View...***

## **Lower Cost**

Moore's Law is alive

Smaller geometries and larger wafers  
and lower defect density (=higher yield )  
continue to achieve lower cost per function

LUT + flip-flop: \$1.- in 1990, \$ 0.002 in 2003

State-of-the-art: 90 nm on 300 mm wafers

Spartan-3 uses this technology for lowest cost

***Rapid price reductions, intense competition***



# ***A Bird's Eye View...***

## **More Logic and Better Features:**

- >100,000 LUTs & flip-flops

  - >200 BlockRAMs, and same number 18 x 18 multipliers

- 1156 pins (balls) with >800 GP I/O

  - 50 I/O standards, incl. LVDs with internal termination

- 16 low-skew global clock lines

  - Multiple clock management circuits

- On-chip microprocessor(s) and Gbps transceivers

***Gate count is really a meaningless metric***



# *A Bird's Eye View...*

## Higher Speed

Smaller and faster transistors

90 nm technology, using 193 nm ultra-violet light

Cu interconnect ( instead of Al ) was easily achieved

Low-K dielectric progress is disappointing

**System speed:** up to 500 MHz,

Mainly through smart interconnects, clock management,  
dedicated circuits, flexible I/O.

Integrated transceivers running at **10 Gigabits/sec**

*Speeding up general-purpose logic is getting difficult*



# *A Bird's Eye View...*

## **Better tools**

**Back-End** Place&Route and XST synthesis

VHDL and Verilog becoming entry point

**IP/Cores** speed up design and verification

**Embedded** Software Development Tools

support architectures and merge HW and SW

**Domain-Specific Languages**

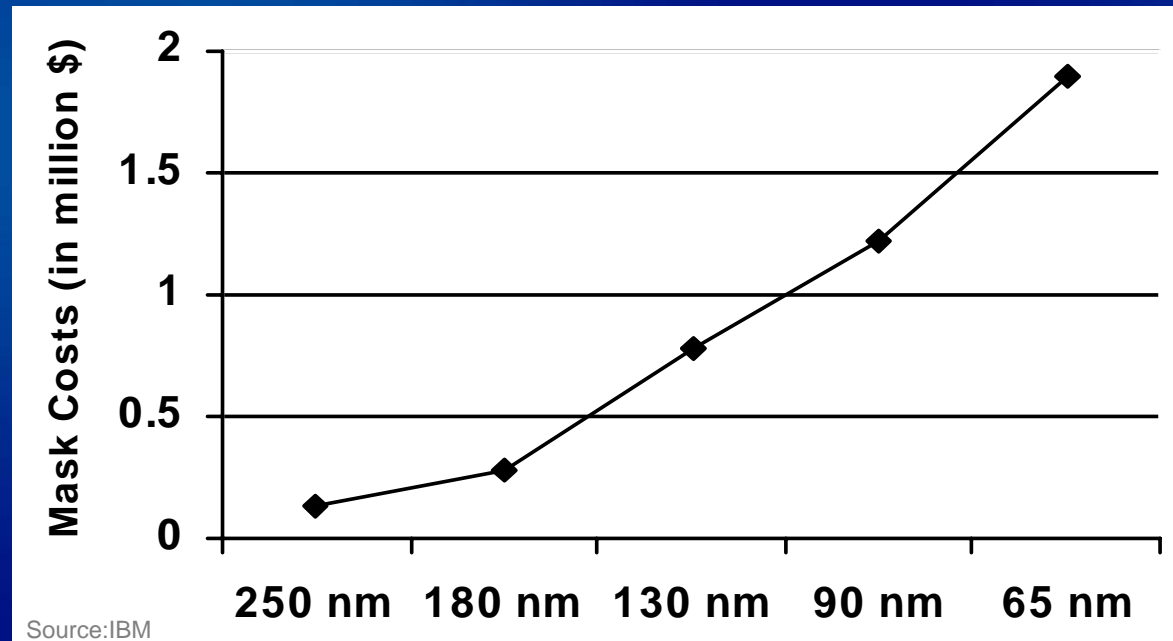
System Generator bridges the gap between  
Matlab/Simulink and FPGA circuit description

*ASIC-size FPGAs need ASIC-like tools*



# *ASICs Are Losing Ground*

Mask set >\$1M + design + verification + risk



*ASICs are only for extreme designs:  
Extreme volume, speed, size, low power*





# Evolution

	1965	1980	1995	2010(?)
Max Clock Rate (MHz)	1	10	100	1000
Min IC Geometries ( $\mu$ )	-	5	0.5	0.05
# of IC Metal Layers	1	2	3	12
PC Board Trace Width ( $\mu$ )	2000	500	100	25
# of PC-Board Layers	1-2	2-4	4-8	10-20

*Every 5 years:*

*System speed doubles, IC geometry shrinks 50%*

*Every 7-8 years:*

*PC-board min trace width shrinks 50%*



# ***The Ever-Shrinking Circuitry***

**Number of LUTs + flip-flops + routing  
that fit on the cross section of a human hair**

- 2000            2 LUTs in Virtex-II (150 nm)
- 2002            3 LUTs in Virtex-IIPro (130 nm)
- 2004            4 LUTs in Virtex-4 (90 nm)
- 2005            *8 LUTs = one CLB in 65 nm*

***Moore's law is alive and well in FPGAs***



# ***Middle-of-the-Road FPGAs***

1990	XC3042	288	LUTs + flip-flops
1994	XC4005	512	LUTs + flip-flops
1998	XC4013XL	1,152	LUTs + flip-flops
2000	XCV300	6,144	LUTs + flip-flops
2002	XC2V1000	10,240	LUTs + flip-flops
2004	XC2VP30	27,382	LUTs + flip-flops
2005	XC4V60-LX	53,248	LUTs + flip-flops

***Same price for each: One day's engineering salary***



# Thirteen Years of Progress

**200x More Logic**

plus memory,  $\mu$ P,  
DSP, MGT

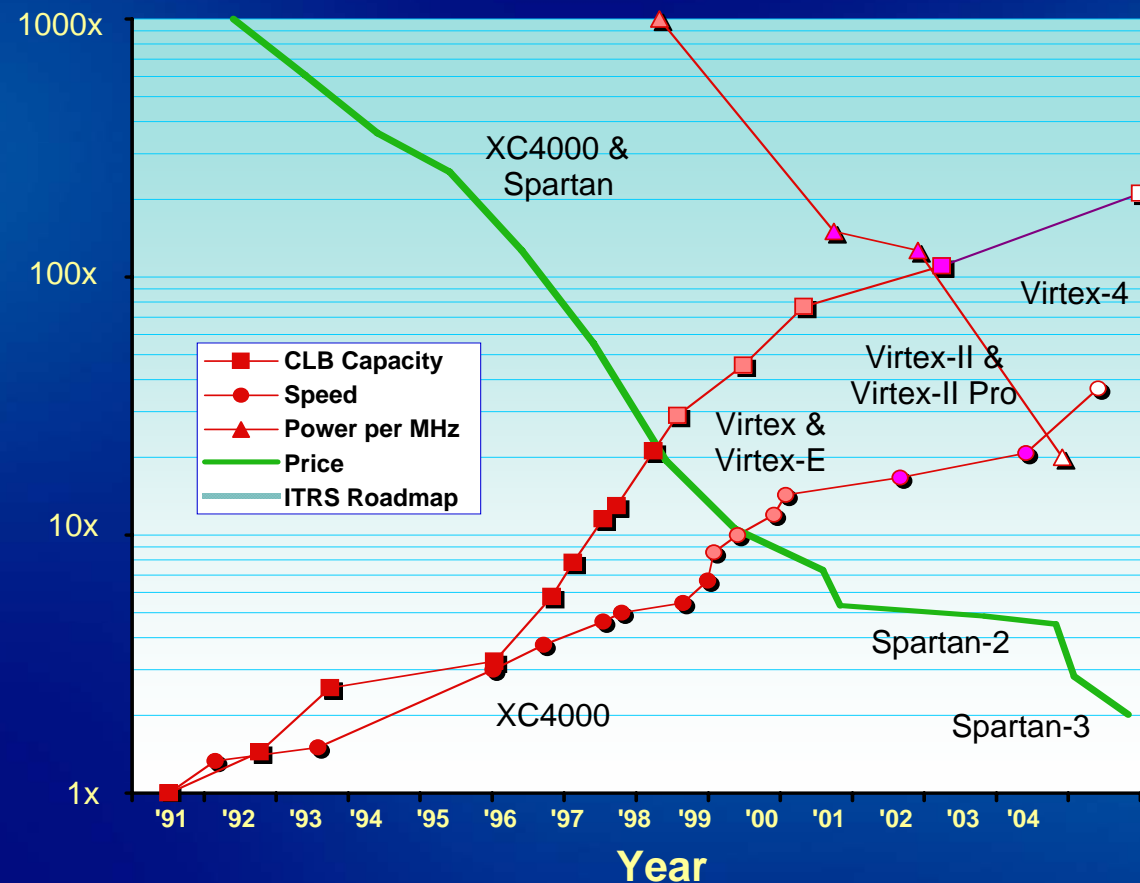
**40x Faster**

**50x Lower Power**

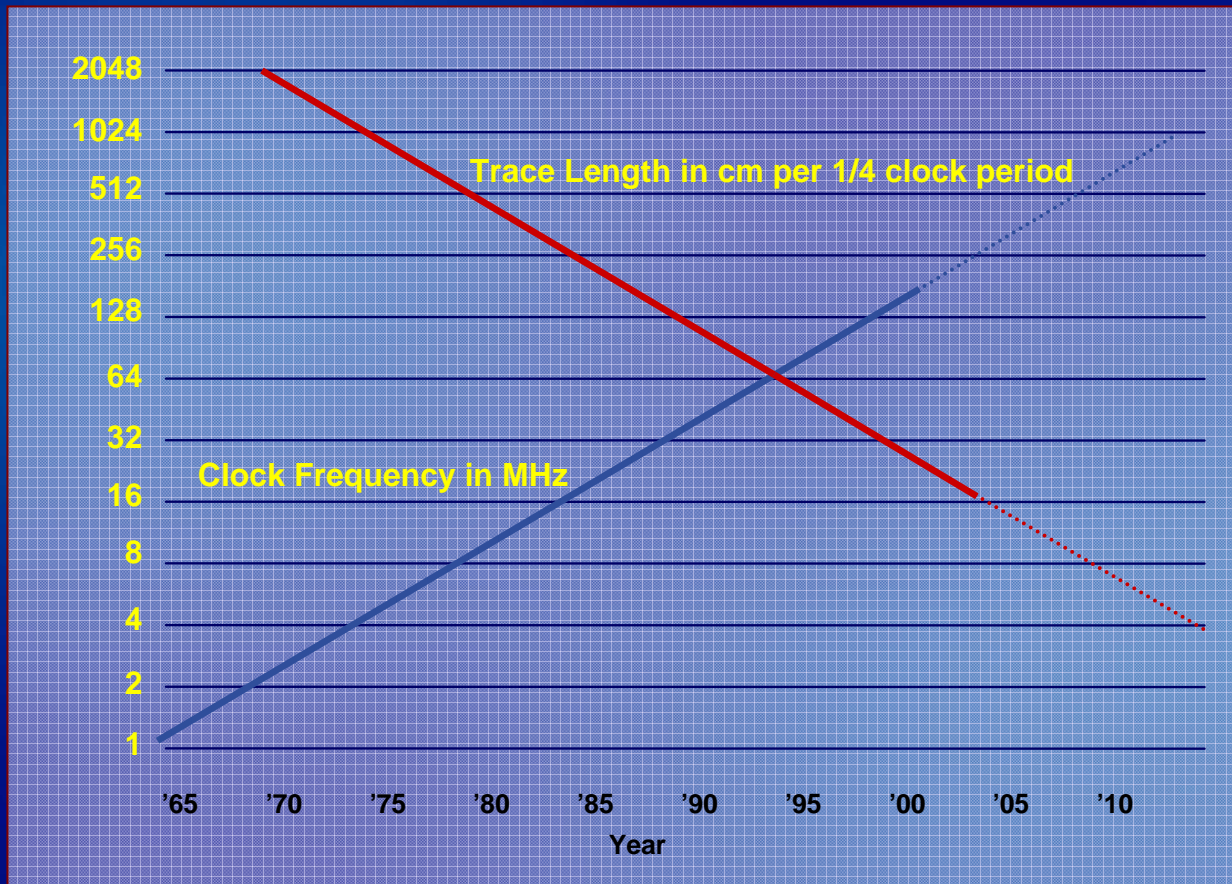
per function x MHz

**500x Lower Cost**

per function



# Moore Meets Einstein



- Speed Doubles Every 5 Years...  
...but the speed of light never changes



# *Higher Leakage Current...*

High Leakage current = static power consumption

Was <100 microamps, now > 100 mA, even amps (!)

Caused by:

- Gate leakage due to 16 Å gate thickness
- Sub-threshold leakage current  
incomplete turn-off because threshold does not scale

**Tyranny of numbers:**

10 nA x 100 million transistors = 1 A

evenly distributed, thus no reliability problem

*Sub-100 nm is **not** ideal for portable designs*



# ***FPGAs in 2003***

1000 to 80,000 LUTs and flip-flops,  
millions of bits in dual-ported RAMs

Low-skew Global Clocks,

Frequency synthesis, 50 ps phase control

18 Kbit BlockRAMs and 18 x 18 multipliers

***FPGAs are not glue-logic anymore***





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# ***FPGAs in 2003***

300+ MHz system clock,

800 MHz I/O

3+ Gigabit transceivers

Embedded hard and soft microprocessors

Design security: Triple-DES encryption

VHDL/Verilog entry, synthesis, auto place and route

***FPGAs are a compelling alternative to ASICs***



# *FPGAs in 2004*



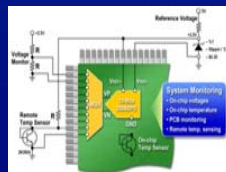
# Virtex-4 in September 2004



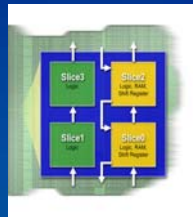
**Integrated 450 MHz PowerPC Cores**



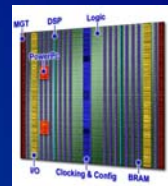
**Integrated Tri-Mode Ethernet MAC Cores**



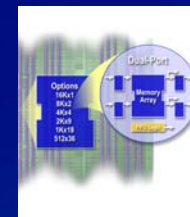
**Integrated System Monitor**



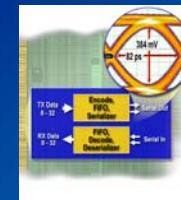
**4th Generation Advanced Logic**



**ASMBL™ Column-Based Architecture**



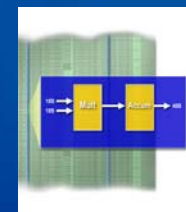
**500 MHz SmartRAM™ BRAM/FIFO**



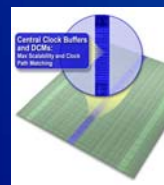
**0.6 - 11.1 Gbps RocketIO™**



**SelectIO with ChipSync™ Technology:**  
- 1 Gbps LVDS  
- 600 Mbps SE



**500 MHz Xtreme DSP™ Slice**



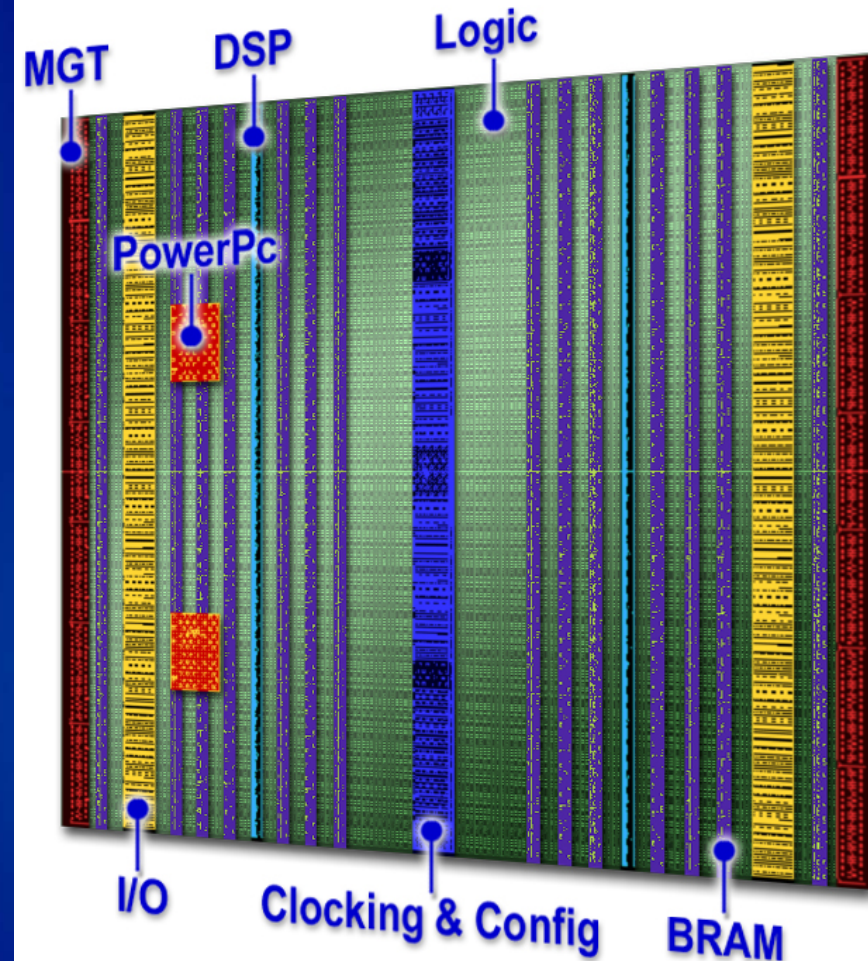
**500 MHz Xesium™ Clocking**





# *New ASMBL™ Columnar Architecture*

- **Enables “Dial-In” Resource Allocation Mix**
  - Logic, DSP, BRAM, I/O, MGT, DCM, PowerPC
- **Made possible by Flip-Chip Packaging**
  - I/O Columns Distributed throughout the Device



# ***FPGA Innovation: Virtex-4***

90 nm technology, triple-oxide, 1.2-V V<sub>ccint</sub> supply

General-purpose I/O up to 1 Gbps,

V<sub>cco</sub>=1.5, 2.5, or 3.3-V

0.6 to 11.2 Gigabit/sec ***RocketI/O*** transceivers

**Advanced Silicon Modular Block architecture**

Three sub-families:

**V4-LX** for logic-intensive applications

**V4-SX** for DSP-intensive applications

**V4-FX** with PPC micros and multi-gigabit transceivers

***Common architecture for diverse applications***



# ***FPGA Innovation: Virtex-4***

- Higher Performance:
  - 500 MHz for all sub-blocks
- More Versatility
  - New innovative functions
- Higher Level of Integration
  - More LUTs, flip-flops, RAMs, multipliers
- Lower Cost
  - Smaller area = lower cost per function
- Lower Power per ( Function times MHz )



# ***FPGA Innovation: Virtex-4***

Flip-chip packaging:

- lower pin-inductance, stiffer Vcc distribution

Lower power per function and MHz

- Triple-oxide gates, multiple thresholds,  
smaller size, lower Vcc, better design

Better clocking, less skew, more flexibility

Better configuration control, partial reconfiguration

Robust configuration cell, SEU tolerant like 130 nm

***Details available now, after Virtex-4 official introduction***



# ***FPGA Innovation: Virtex-4***

## **Improved I/O Flexibility and Performance**

Supports >50 standards, on-chip termination

Source-synchronous and system-synchronous

Serializer/deserializer behind each pin

Programmable delay available for each pin

> 1Gbps SelectI/O on each pin

>10 Gbps transceivers on dedicated pins (-FX family only)

***Source-synchronous I/O improves performance***

***Serial I/O saves pins and pc-board area***





# ***FPGA Innovation: Virtex-4***

Faster logic and memory

- 500+ MHz operation of all on-chip functions

32-bit arithmetic

- 48-bit adders and synchronous loadable counters

Up to 72-bit wide memory

4- to 36-bit wide FIFO control in each BlockRAM

- Operates with fully independent write and read clocks

- Reliable EMPTY and FULL outputs

  - also ALMOST Empty and ALMOST Full

***FIFOs need no fabric resources and no design expertise***



# *Advanced Clocking*

Proper clocking is extremely important  
for performance and reliability

Most design need many global clock lines  
with minimal clock delay and clock skew

**Digital Clock Manager** (DCM) provides:

- Four-phase outputs,

- Frequency multiplication and division

- Fine phase adjustment



# *Advanced I/O*

## **>50 Different Output Standards**

(strength, voltage, input threshold, etc)

multiple parallel output transistors

which are either fully on or fully off,

Nothing is ever analog, except in LVDS

## **Digitally Controlled Impedance =DCI**

for series-termination of transmission-line drivers

Adjusts up/down strength to be = external resistor

One external pull-up and pull-down resistor per bank

V2Pro and Virtex-4 can “update-only-if-necessary”



# *System Synchronous*

- System-Synchronous when the clock arrives “simultaneously” at all chips  
typically used below 200 MHz clock rate
- On-chip clock distribution DCM  
Zero clock delay controls set-up time,  
and avoids hold time requirements

*The traditional design methodology*



# *Source Synchronous*

Each data bus has its own clock trace  
typically used at 200 to 800 MHz clock rate

On-chip clock-distribution DCM

centers the clock in the data eye

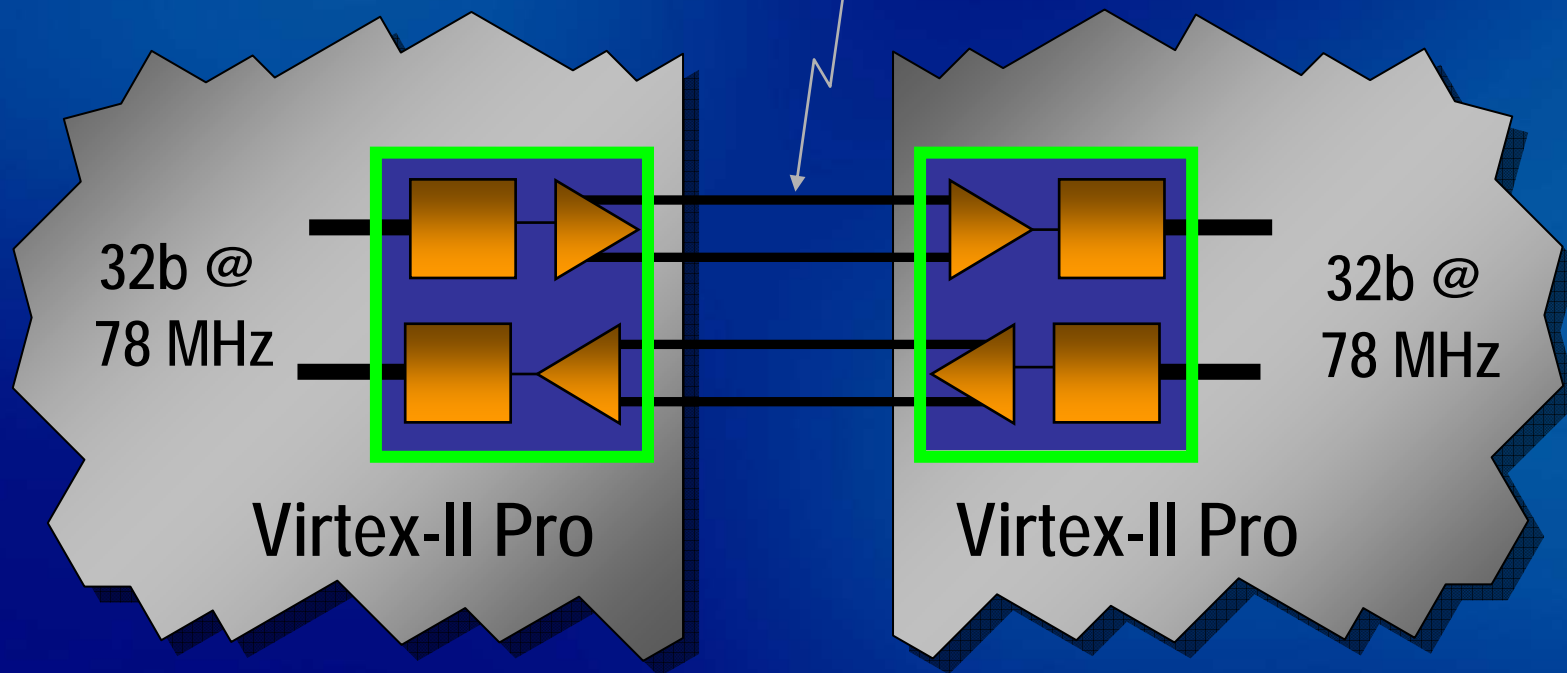
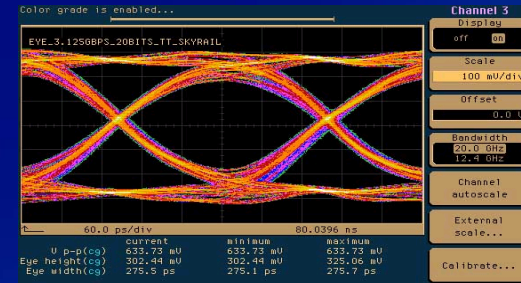
Adds more unidirectional-only clock lines

*The only way above 300 MHz*



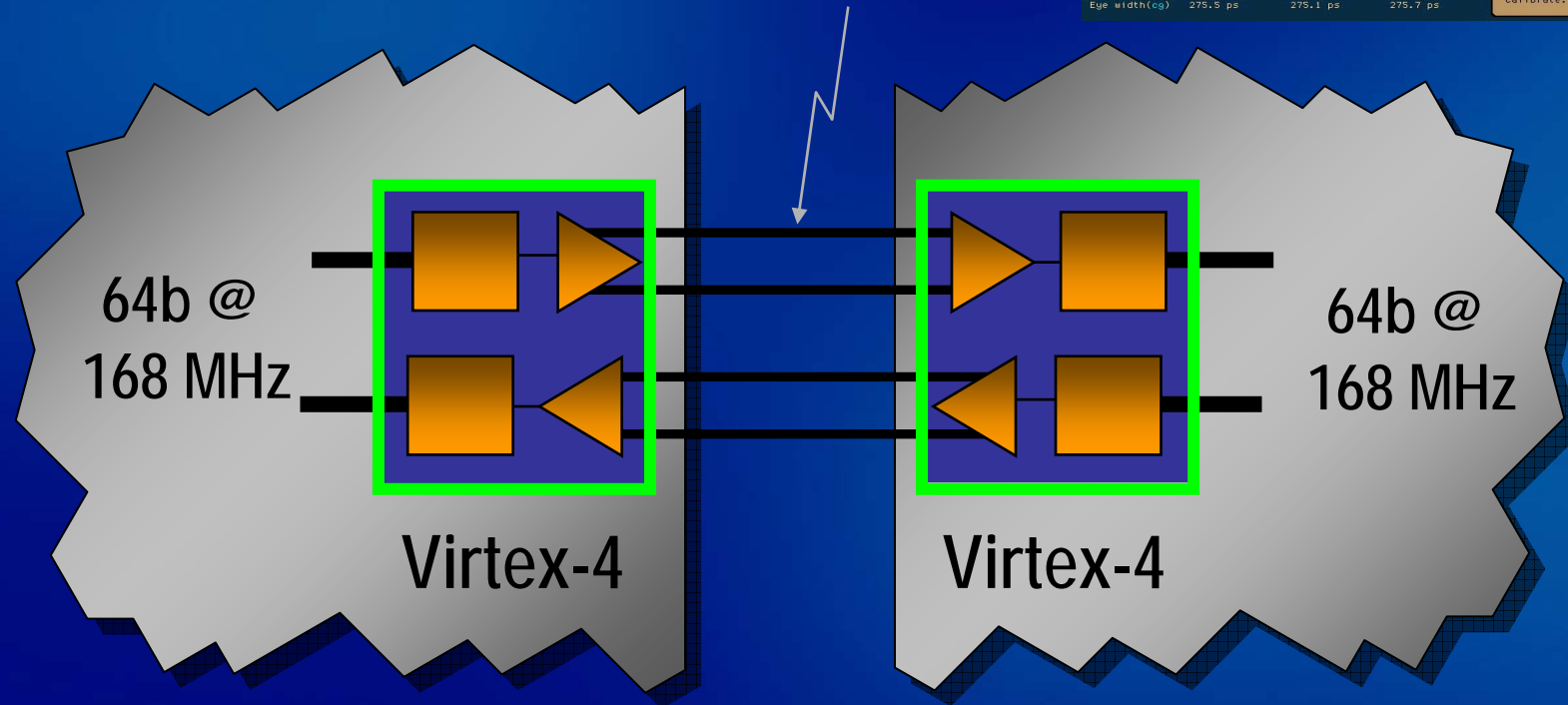
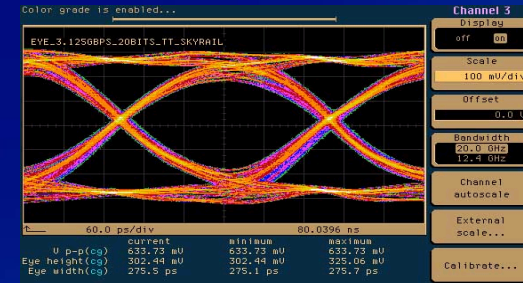
# Serial Transceiver Technology

*3.125 Gbps  
over each pair*



# Serial Transceiver Technology

*Up to 11.1 Gbps  
over each pair*



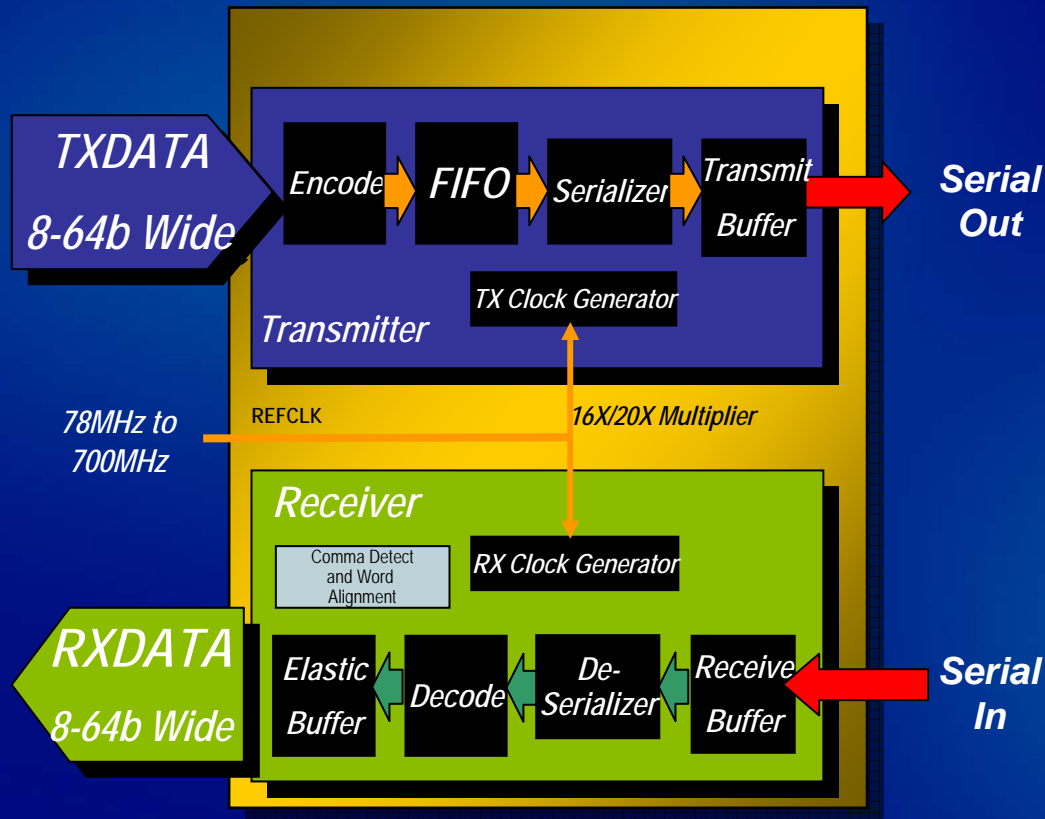


# RocketIO™

## Multi-Gigabit Transceiver

8 to 24 per device

622 Mb/s – 11.1 Gb/s



### Programmable Features:

- 64b/66b or 8b/10b EnDec
- Comma Detect
- Rx and Tx FIFO
- Pre-Emphasis
- Receiver Equalization
- Output Swing
- On-Chip Termination
- Channel bonding
- AC & DC Coupling





# ***Virtex-4 Capabilities***

- Any type of design runs at >400 MHz
- Pipelining provides extra performance “for free”
- Synchronous is best, but 32 clock are available
- Gigabit serial saves pins and board area
- On-chip termination for board signal integrity
- I/O features support double-data rate operation and source-synchronous design

***Details available now, after Virtex-4 official introduction***



# *Virtex-4 Capabilities*

- Popular functions are hard-wired  
for lower cost, higher performance, and ease-of-use:  
microprocessors, FIFOs, serial I/O, clock management, etc.
- Many pre-tested soft cores are available  
Some are free, some for a fee
- One-hot state machines are preferred  
But MicroBlaze and PicoBlaze may be better
- Massive parallelism enhances DSP,  
Up to 1024 fast two's complement multipliers per chip,  
faster than dedicated DSP chips, but needs system-rethinking



# ***2004 Challenges***

Technology moves rapidly: 130, 90, 65 nm

Multiple Vcc, lower voltage - higher current

Lower Vcc makes decoupling very critical

Moore's law becomes more difficult to sustain

Leakage current has increased significantly

Triple-oxide transistors and clever design provide relief

Signal integrity on pc-boards is crucial

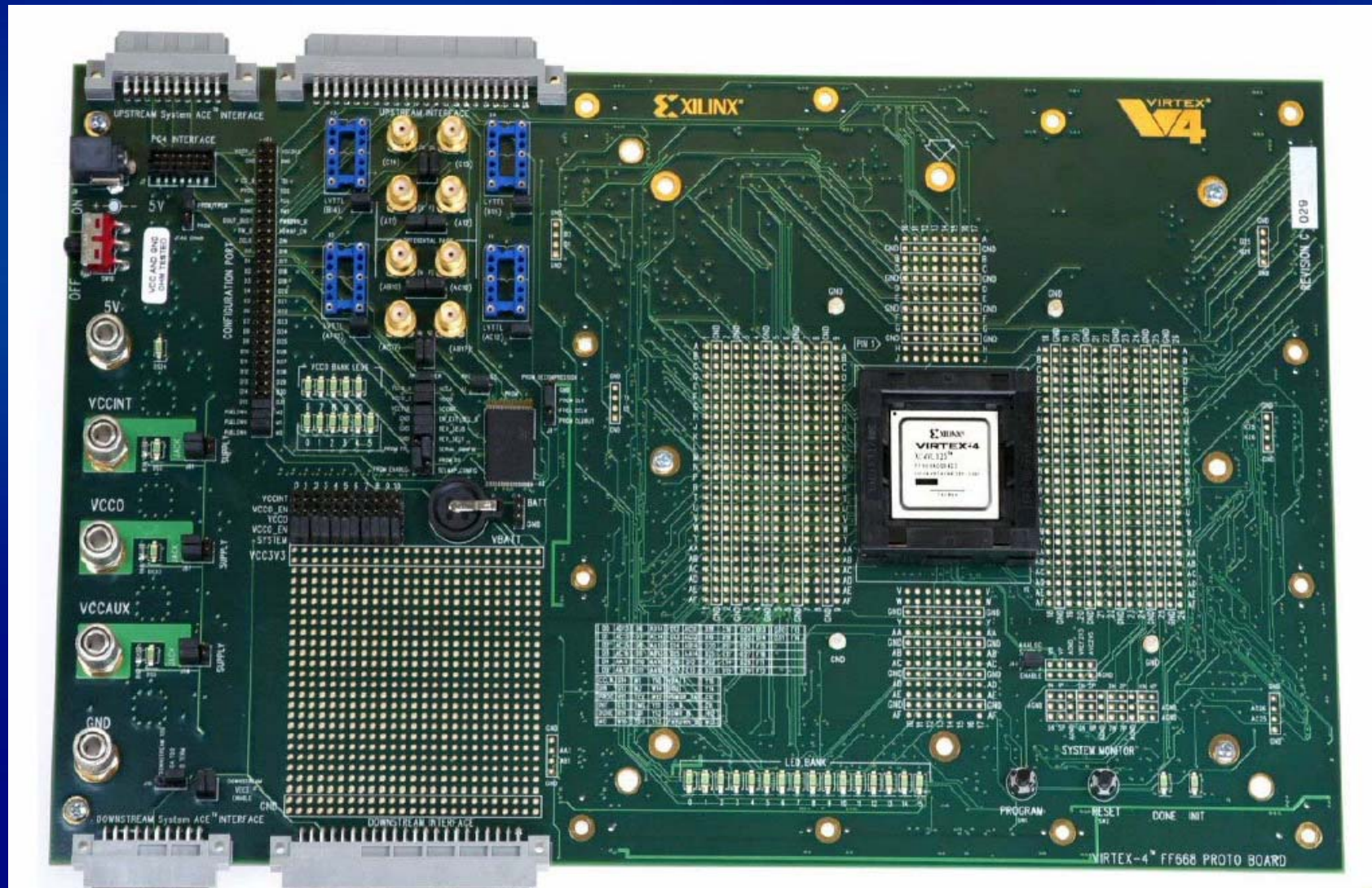
“homebrew” prototyping would waste money and time

***Use Standard Evaluation Boards Instead***



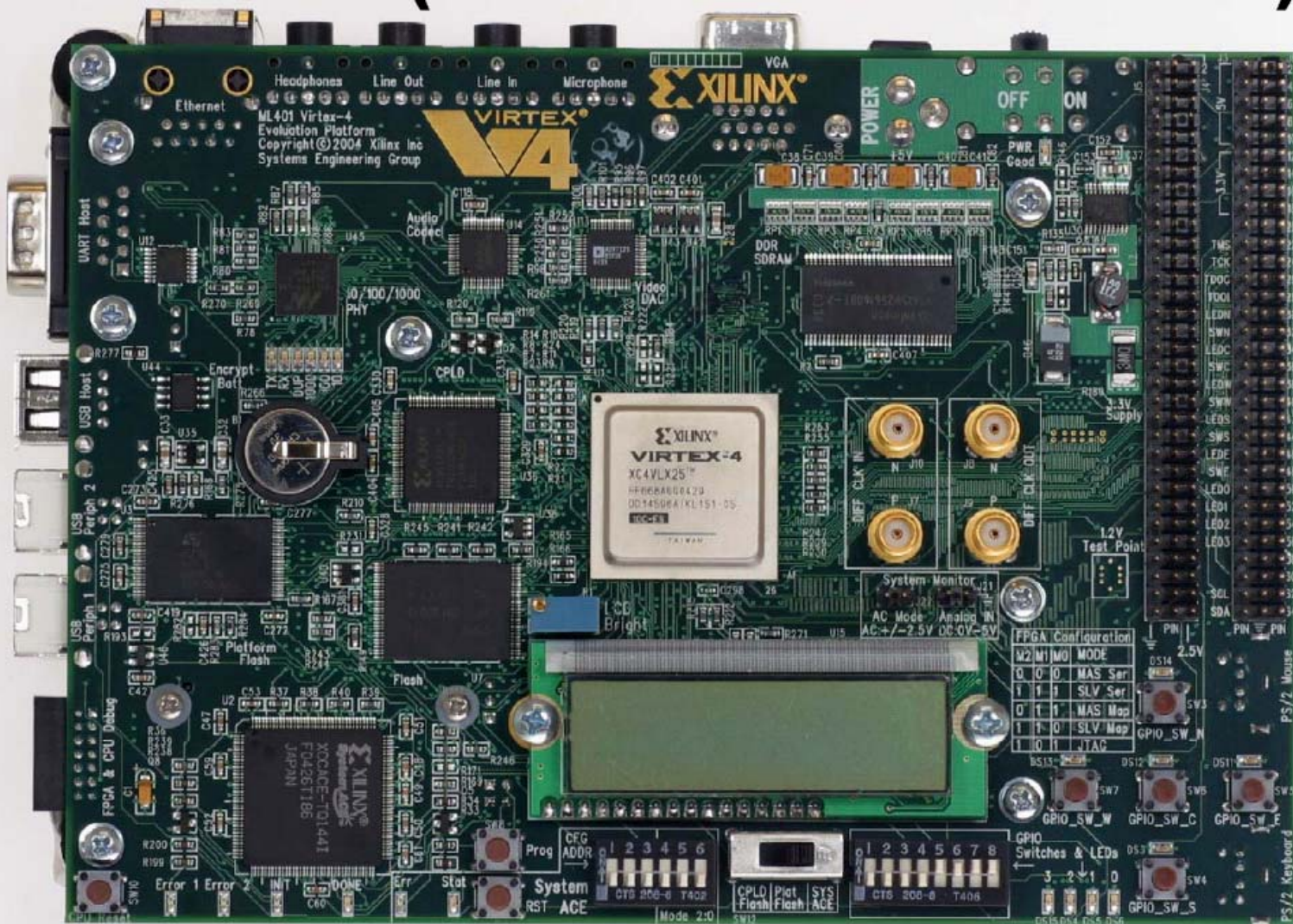


# AFX Basic Evaluation Boards



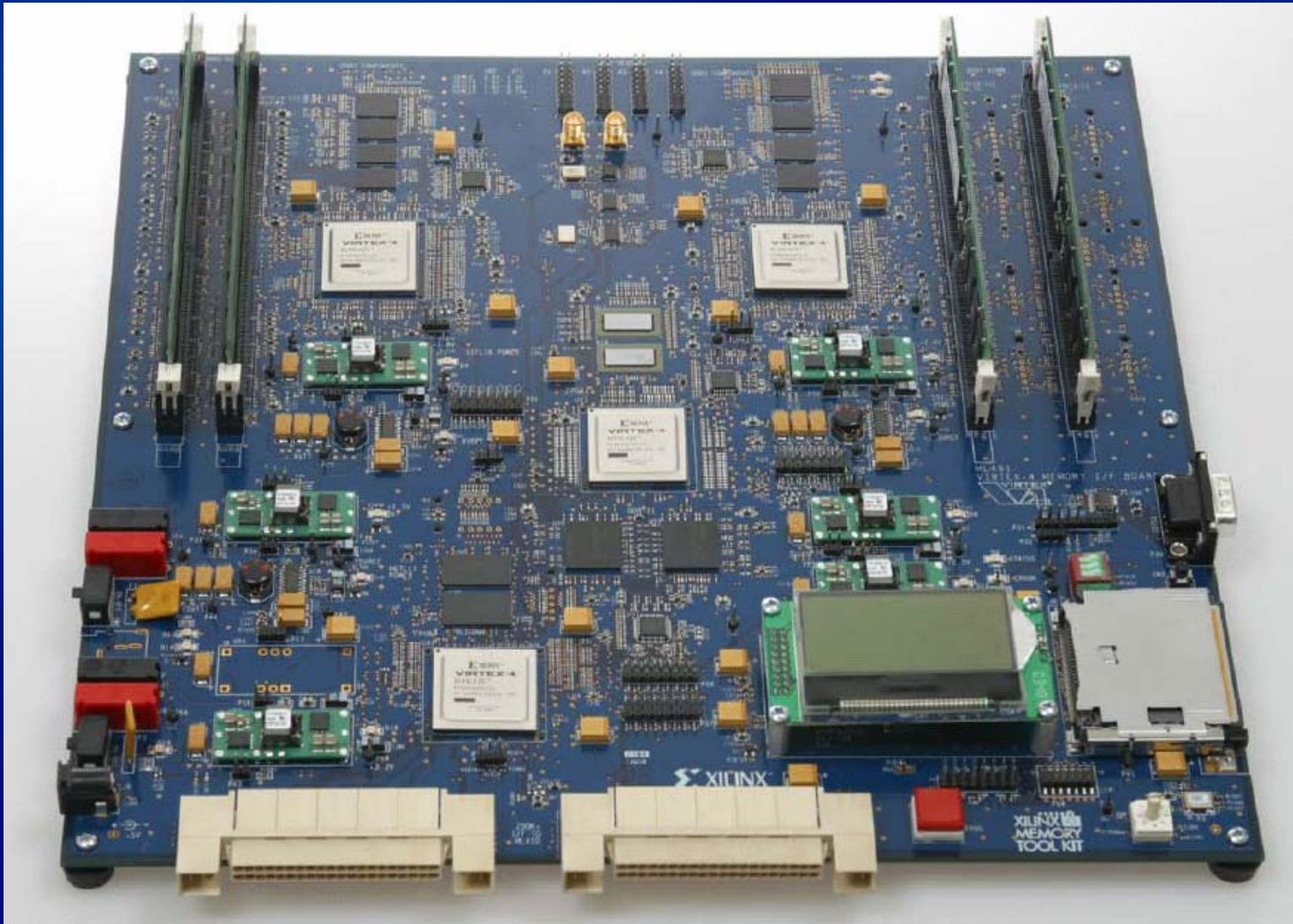


# Low-Cost ML40X (~ \$ 700)





# *ML46X- Memory Eval. Board*



# ***ChipScope Pro for Real-Time Debug***

- Debugging usually dominates the design effort
  - needs access to chip-internal nodes and busses
  - practically impossible to dedicate extra pins and routing
  - don't waste time “debugging the debugger”
- ChipScope Pro has internal virtual test headers
  - Small cores that act as internal logic state analyzers
- ChipScope Pro provides full visibility at speed
  - Read-out via JTAG, no extra pins needed

***ChipScope Pro is the best tool for logic debugging***



# ChipScope Pro Available Today



ChipScope Pro on-chip debug solution

60-Day free evaluation version

\$695 full version

[www.xilinx.com/chipscope](http://www.xilinx.com/chipscope)



## Agilent FPGA Dynamic Probe

Purchased separately from Agilent  
Acquisition \$ 995 option for your  
16900, 1690 or 1680 logic analyzer  
[www.agilent.com/find/FPGA](http://www.agilent.com/find/FPGA)





# ***1 Hz to 640 MHz Pulse Generator***

- Direct Digital Synthesis in smallest Spartan3 chip
  - PicoBlaze for arithmetic and user interface
  - Special DCM frequency synthesis for <350 ps jitter
  - External PLL for jitter reduction to 100 picoseconds
- Max 640 MHz in 1 Hz steps, 1 ppm accuracy
- Three SMA outputs: LVDS plus single-ended
  - 1000 frequency values can be stored in EEPROM
- Small size, low cost, easy single-knob control

***Early 2005, next generation will reach 5 GHz***



# 640 MHz Pulse Generator



# ***Two Problems and Solutions***

## **Single-Event Upsets (SEUs)**

radiation-induced soft errors

and

## **Extra Metastable Delay**

unpredictable delay when set-up time is violated



# *Single-Event Upsets in Virtex-II*

SEU = random **soft** error,

directly or indirectly caused by solar radiation

Known problem at high altitude and space  
traditionally not a problem at sea level.

Many tests, papers, show ways to mitigate:  
readback, scrubbing, triple redundancy

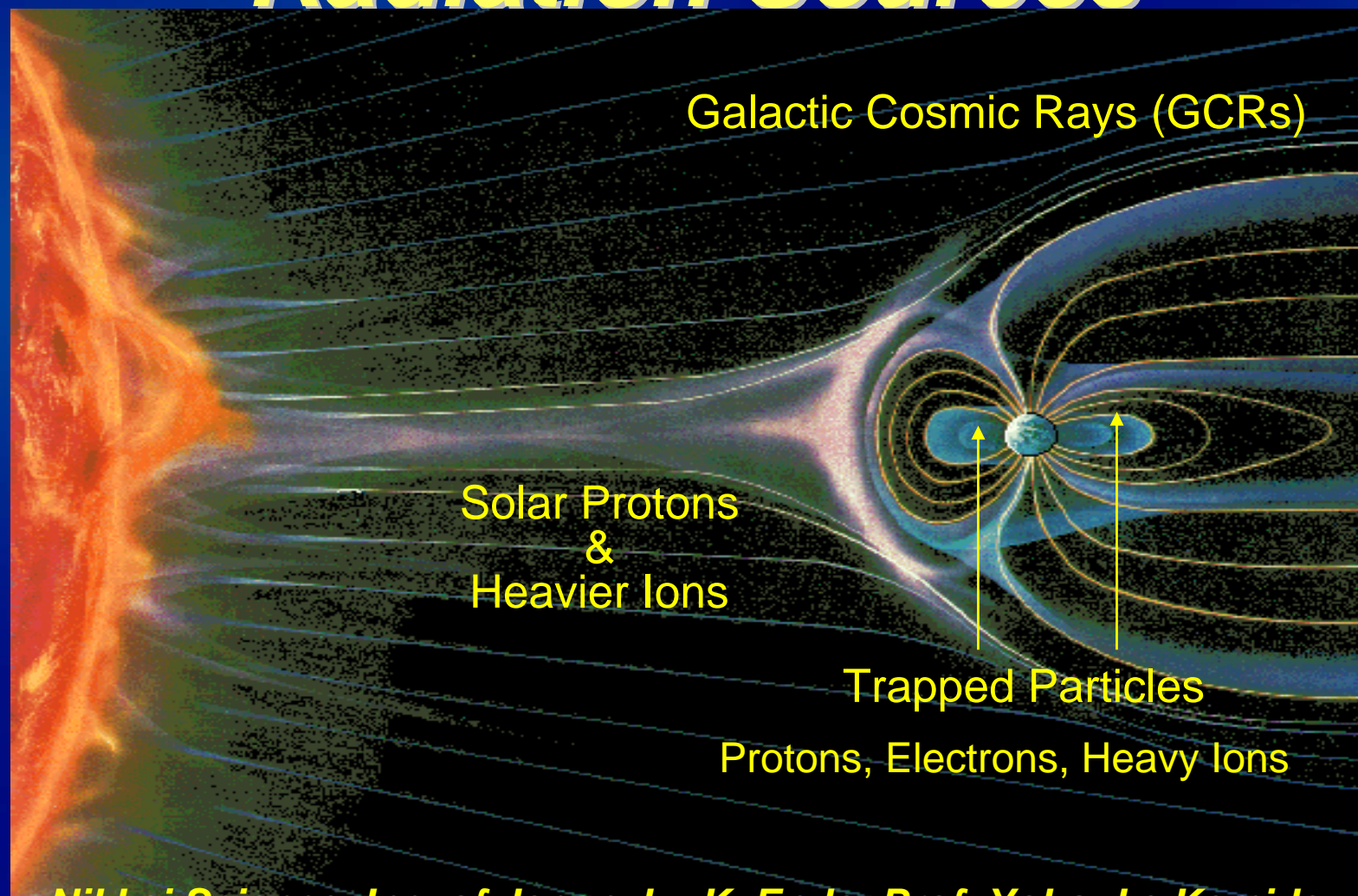
Aerospace apps tolerate the cost/size penalty.

*Creates FUD: Fear, Uncertainty & Doubt*





# Radiation Sources



*Nikkei Science, Inc. of Japan, by K. Endo, Prof. Yohsuke Kamide*



# *Traditional Test Methods*

Vastly accelerated testing procedures  
bombarding operating FPGAs  
at Los Alamos and Sandia Labs

Many SEUs are detected and reported

But:

There is no agreed-upon conversion factor to  
“normal” terrestrial operation.

*... there really was no meaningful data*



# ***Xilinx Large-Scale Test***

**4 boards with 100 XC2V6000s each**

Running 24 hrs/day, internet-monitored  
readback and error logging 24 times/day

San Jose, (at sea level)

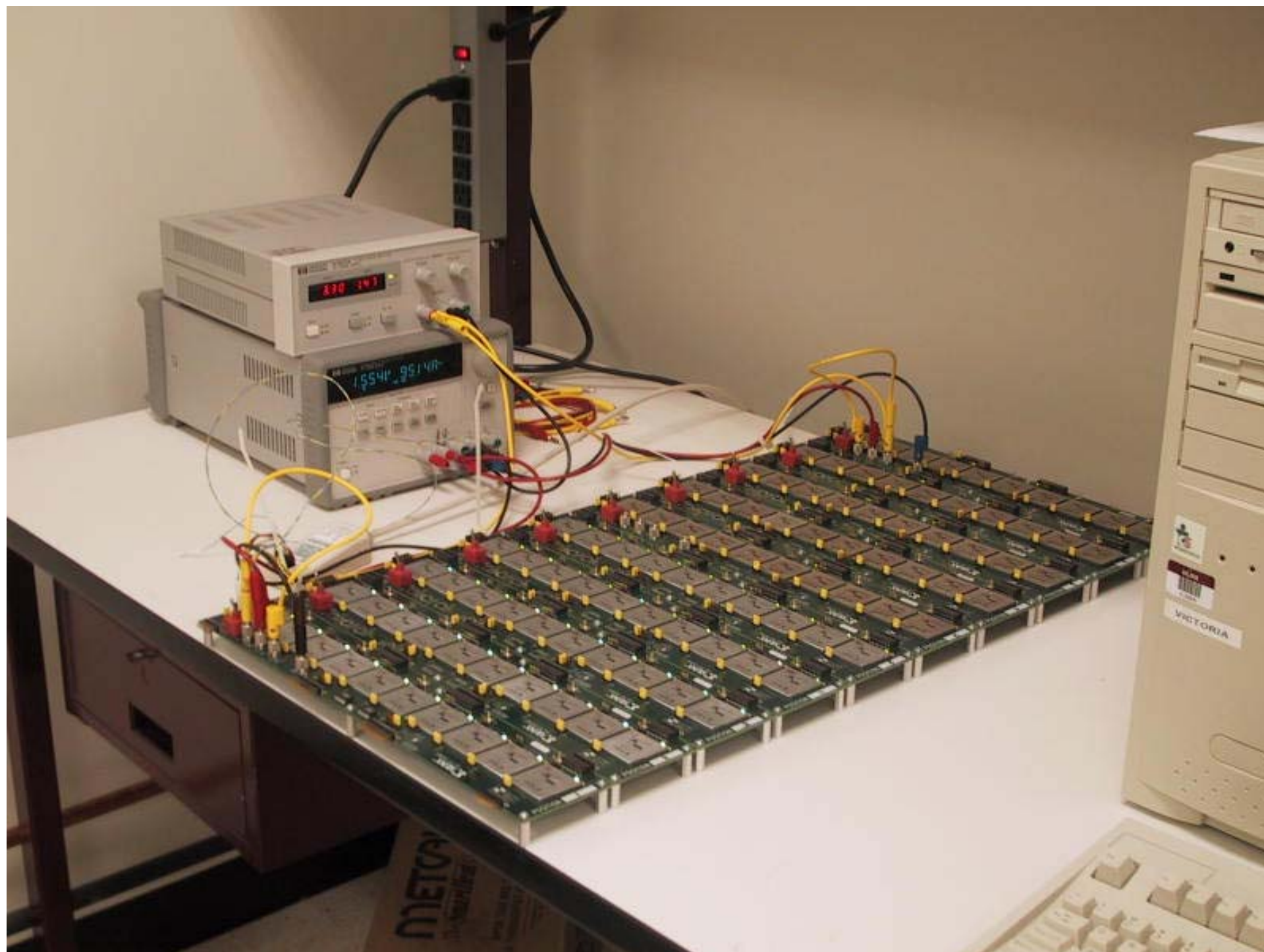
Albuquerque, NM (1500 m elevation)

White Mountain, CA (4000 m )

Mauna Kea, Hawaii, (4000 m )







# ***What's the Real MTBF ?***

Measured mean time between SEUs  
in XC2V6000 at sea level is

**18 to 23 years** (with 95% confidence.)

But >90% of config. cells are always unused,

The Real **Mean Time Between Functional Failure**  
therefore is **180 to 230 years** for XC2V6000

or **1300 years MTBFF** for XC2V1000

*90-nm has been tested to be 15% better yet !*



# *Metastability*

Violating set-up time can cause **unknown delay**

A potential problem for **all** asynchronous circuits

Problem is statistical and **cannot be “solved”**

Xilinx published tests in 1988, 1996, and 2001

Modern CMOS flip-flops recover surprisingly fast

*Metastability is now irrelevant in many cases*



# ***Metastability Capture Window***

Tested on Virtex-IIPro

- 0.07 nanoseconds for a 1 ns delay clk-to-Q+set-up
- 0.07 femtoseconds for a 1.5 ns delay
- etc

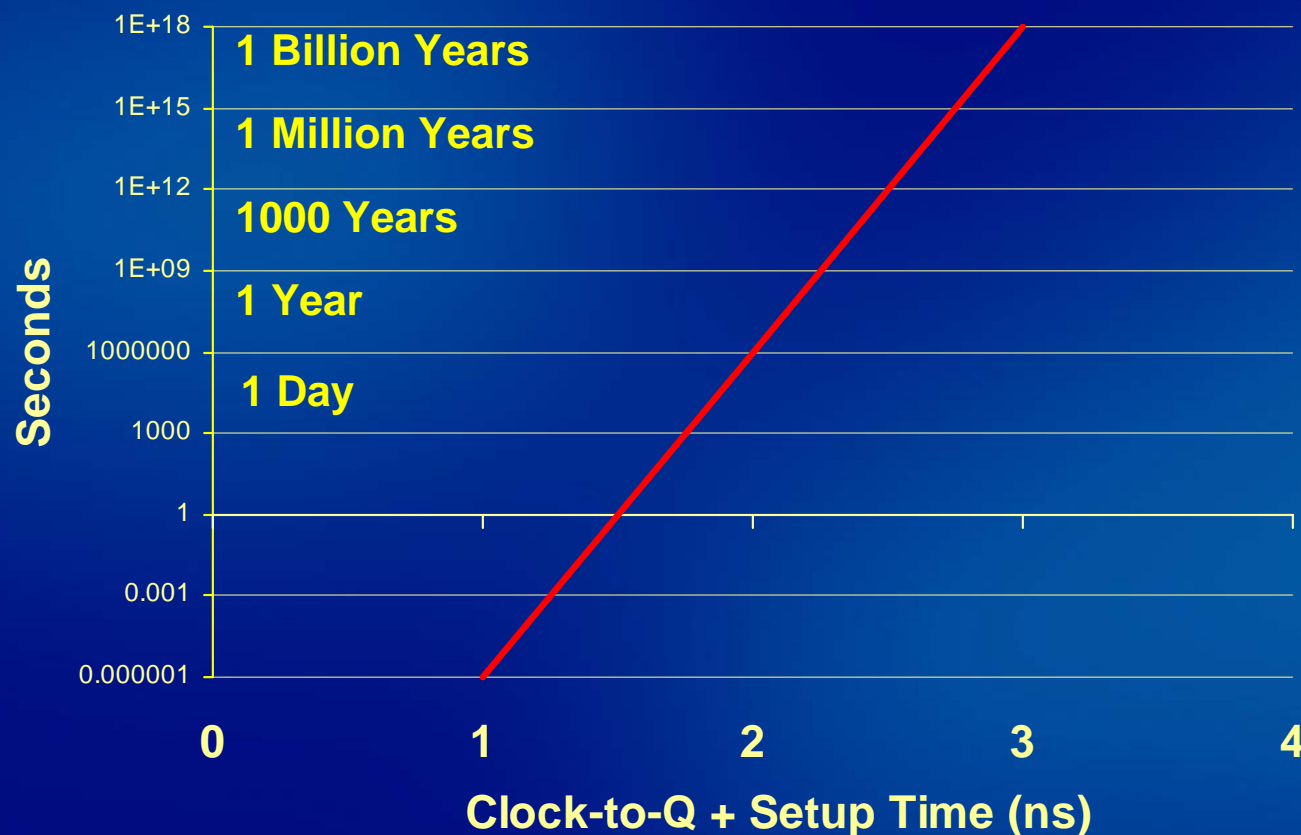
A **million** times smaller  
for each additional **0.5 ns** of delay

This parameter is independent of clock and data rates

***Makes it easy to calculate MTBF in any system***



# *Mean-Time-Between-Failure as a Function of Tolerable Delay*



*at 300 MHz clock rate and ~50 MHz data rate*



***FPGAs have become***

***cheaper***

***faster***

***bigger***

***more versatile***

***and easier to use***

***They are now the obvious first choice  
for the system designer***

***Thank you for your attention !***





# *FPGAs in 2004*

