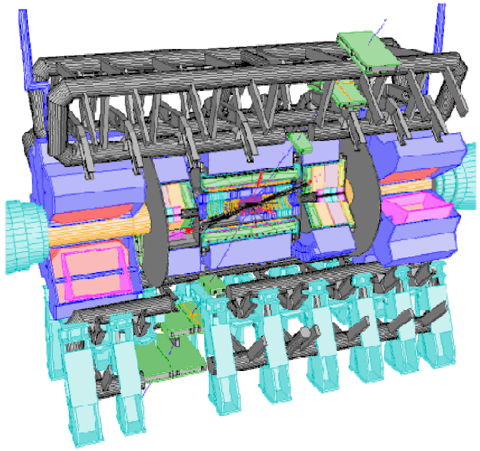

ATLAS

ATLAS / LAr CALIBRATION SYSTEM

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Outline

- ✓Motivations
- ✓Requirements
- ✓Description of the calibration board
- ✓Performances of last prototype
- ✓Production, tests and qualification

Motivations

✓Liquid argon calorimeter: stability and uniformity of the ionisation signal

✓Physics requirements

- Excellent energy resolution: to reconstruct energy of e^-, γ and jets
- Large dynamic range: from 50 MeV to 3 TeV
- Charge not totally integrated: fast response (< 50 ns)
- Good radiation tolerance: high fluences during 10 years

✓Energy resolution :

$$\frac{\sigma_E}{E} = \frac{10\%}{\sqrt{E}} \oplus \frac{300\text{MeV}}{E} \oplus 0.7\%$$

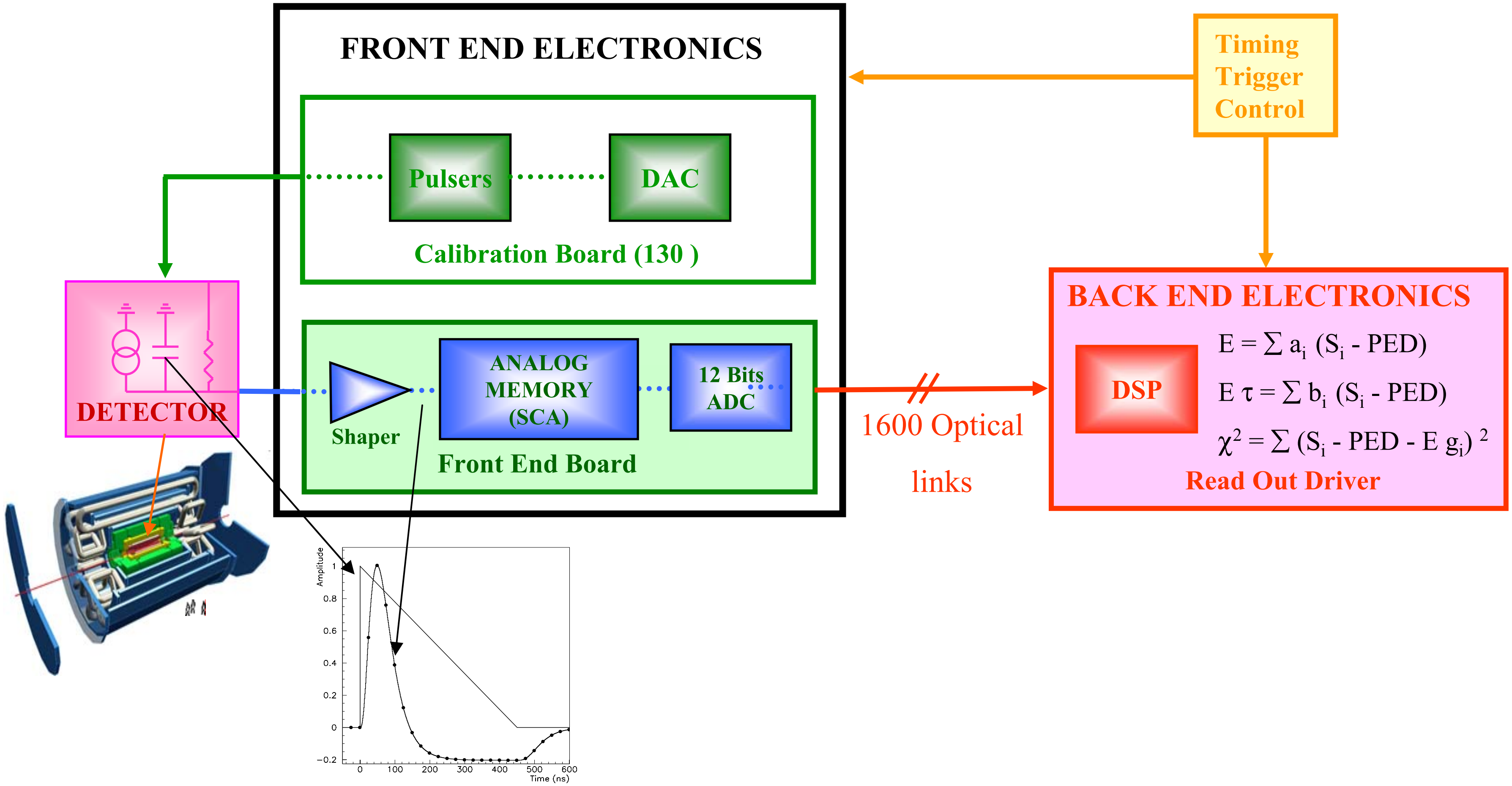
expected constant term

Non-uniformity sources	%
Absorber non-uniformity	0.2
Liquid gap non-uniformity	0.15
Residual Φ-modulation	0.2
Electronics read-out	**0.25**
+ other effects …	
Total	< 0.7

Main contribution!

Linked to our ability to calibrate the 200000 channels with a good accuracy

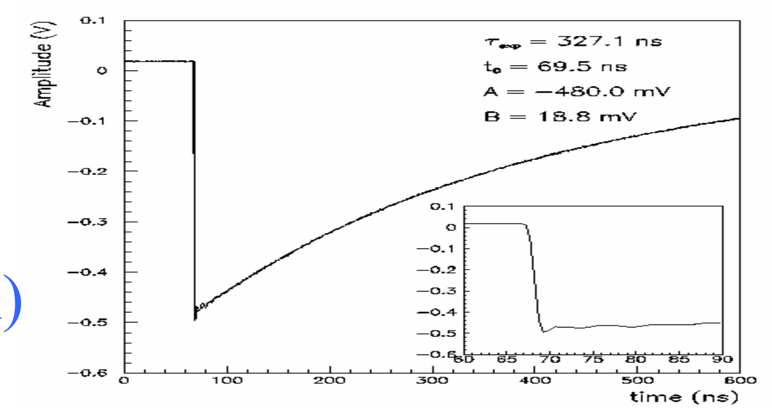
The Calibration board in the electronics chain



⇨ Designed to deliver a uniform, stable and linear signal with a shape similar to the calorimeter ionization current signal

Requirements

- ✓ Goal: inject a current pulse as close as possible as the physics pulse
- ✓ Output: 128 analog channels
- ✓ Rise time: < 1 ns
- ✓ Decay Time: 450 ns
- ✓ Dynamic range: 16 bits (2 μA to 200 mA)
- ✓ Integral non linearity: < 0.1%
- ✓ Uniformity between channels: < 0.25%
- ✓ Timing between physics and calibration pulse: ±1 ns
- ✓ Radiation hardness:
  - 50 Gy, 1.6 10^{12} Neutrons/cm^2 in 10 years
  - DMILL chips (active elements) qualified up to 500 Gy, 1.6 10^{13} Neutrons/cm^2 to include safety factors
- ✓ Jitter introduced by the board: better than the one induced by the arrival time of the particles → < 150 ps

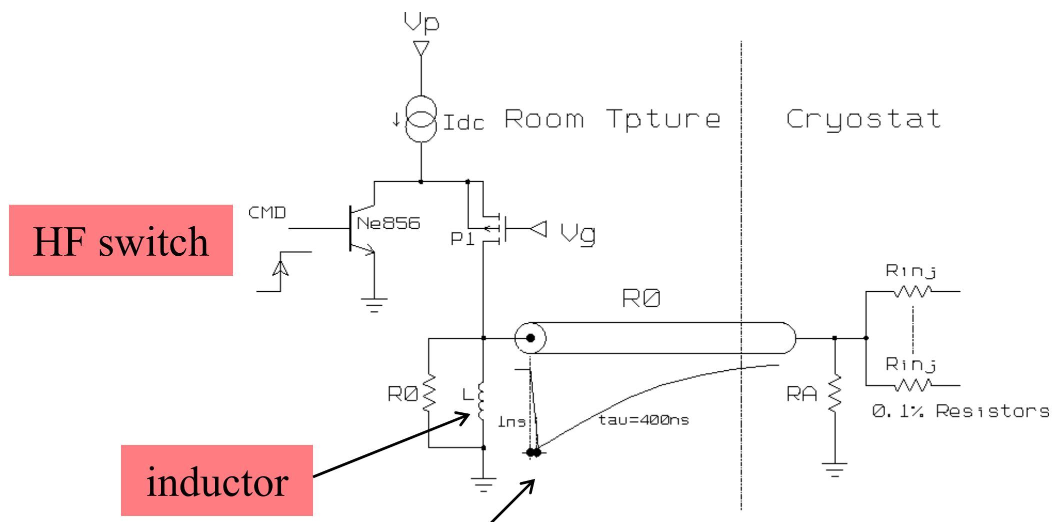


Principle of the calibration

1. Selection of a calibration value from a 16 bits DAC
2. Low offset opamp to generate a precise DC current (Idc)
3. Idc flowing in inductor L
4. Command pulse diverting Idc to ground
5. Second fast transistor then cutted off

} HF switch

6. Fast pulse produced by the magnetic energy stored in the inductor

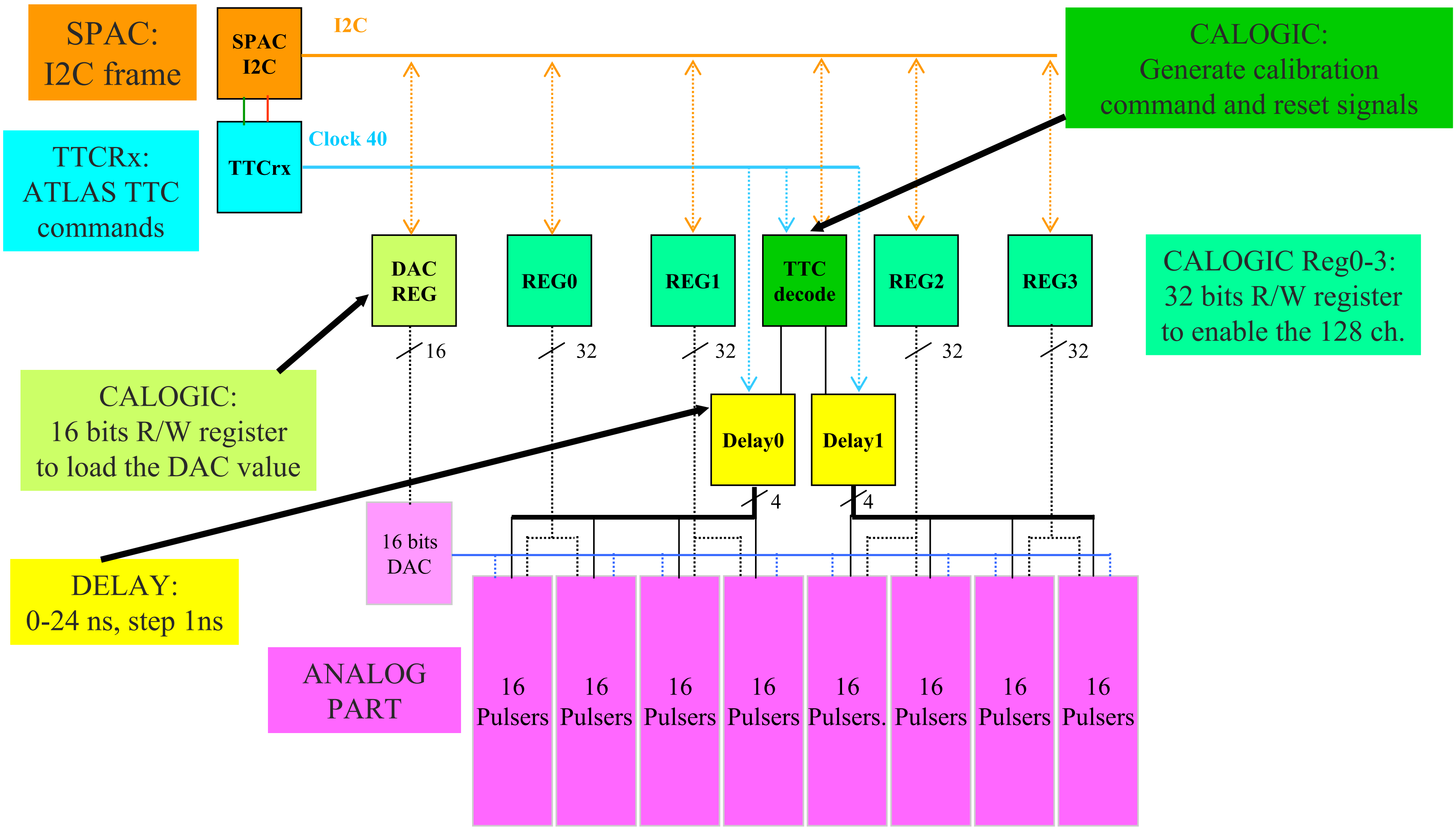


$$I_{cal} = I_{dc} \frac{R0/2}{R_{inj}} e^{-2R0t/L}$$

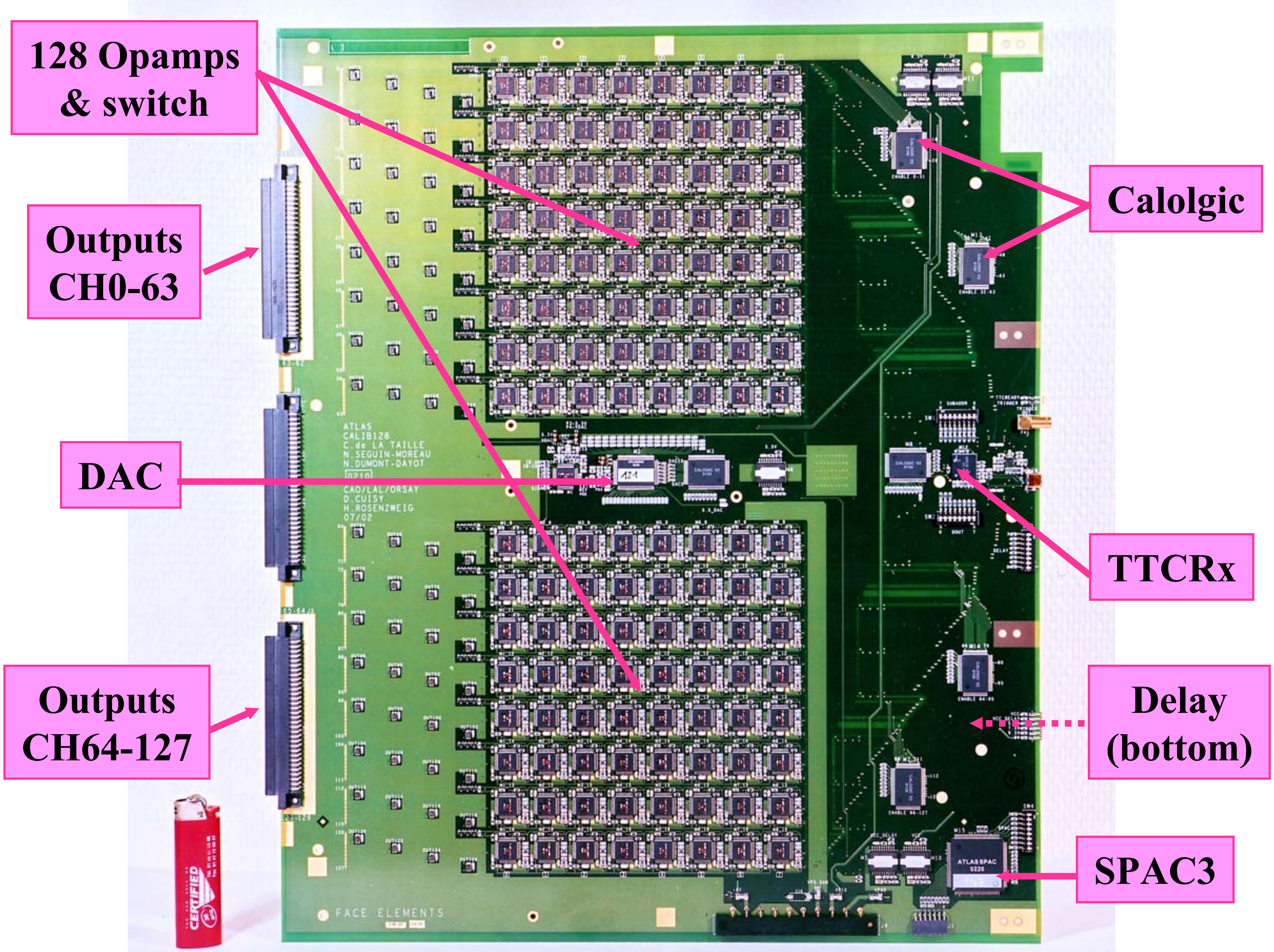
Board description

- ✓ 128 channels per board
- ✓ Analog part:
  - Challenge to obtain a uniform distribution (in time and in amplitude) with a very high density of components
  - Difficult routing to minimize the coupling between channels
- ✓ Digital part:
  - Receives the 40MHz clock from the TTC (Timing Trigger Control)
  - Decode the calibration command
  - Manages external communications via a dedicated protocol (I2C):
    - Enable desired channels (32 bits output registers)
    - Load DAC value (16 bits output register)
    - Delay calibration command (between 0 and 24 ns, step=1 ns)
    - Control the voltage regulators
    - Monitor the temperature

Digital part



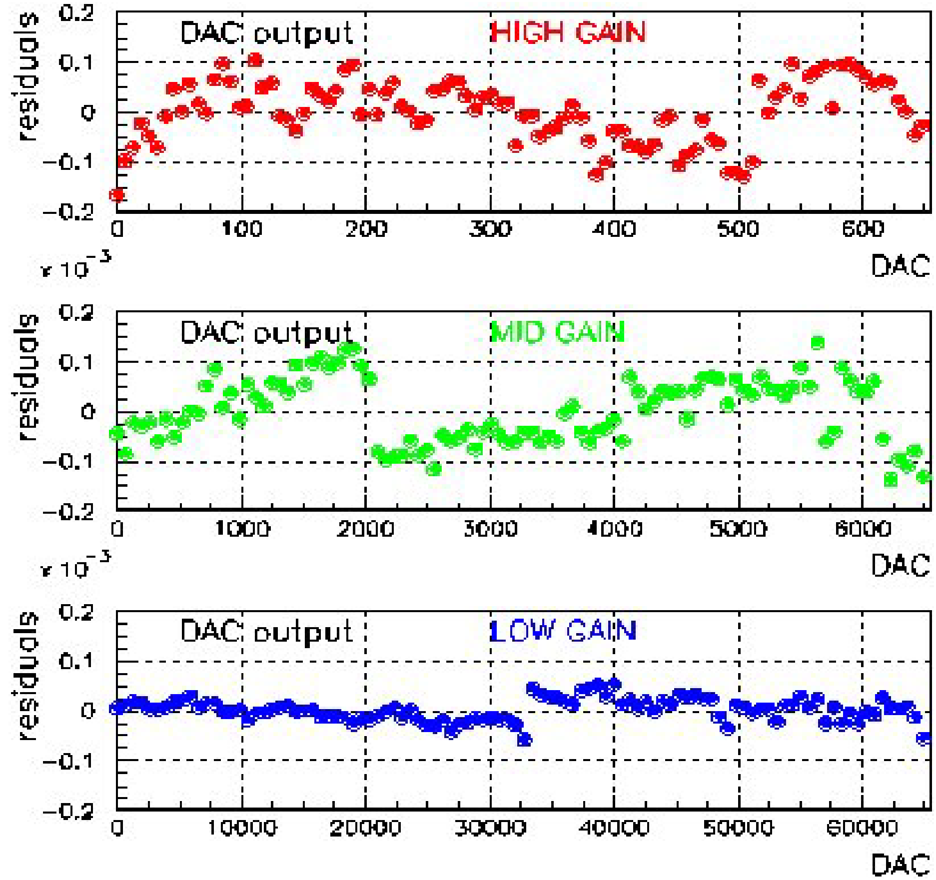
View of the calibration board



DAC measurements

- ✓ 1 DAC / board distributed to all channels
- ✓ DAC linearity performed with a precise voltmeter (after 30 mn warming up)
- ✓ 3 shaper ranges
  - High gain: 0 – 655 (0-10 mV)
  - Medium gain: 0 – 6553 (0-100 mV)
  - Low gain: 0 – 65535 (0-1 V)
- ✓ Residuals:
  - HG: < ± 1 µV
  - MG: < ± 10 µV
  - LG: < ± 50 µV
- ✓ Non-linearity: < 0.01%, far better than the requirement (0.1%)
- ✓ Fit parameters of DAC linearity:
  - P0: due to the distribution opamp offset
  - P1: 1 LSB = 15.26 µV

Residuals of DAC linearity over the 3 gains



VDAC/DAC	P0	P1	RMS
High Gain	18 µV	15.282 µV/DAC	60 ppm
Mid Gain	16.61 µV	15.276 µV/DAC	63 ppm
Low Gain	25.2 µV	15.268 µV/DAC	23 ppm

DC linearity and uniformity

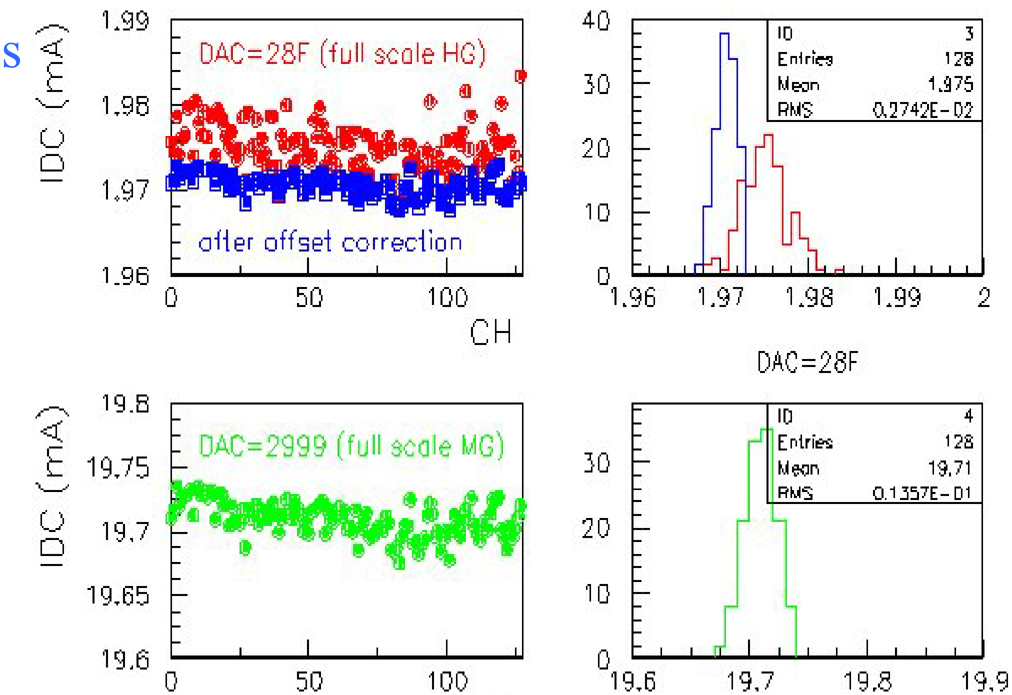
✓ DC output current linearity

- residuals < 0.01%
- Similar pattern as the DAC residuals
- DC output current independent of the number of channels ON

IDC/DAC HG	P0	P1	RMS
1 channel	1.616 µA	3.0075 µA/DAC	63 ppm
128 channels	1.678 µA	3.0062 µA/DAC	49 ppm

✓ DC current uniformity on 128 channels

- DAC = 655 (full scale HG):
  - non uniformity dominated by the opamps offsets
  - Without offset correction: 0.139%
  - With offset correction: 0.061%
- DAC = 6553 (full scale MG):
  - non uniformity dominated by the accuracy on the discrete components
  - dispersion = 0.069%



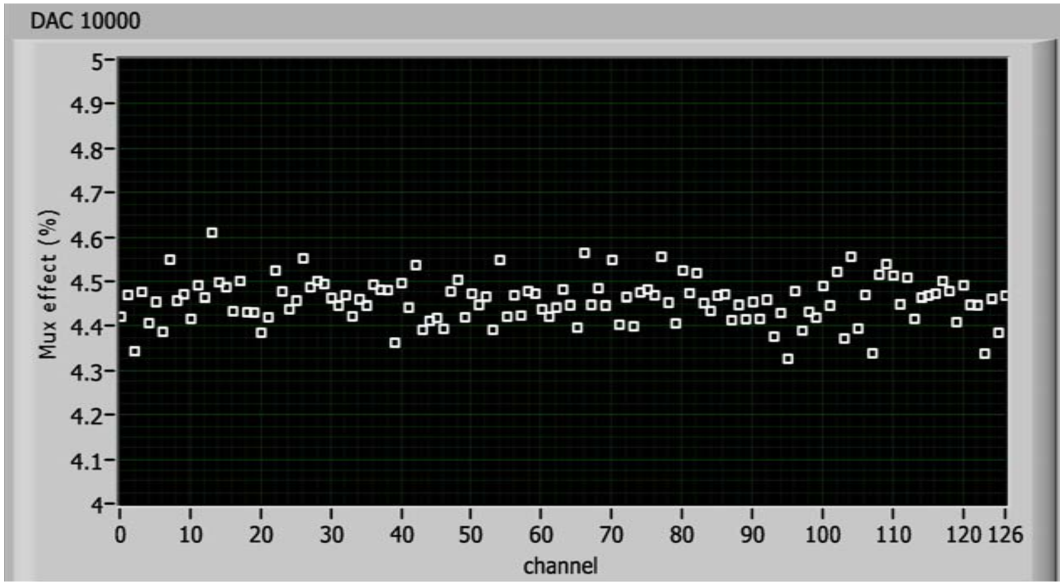
DC current uniformity for 2 gains at full scale

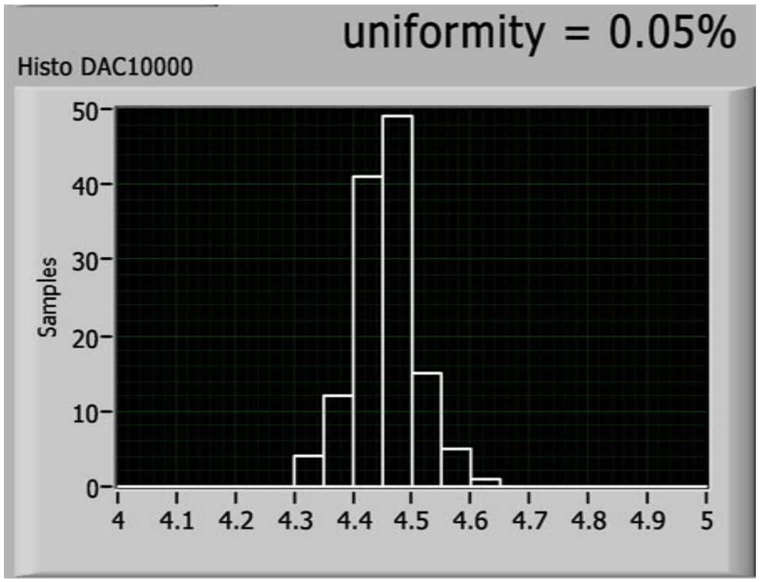
Dynamic measurements

✓Hardware used to do these measurements:

- Automatic measurement on the 128 channels with a multiplexor
- shaper CR-RC2 with a time constant of 50 ns
- Readout system: 12 bits ADC
- Amplitude measurement at the signal peak averaged on 100 triggers

Dispersion measurement of the 128 channels multiplexor



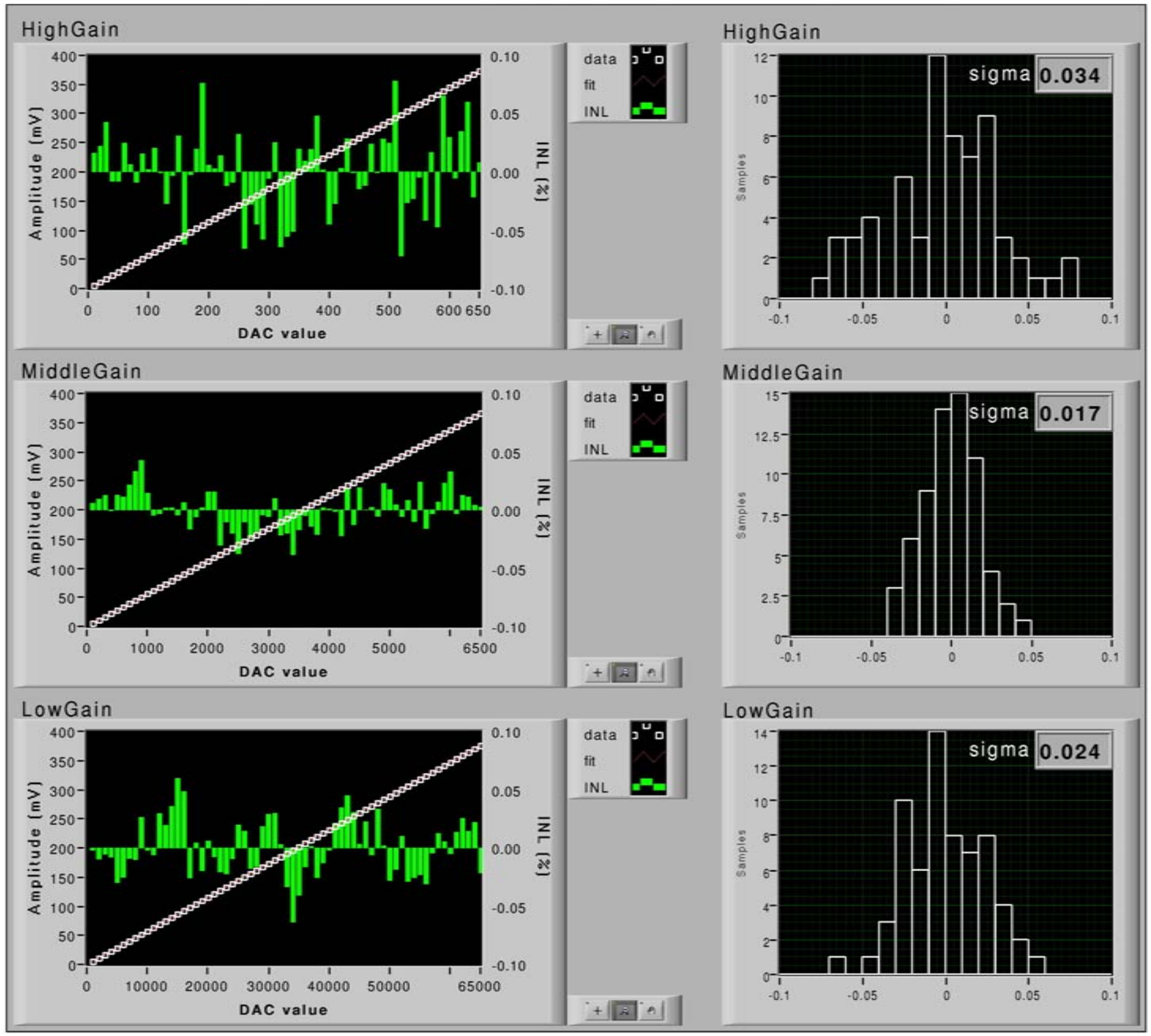


Pulse Linearity

- ✓ Integral non linearity:
  - < 0.1% for all gains
  - Dynamic linearity worse by about x10 compared to DC linearity
  - Visible effect of the non linearity of the readout

- ✓ Better than the 0.1% requirements

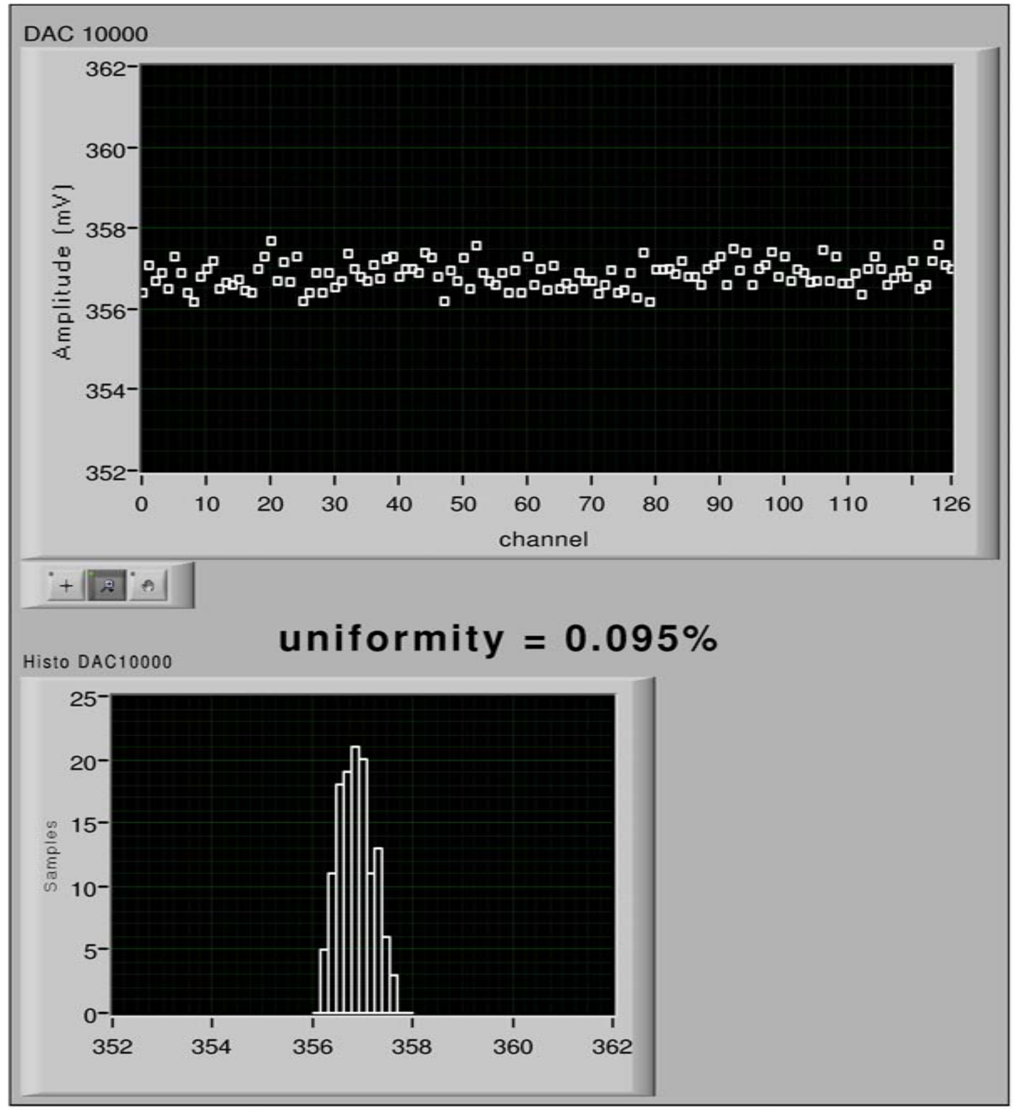
Integral non linearity of the amplitude after shaping over the 3 gains



Pulse uniformity

- ✓ Uniformity at DAC=10000:
  - RMS: 0.095%
  - DC uniformity: 0.07%
  - Possible contribution from output lines and inductors
- ✓ Same uniformity obtained whatever the DAC setting, due to the good linearity
- ✓ x2 better than the requirements (0.25%)

Amplitude uniformity for DAC = 10000



Timing measurements

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- ✓Two ways to set the delay between the LV1A (trigger) and the Calibration pulse:
  - with the 2 PHOS4_RH delays (0-24 ns, 1 ns step)
    - One PHOS4-RH delay line drives 16 calibration channels
    - Used to compensate for the cables lengths across the calorimeter
  - with the TTCrx fine delay (0-24ns, 104 ps step)
    - One unique delay value for the 128 channels
    - Used to scan the calibration pulse during special runs
- ✓Measurements procedure
  - Characterization of the timing of the full calibration chain
  - Accuracy measurement with an oscilloscope 16GS/s, 1GHz
  - Recording histograms of the delay between the 40 MHz clock and the outputs of the board channels
  - Intercept, slope and averaged jitter extracted from linear fit

Linearity with the PHOS4-RH delay

Laboratoire d'Annecy-le-vieux de Physique des Particules

✓ Chip study:

- Dependence of the performances with temperature, supply voltage,...
- Production tested in a monitored environment
- Chips selected on jitter and sorted on the step value

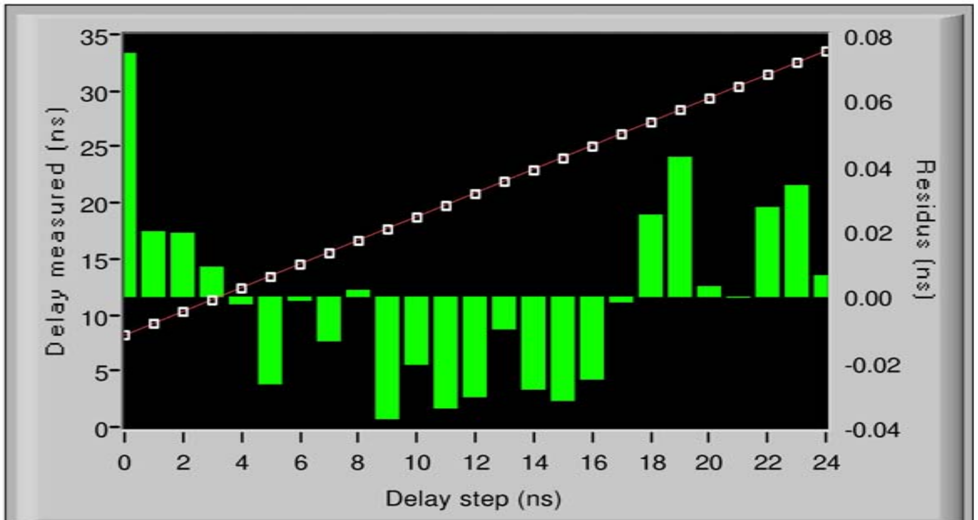
✓ Timing linearity:

- slope: not exactly = 1
- depends on the delay line, the chip and the temperature
- residuals: <70 ps

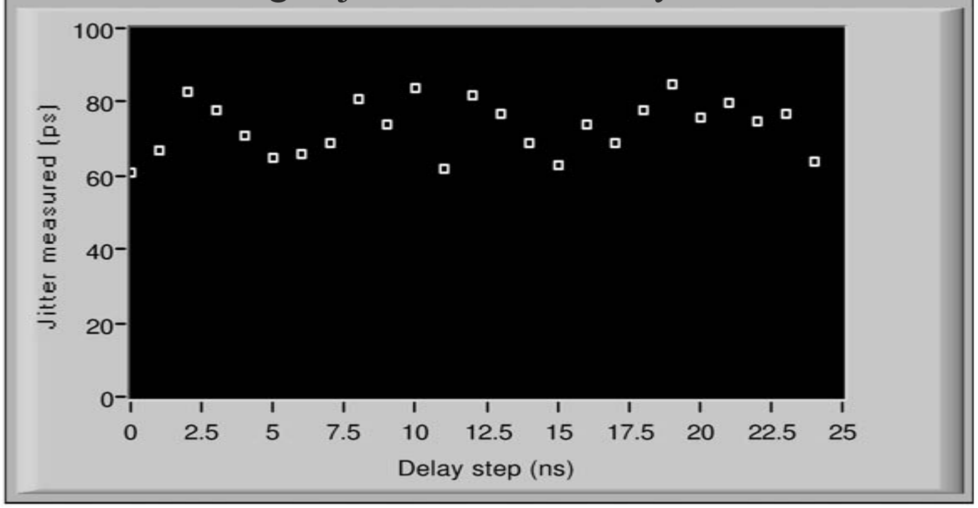
✓ Jitter:

- average: 75 ps
- stable whatever the delay value due to the chip selection
- operation point must be below a temperature threshold: !! cooling !!

Linearity measurement with PHOS4-RH delay chip



Averaged jitter for each delay value



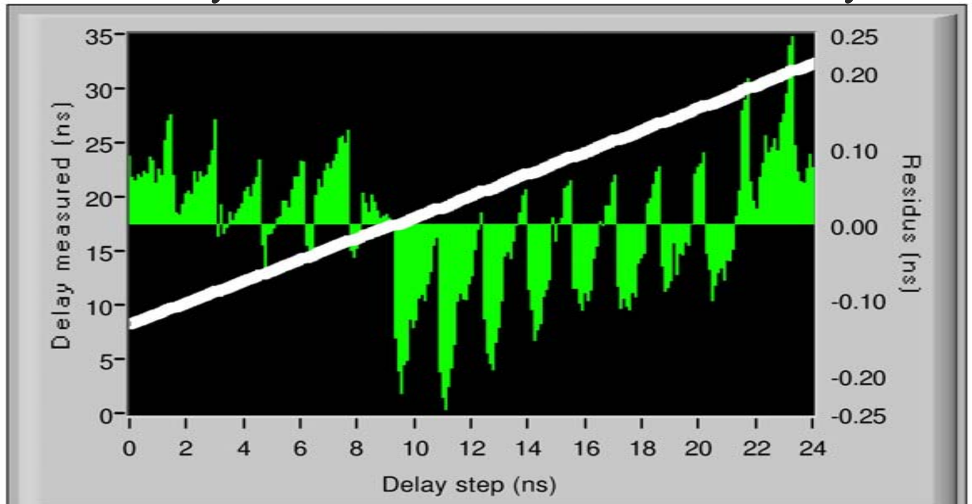
Linearity with the TTCrx fine delay

Laboratoire d'Annecy-le-vieux de Physique des Particules

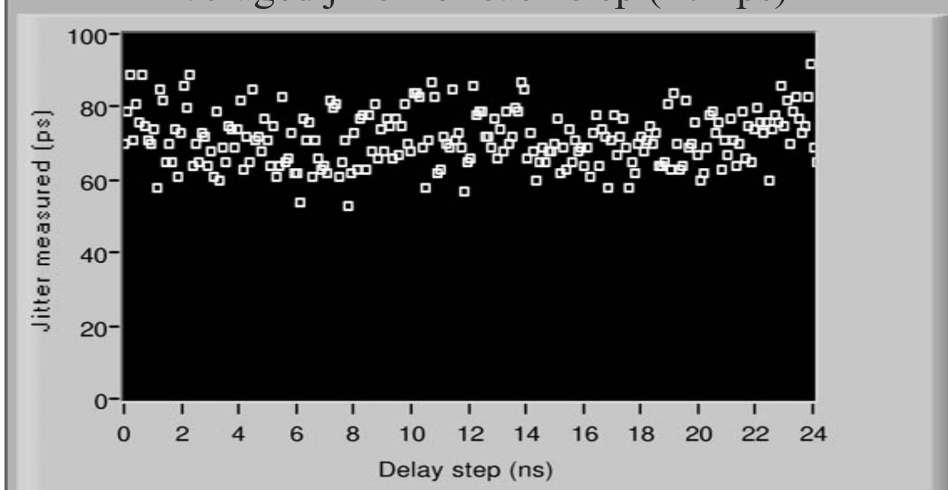
- ✓ Timing linearity:
  - slope: 1.00
  - residuals: ±250 ps (in agreement with the TTCrx datasheet)
- ✓ Jitter:
  - average: 75 ps
  - stable whatever the delay value

- ✓ Jitter induced by the calibration board should be below the one induced by the arrival time of the particles (150ps)

Linearity measurement with TTCrx fine delay



Averaged jitter for each step (104 ps)



Timing uniformity

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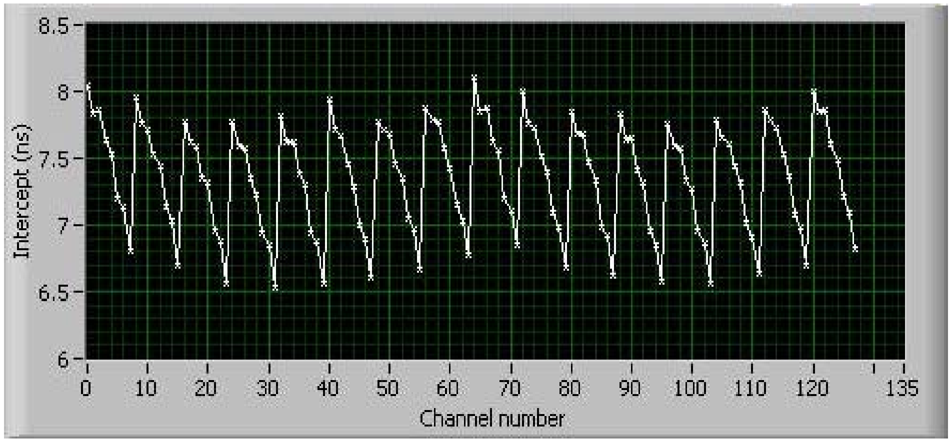
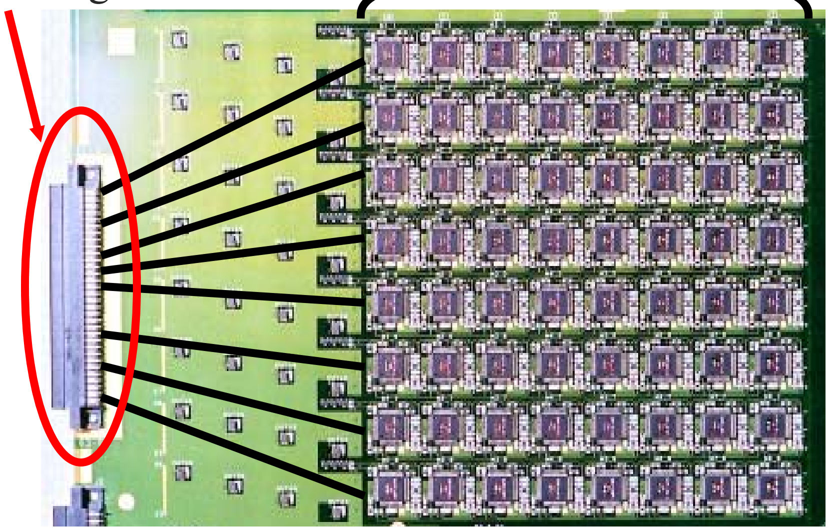
- ✓ Timing response measurement of all channels (scanning the delay values of the PHOS4-RH)
- ✓ Intercept:
  - Dispersion inside a row of 8 opamps: one calibration line distributes one row of 8 opamps
  - Parabolic behavior by group of 64 channels due to the different output lengths at the connector level
  - Dispersion by group of 16 channels due to the offset of each PHOS4RH output: little effect submerged by the parabolic behavior

Time intercept uniformity versus channel number



Different output lengths

1 calibration line / row

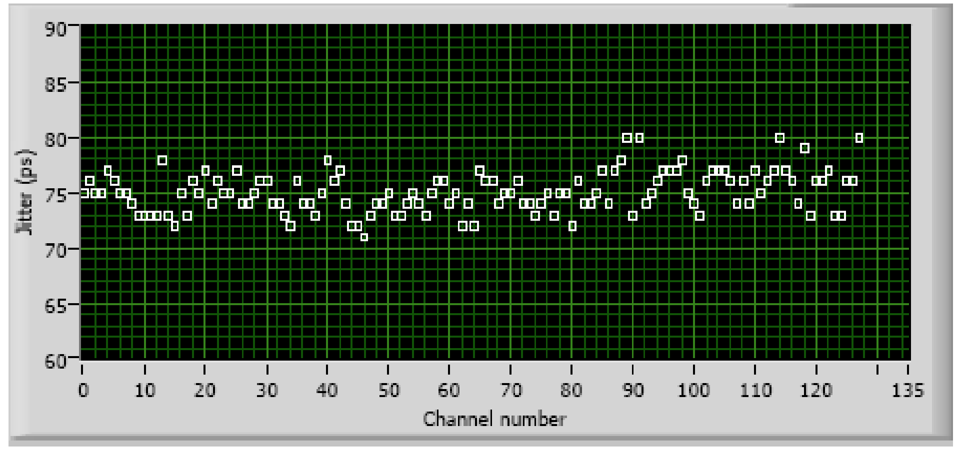


Timing uniformity (2)

✓ Jitter:

- Stable whatever the calibration channels, around 75 ps

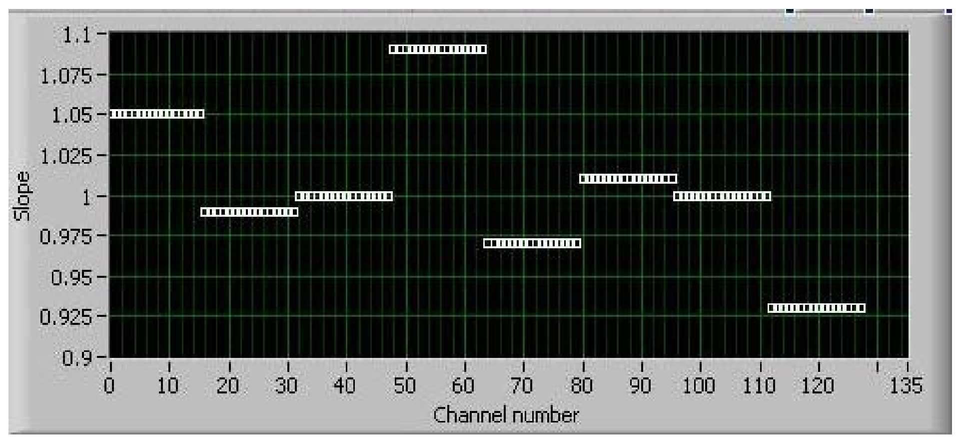
Averaged jitter versus channel number



✓ Slope:

- Constant by group of 16 channels: one PHOS4-RH line drives 16 calibration channels
- Dispersion between group of 16 channels: intrinsic characteristics of the PHOS4-RH delay chips
- Slope value between 0.93 and 1.09: need to be corrected in ATLAS (values stored in a database)
- Used for global timing adjusting: no need of excellent accuracy !

Delay chip slope uniformity versus channel number



Boards qualification procedure

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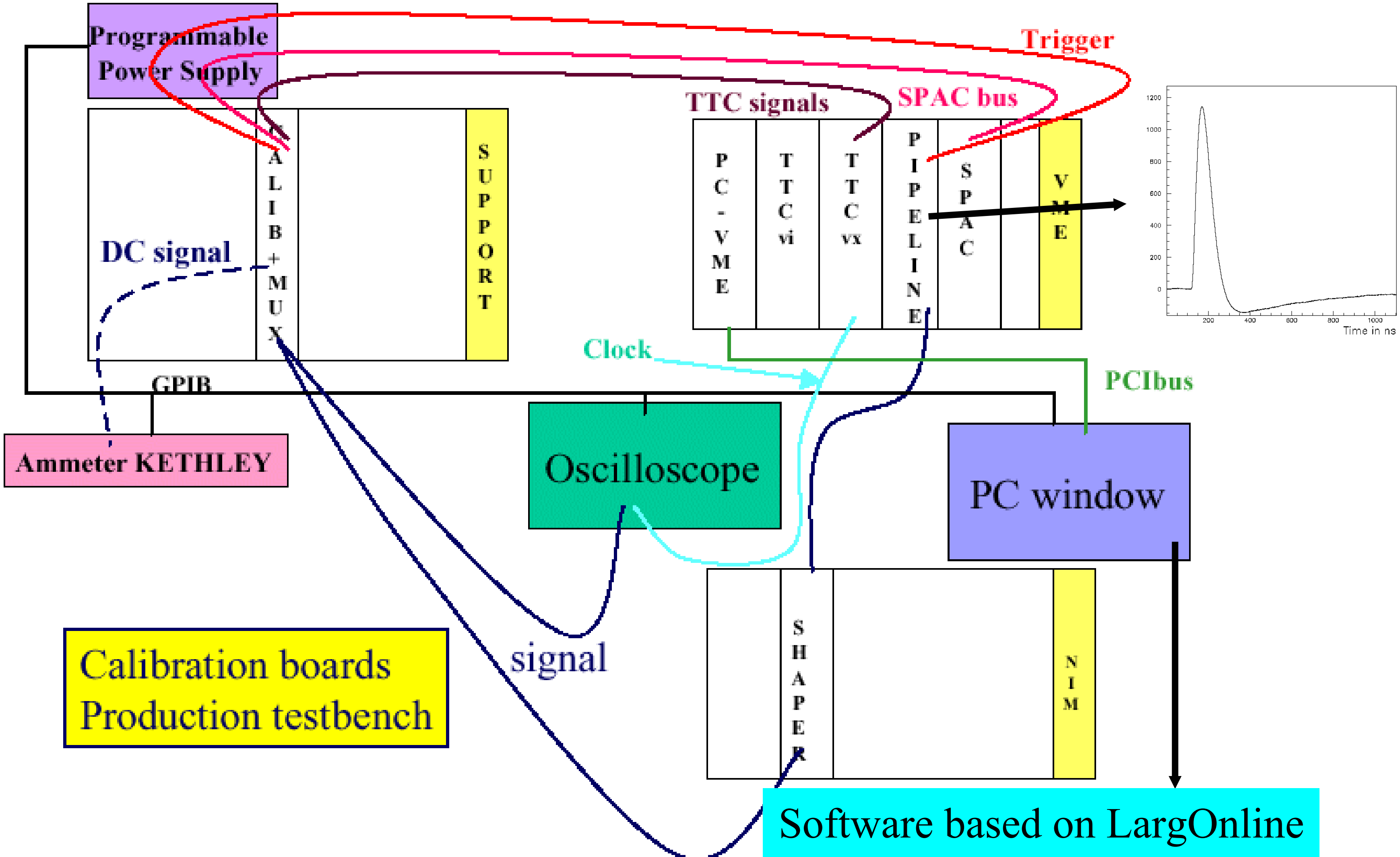
✓ Tests in industry:

- Visual inspection of the board
- Measurement of the power supply consumption
- Burn in test

✓ Qualification in laboratory:

- Identification of the whole chips on the board (traceability)
- Board powered up and current measured and compared to measurement done before burn-in at assembly firm
- Digital part tested
- Parameters tuned: voltage regulator, DAC scale
- Opamp offsets measured
- Inductor resistance measured
- Linearity of all channels and uniformity over the 3 gains measured
- Decay time constant of the exponential calibration measured
- Delay chips characterized: offset, slope, jitter
- TTCrx fine delay monitored

Board qualification in labs: bench setup



Calibration boards
Production testbench

Software based on LargOnline
+ Labview User Interface

Board qualification in labs: bench setup (2)

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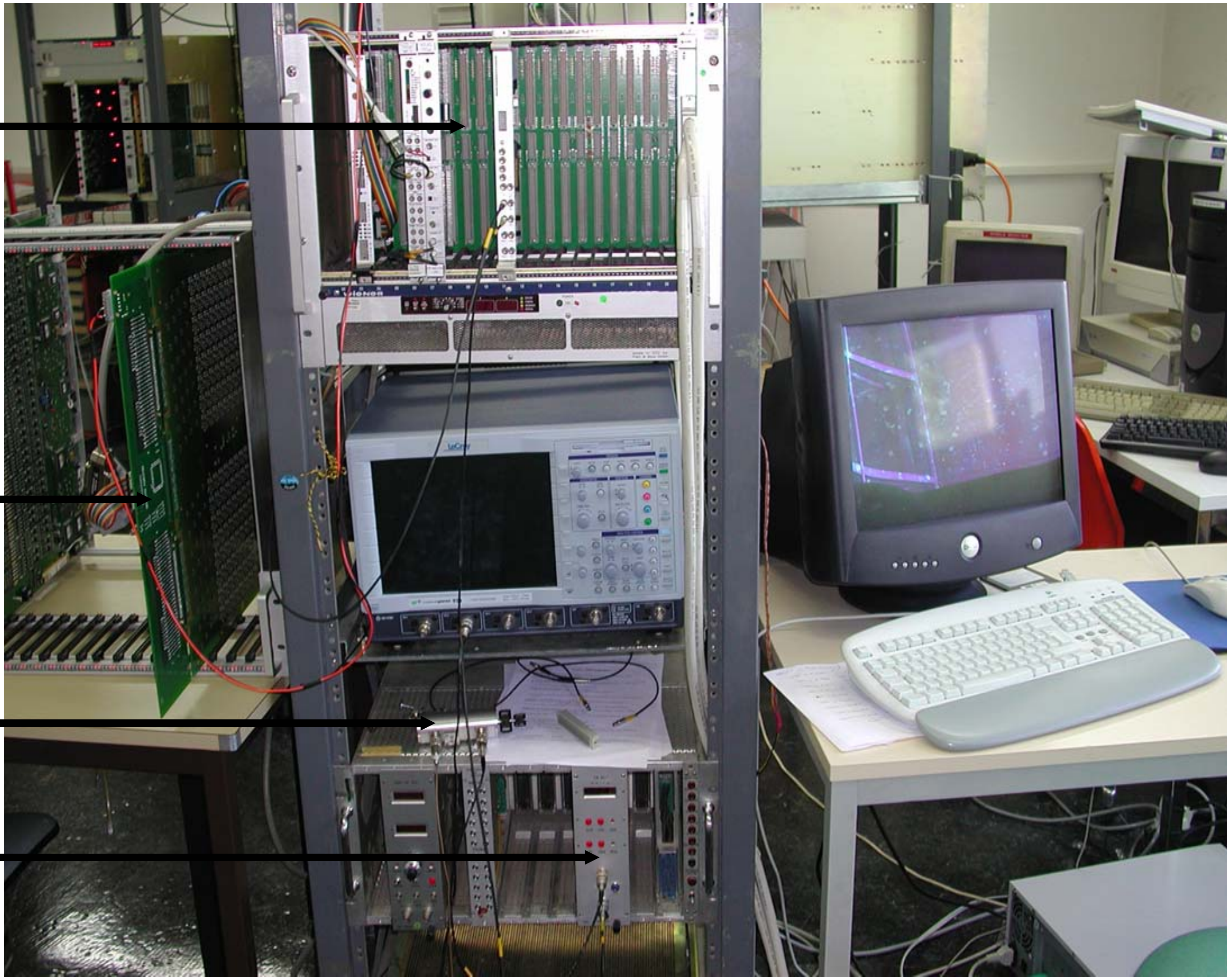
SPAC
TTCvx
TTCvi
Digitizing board

Mux board

attenuator

shaper



Conclusion

- ✓ History:
  - 10 non radhard boards produced in 98: 5 years successful operation in beam tests
  - Active elements designed in DMILL in 99-01: DAC, pulser, control logic, delay
  - 3 versions of radiation hard boards produced in 02-03
  - Last prototype in operation at the CERN combined run this summer
- ✓ Components status
  - DAC: chips produced, measurements in progress
  - OP AMPs: chips produced, tested and selection in progress
  - CALOGIC: chips produced, tested and sorted
  - Delays: chips produced, tested and sorted
- ✓ Pre-series of 4 calibration boards ready for tests of final ATLAS calorimeter electronics next october
- ✓ Production of 130 boards for ATLAS: beginning 2005
- ✓ Installation on the calorimeter at CERN: spring 2005