SLHC Trigger & DAQ

LHC Electronics Workshop

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U. Wisconsin - Madison

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Outline:

- Impact of Luminosity up to 10^{35}
- Trigger Requirements
- Calorimeter, Muon & Tracking Triggers
- DAQ requirements & upgrades
- R&D Technologies

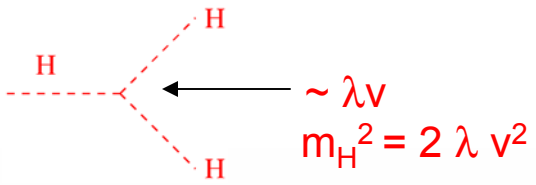
This talk is available on:

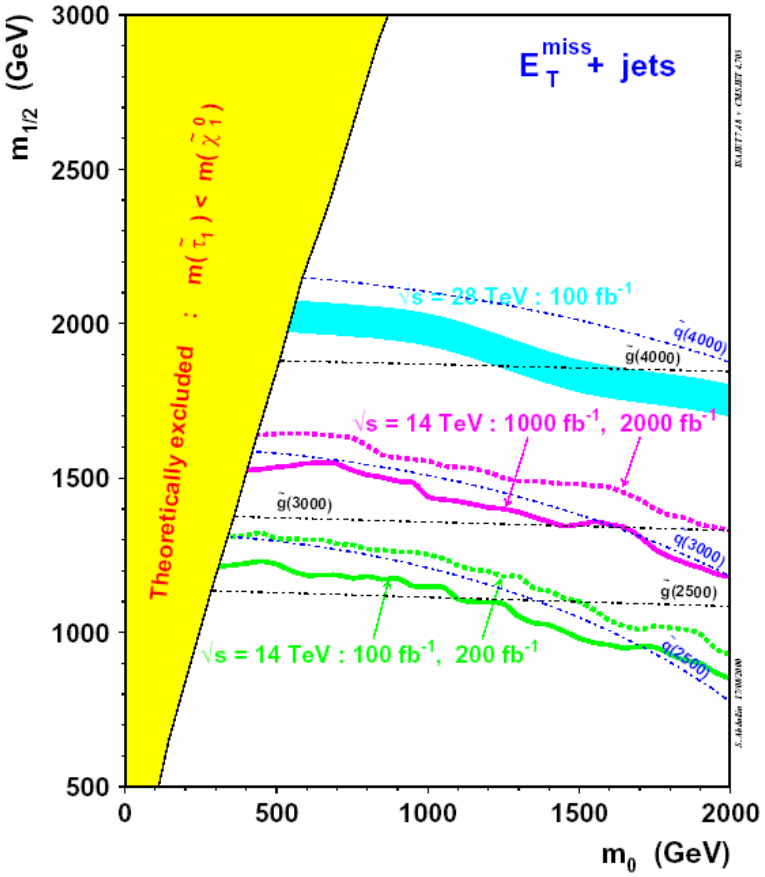
http://cmsdoc.cern.ch/cms/TRIDAS/tr/0409/Smith_SLHC_LECC04.pdf

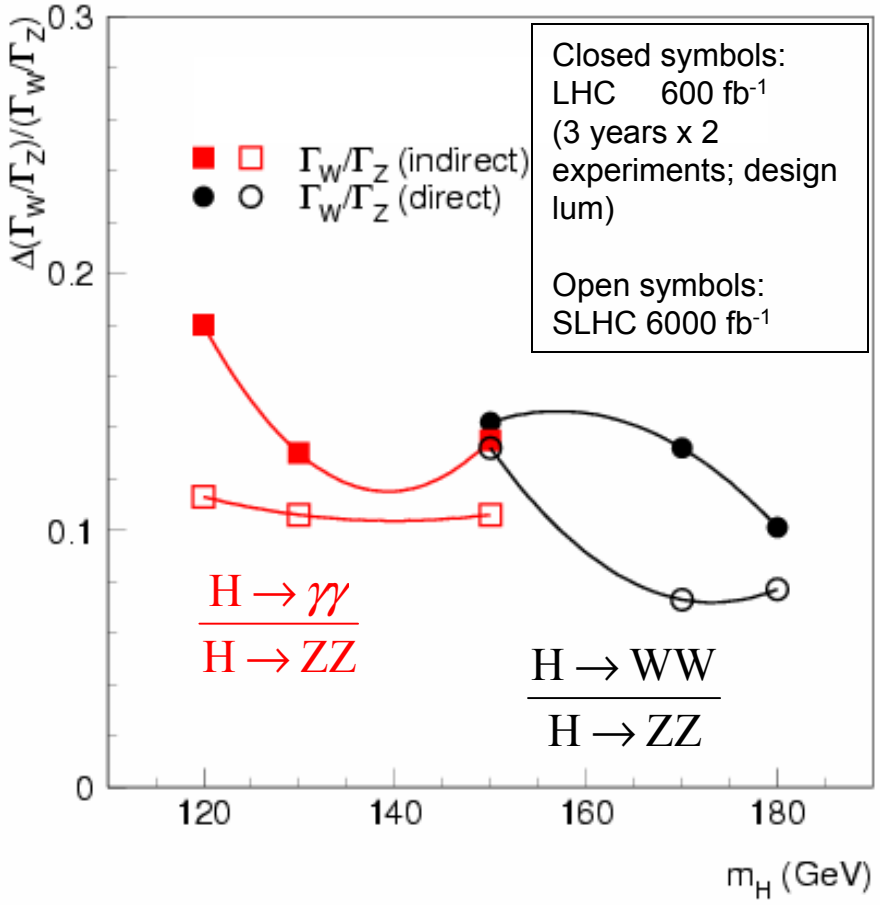
Physics of LHC Lumi x 10

Extends LHC mass reach by ~ 20-30%

Opens possibility to measure Higgs self coupling







SLHC Upgrade & Schedule

- ***SLHC Luminosity upgrade to 10^{35}:***

-- increase bunch intensity to beam–beam limit → L ~ 2.5 x 10^{34}

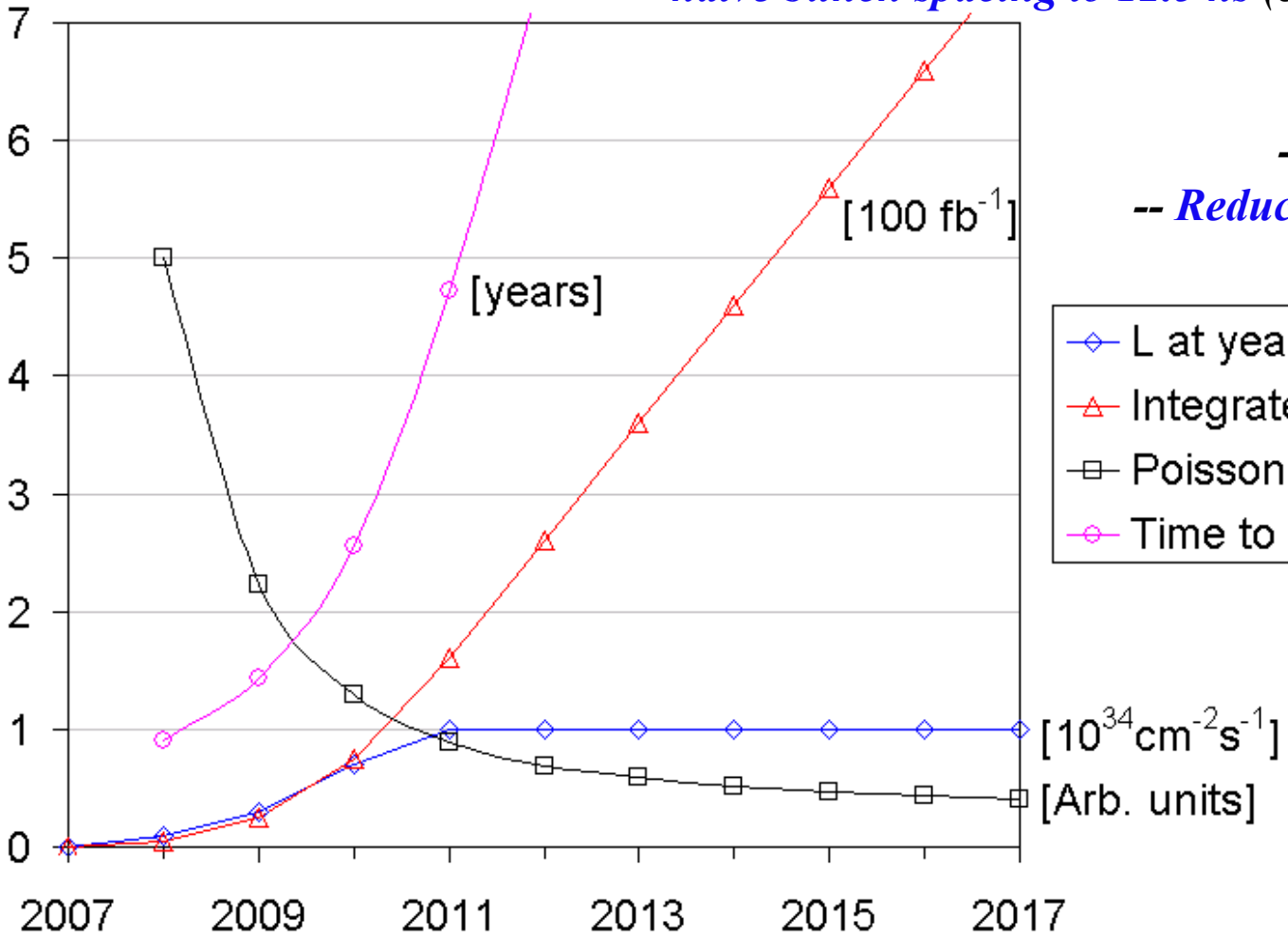
-- halve bunch spacing to 12.5 ns (electron cloud limitation?)

-- Reduce β* by x2-3

(Nb_3Sn insertion magnets)

-- Increase crossing angle.

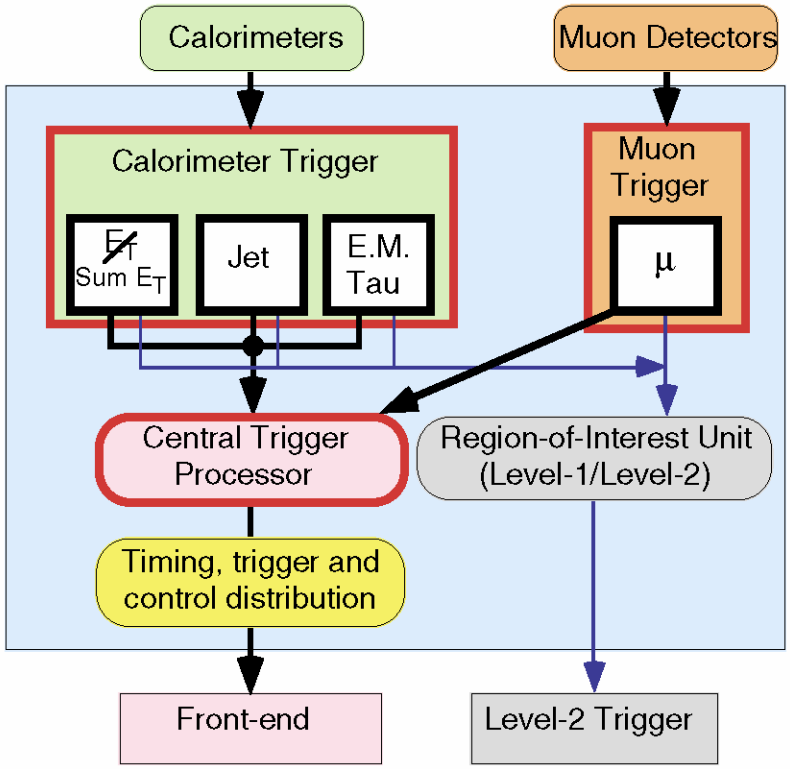
-- Reduce bunch length. (new RF)



ATLAS Trig & DAQ for LHC

Overall Trigger & DAQ Architecture: 3 Levels:

Level-1 Trigger:



Interaction rate ~1 GHz

Bunch crossing rate 40 MHz

LEVEL 1 TRIGGER

75 (100) kHz

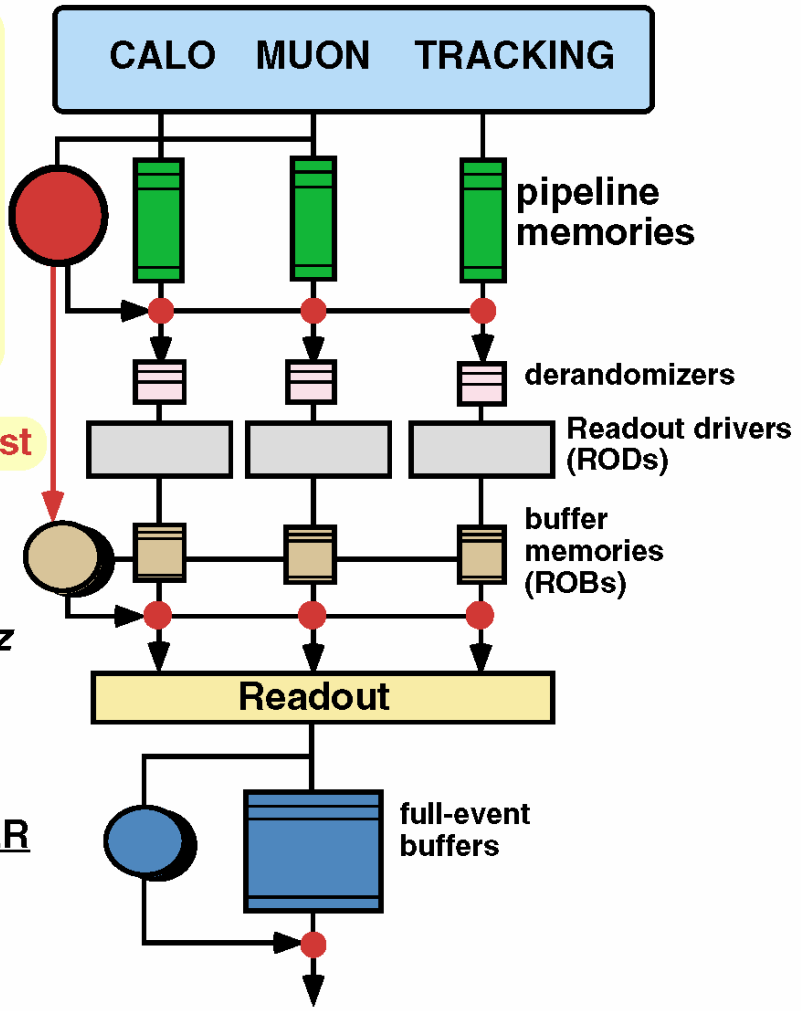
Regions of Interest

LEVEL 2 TRIGGER

100–1000 Hz

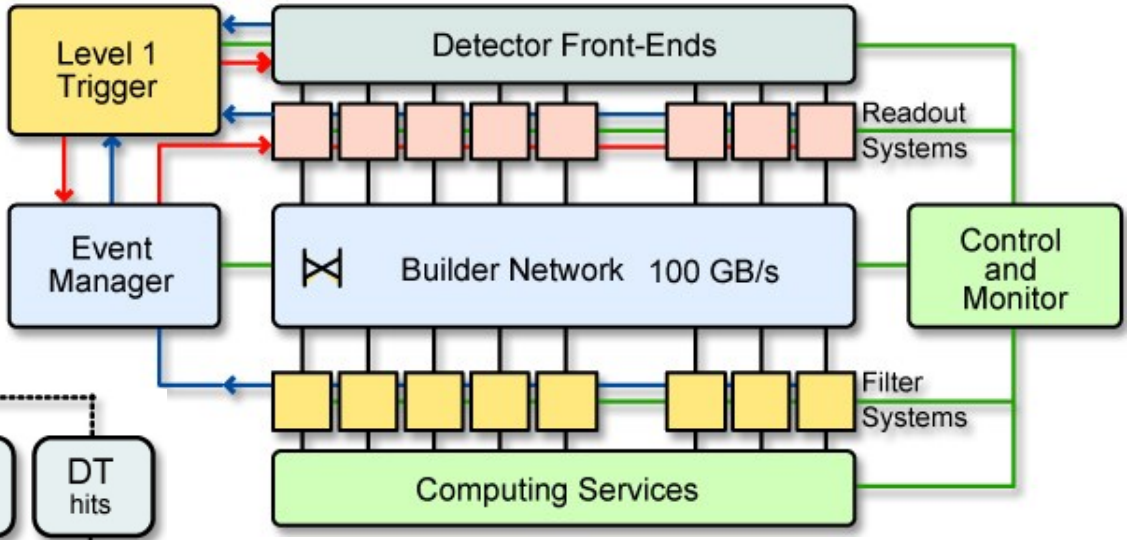
EVENT FILTER

10–100 Hz

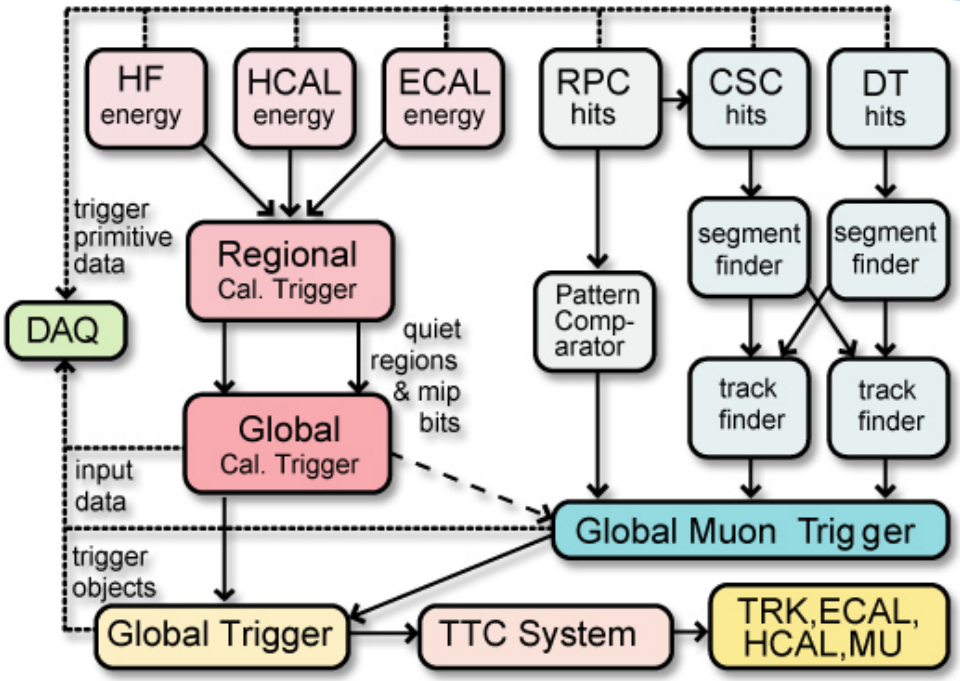


CMS Trig & DAQ for LHC

Overall Trigger & DAQ Architecture: 2 Levels:



Level-1 Trigger:



Interaction rate: 1 GHz

Bunch Crossing rate: 40 MHz

Level 1 Output: 100 kHz (50 initial)

Output to Storage: 100 Hz

Average Event Size: 1 MB

Data production 1 TB/day

SLHC Level-1 Trigger @ 10^{35}

Occupancy

- **Degraded performance of algorithms**
  - Electrons: reduced rejection at fixed efficiency from isolation
  - Muons: increased background rates from accidental coincidences
- **Larger event size to be read out**
  - New Tracker: higher channel count & occupancy $\rightarrow$ large factor
  - Reduces the max level-1 rate for fixed bandwidth readout.

Trigger Rates

- **Try to hold max L1 rate at 100 kHz by increasing readout bandwidth**
  - Avoid rebuilding front end electronics/readouts where possible
    - **Limits: ⟨readout time⟩ (< 10 μs) and data size (total now 1 MB)**
  - Use buffers for increased latency for processing, not post-L1A
  - May need to increase L1 rate even with all improvements
    - **Greater burden on DAQ -- see talk by S. Cittolin**
- **Implies raising E_T thresholds on electrons, photons, muons, jets and use of less inclusive triggers**
  - Need to compensate for larger interaction rate & degradation in algorithm performance due to occupancy

Radiation damage -- Increases for part of level-1 trigger located on detector

SLHC Trigger @ 12.5 ns

Choice of 80 MHz

- Reduce pile-up, improve algorithm performance, less data volume for detectors that identify 12.5 ns BX data
- Be prepared for LHC Machine group electron-cloud solution
- Retain ability to time-in experiment
  - Beam structure vital to time alignment
- Higher frequencies ~ continuous beam

Rebuild level-1 processors to use data "sampled" at 80 MHz

- Already ATLAS & CMS have internal processing up to 160 MHz and higher in a few cases
- Use 40 MHz sampled front-end data to produce trigger primitives with 12.5 ns resolution
  - e.g. cal. time res. < 25 ns, pulse time already from multiple samples
- Save some latency by running all trigger systems at 80 MHz I/O
- Technology exists to handle increased bandwidth

SLHC Trigger Requirements

High-P_T discovery physics

- Not a big rate problem since high thresholds

Completion of LHC physics program

- Example: precise measurements of Higgs sector
- Require low thresholds on leptons/photons/jets
  - Use more exclusive triggers since final states will be known

Control & Calibration triggers

- W, Z, Top events
- Low threshold but prescaled

SLHC Level-1 Trigger Menu

ATLAS/CMS Studies in hep-ph/0204087:

- inclusive single muon p_T > 30 GeV (rate ~ 25 kHz)
- inclusive isolated e/γ E_T > 55 GeV (rate ~ 20 kHz)
- isolated e/γ pair E_T > 30 GeV (rate ~ 5 kHz)
  - or 2 different thresholds (i.e. 45 & 25 GeV)
- muon pair p_T > 20 GeV (rate ~ few kHz?)
- jet E_T > 150 GeV.AND.E_T(miss) > 80 GeV (rate ~ 1-2 kHz)
- inclusive jet trigger E_T > 350 GeV (rate ~ 1 kHz)
- inclusive E_T(miss) > 150 GeV (rate ~1 kHz);
- multi-jet trigger with thresholds determined by the affordable rate

Trig. Primitives: CMS Calorimeter

HF:Quartz Fiber: Possibly replaced

- Very fast - gives good BX ID
- Modify logic to provide finer-grain information
  - Improves forward jet-tagging

HCAL:Scintillator/Brass: Barrel stays but endcap replaced

- Has sufficient time resolution to provide energy in correct 12.5 ns BX with 40 MHz sampling. Readout may be able to produce 80 MHz already.

ECAL: $PBWO_4$ Crystal: Stays

- Also has sufficient time resolution to provide energy in correct 12.5 ns BX with 40 MHz sampling, may be able to produce 80 MHz output already.
- Exclude on-detector electronics modifications for now -- difficult:
  - Regroup crystals to reduce $\Delta\eta$ tower size -- minor improvement
  - Additional fine-grain analysis of individual crystal data -- minor improvement

Conclusions:

- Front end logic same except where detector changes
- Need new TPG logic to produce 80 MHz information
- Need higher speed links for inputs to Cal Regional Trigger

Trig. Primitives: ATLAS Calor.

- F.E. Taylor

LAr: Pileup will be ~ 3.2 X higher @ 10^{35}

- Electronics shaping time may need change to optimize noise response

Space charge effects present for $|\eta|>2$ in EM LAr calorimeter

- Some intervention will be necessary

BC ID may be problematical with sampling @ 25 ns

- May have to change pulse shape sampling to 12.5 ns

Tilecal will suffer some radiation damage $\Delta LY< 20\%$

- Calibration & correction – may be difficult to see Min-I signal amidst pileup

Trig. Prim.: ATLAS Muons

- F.E. Taylor

Muon Detector issues:

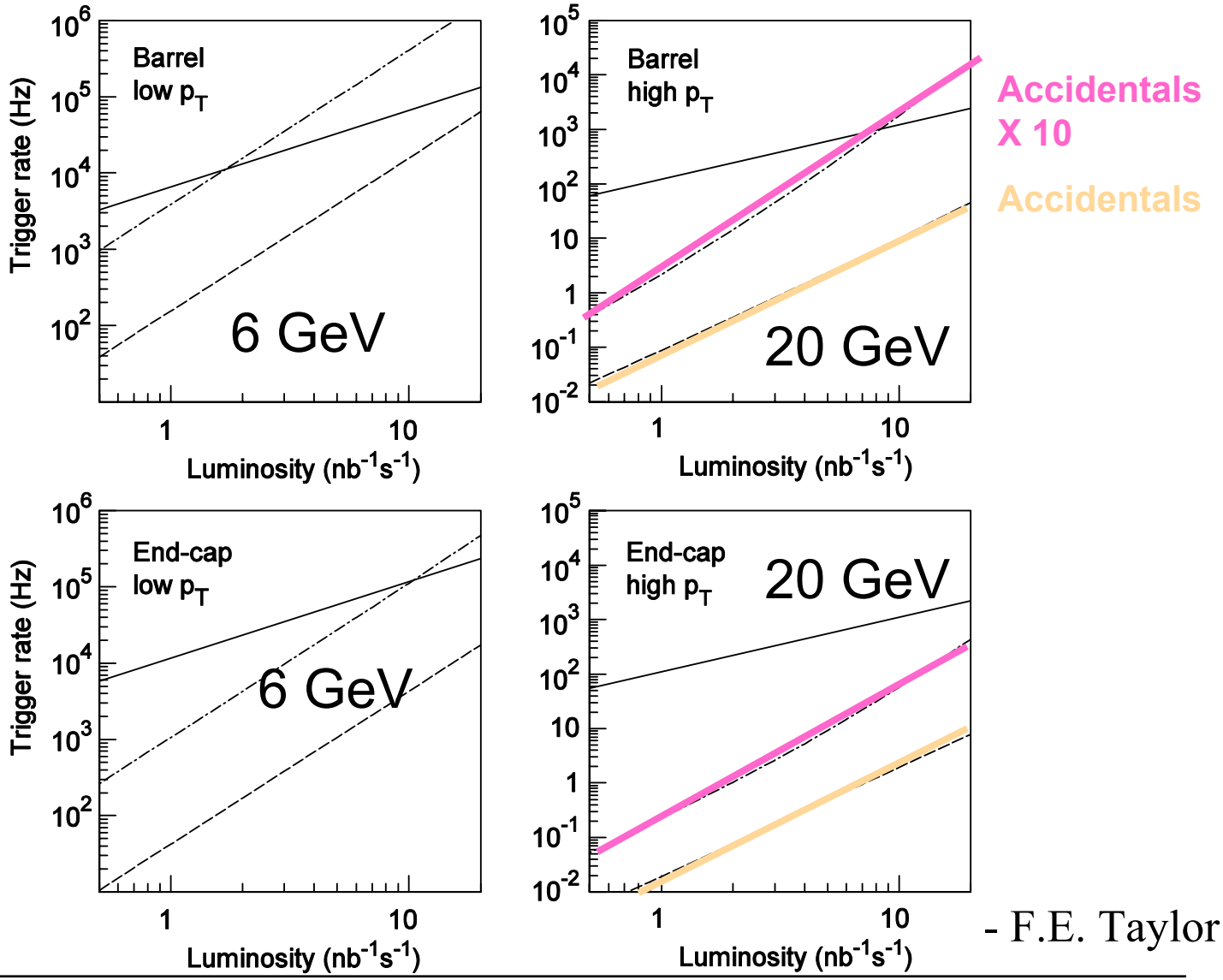
- **Faster & More Rad-Hard trigger technology needed**
  - RPCs (present design) will not survive @ 10^{35}
    - **Intrinsically fast response ~ 3 ns, but resistivity increases at high rate**
  - TGCs need to be faster for 12.5 BX ID…perhaps possible
- **Gaseous detectors only practical way to cover large area of muon system (MDT & CSC) Area ~ 10^4 m^2**
  - Better test data needed on resol'n vs. rate
  - Bkg. γ and neutron efficiencies
  - Search for faster gas $\Rightarrow$ smaller drift time
  - Drive technologies to 10^{35} conditions

Technologies:

- **MDT & CSC & TGC will be stressed – especially high $|\eta|$ ends of deployment, RPCs will have to be replaced**

ATLAS μ Trig. Resolution & Rate

@ 10^{35} (100 nb^{-1} s^{-1}) Trig Rate ~ 10^4 Hz & mostly 'real' if accidental rate nominal – higher thresholds ~ larger fraction of accidentals



- F.E. Taylor

Trig. Prim.: CMS Endcap Muon

4 stations of CSCs: Bunch Crossing ID at 12.5 ns:

- **Use second arriving segment to define track BX**
  - Use a 3 BX window
- **Improve BX ID efficiency to 95% with centered peak, taking 2nd Local Charged Track, requiring 3 or more stations**
  - Requires 4 stations so can require 3 stations at L1
- **Investigate improving CSC performance: HV, Gas, …**
  - If 5 ns resolution $\Rightarrow$ 4 ns, BX ID efficiency might climb to 98%

Occupancy at 80 MHz: Local Charged Tracks found in each station

- **Entire system: 4.5 LCTs /BX**
- **Worst case: inner station: 0.125/BX (others 3X smaller)**
- **P(≥ 2) = 0.7% (spoils di-μ measurement in single station)**
- **Conclude: not huge, but neglected neutrons and ghosts may be under-estimated$\Rightarrow$ need to upgrade trigger front end to transmit LCT @ 80 MHz**

Occupancy in Track-Finder at 80 MHz:

- **Using 4 BX window, find 0.5/50 ns in inner station (every other BX at 25 ns!)**
  - ME2-4 3X smaller, possibly only need 3 BX
- **Need studies to see if these tracks generate triggers**

Trig Primitives: CMS DT & RPC

DT:

- Operates at 40 MHz in barrel
- Could produce results for 80 MHz with loss of efficiency…or…
- Could produce large rate of lower quality hits for 80 MHz for combination with a tracking trigger with no loss of efficiency

RPC:

- Operates at 40 MHz
- Could produce results with 12.5 ns window with some minor external changes.
- Uncertain if RPC can operate at SLHC rates, particularly in the endcap

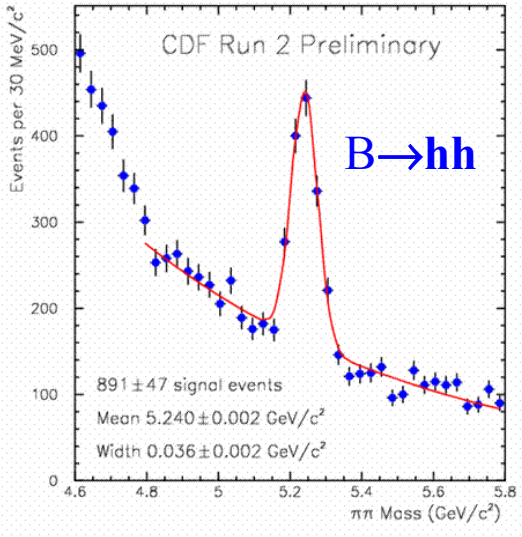
Idea from CDF: eXtremely Fast Tracker + Silicon Vertex Trigger

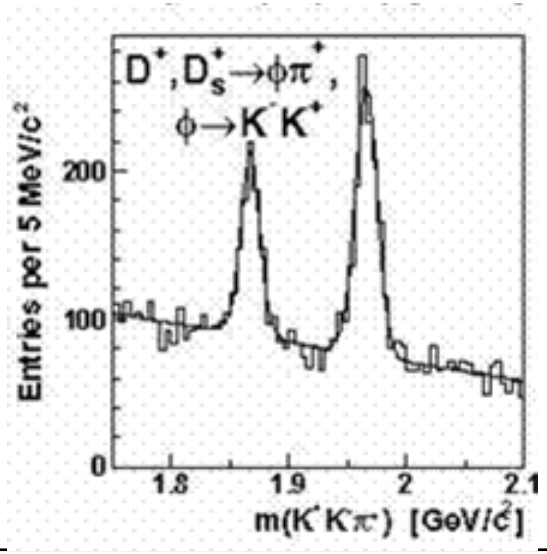
- M. Shochet

Reconstruct all P_T > 1 GeV/c tracks in ~ 20 μsec

- **good P_T resolution; offline quality impact parameter resolution**
- **e, μ fake rejection**
- **3rd generation partons**
  - τ
  - b : reject enormous gluon jet background quickly

In an environment in which b production is 0.1% of hadron production.





Incorporate this into SLHC triggers:
CMS proposal to put into L-1⇒

CMS SLHC L-1 Tracking Trigger
Ideas & Implications for L-1

Additional Component at Level-1

- **Actually, CMS already has a L-1 Tracking Trigger**
  - Pixel z-vertex in $\Delta\eta \times \Delta\phi$ bins can reject jets from pile-up
- **Could provide outer stub and inner track**
  - Combine with cal at L-1 to reject $\pi 0$ electron candidates
  - Reject jets from other crossings by z-vertex
  - Reduce accidentals and wrong crossings in muon system
  - Provide sharp P_T threshold in muon trigger at high P_T
- **Cal & Muon L-1 must produce output with suitable granularity & info. to combine with L-1 tracking trigger**
  - Also need to produce hardware to make combinations

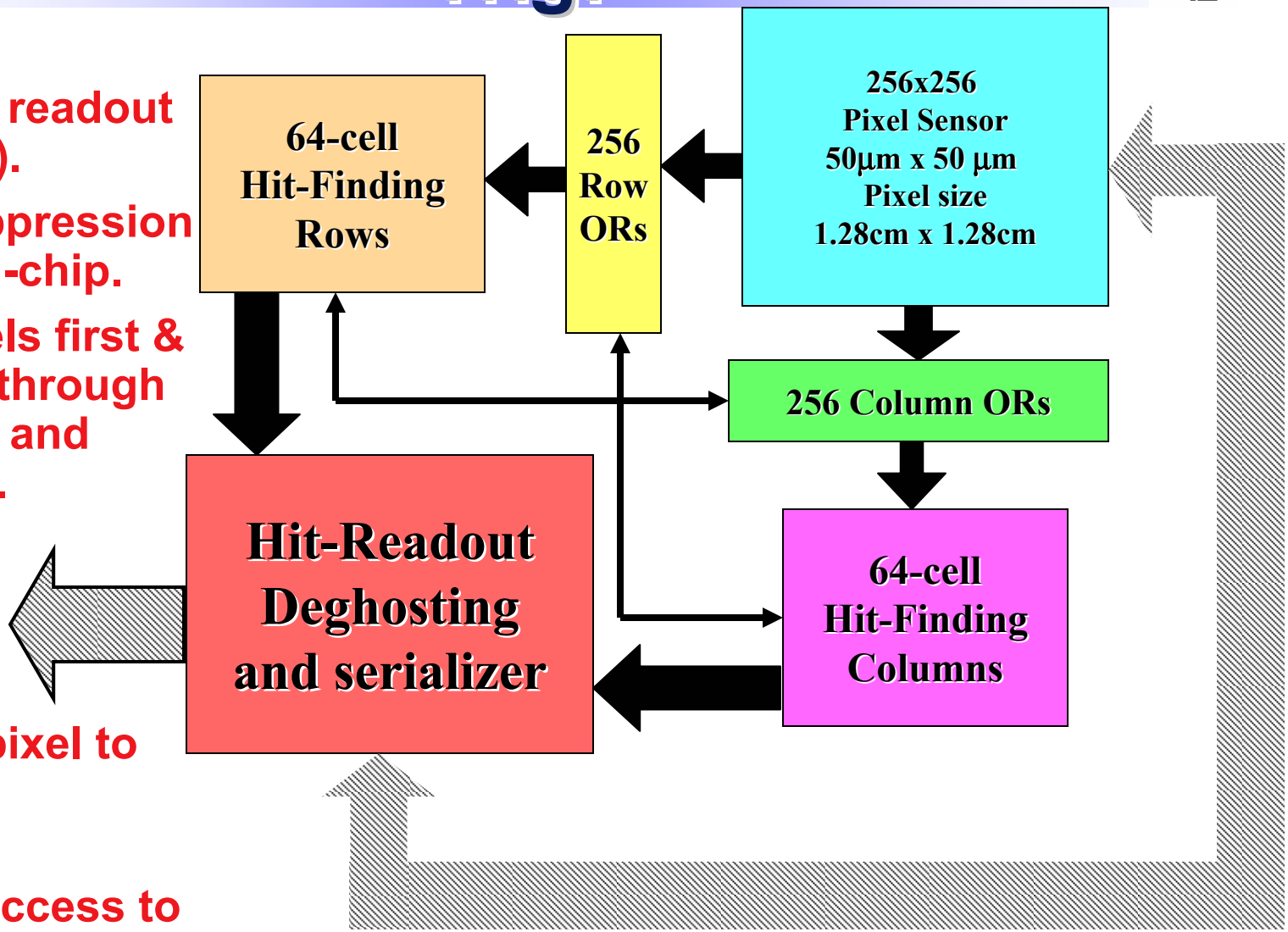
Move some HLT algorithms into L-1 or design new algorithms reflecting tracking trigger capabilities

One strategy: CMS L1 Track Trig.

Assume digital readout (ea. pixel is 0-1).

Apply zero-Suppression & clustering on-chip.

Identify hit pixels first & then loop only through pixels with hits and remove ghosts.



Need pipeline/pixel to allow on-chip processing.

Need random access to read the hits.

- C. Foudas

Tracker R&D Issues

- G. Hall

Higher granularity & more pixels

Material budget

Power

- Increase in channels, power in cables
- Hope for partial relief from smaller feature size technology

Digital readout with sophisticated processing

Radiation Tolerance

- Qualification is time consuming

SEU: Error detection & correction

Large system size & large number of channels

- Automated testing & diagnostics

Design for production

Use of CMS L1 Tracking Trigger

- D. Acosta

Combine with L1 CSC as is now done at HLT:

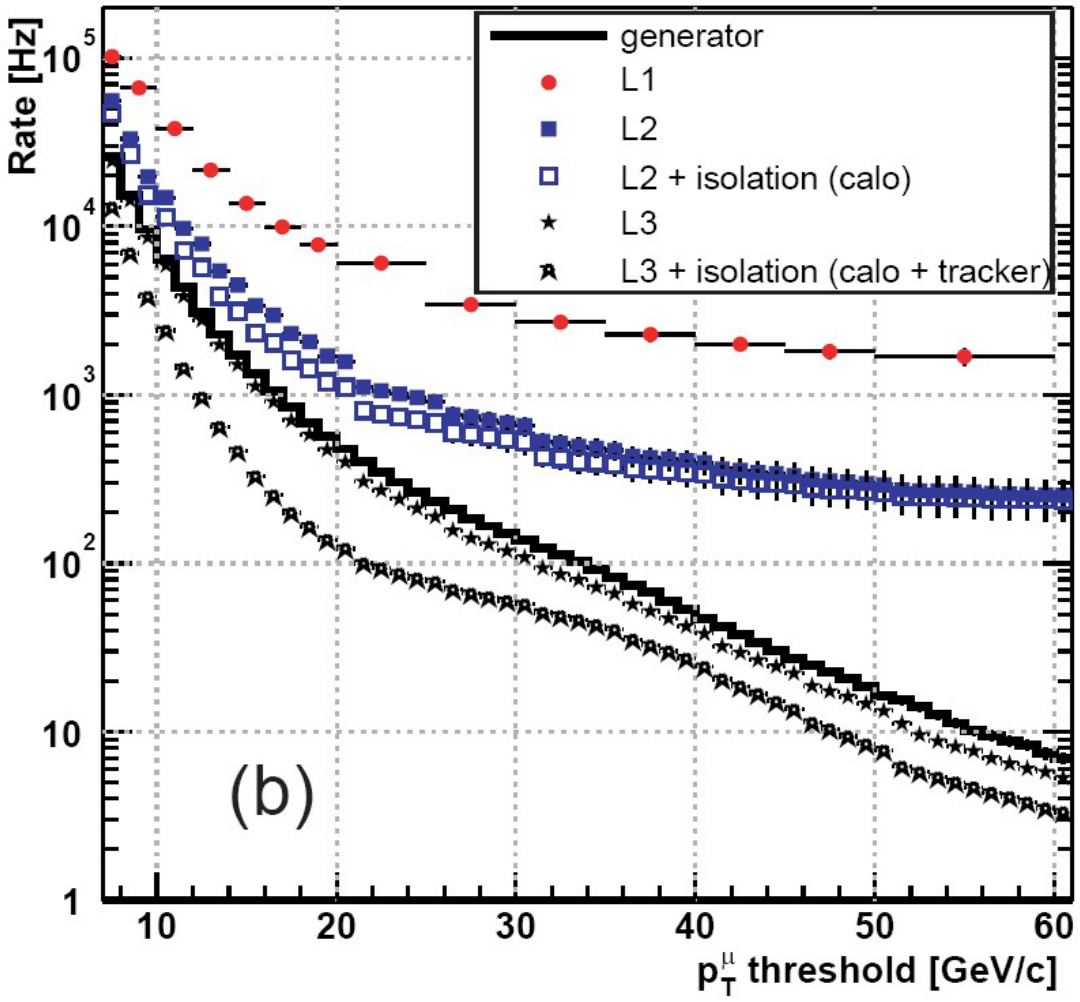
- **Attach tracker hits to improve P_T assignment precision from 15% standalone muon measurement to 1.5% with the tracker**
  - Improves sign determination & provides vertex constraints
- **Find pixel tracks within cone around muon track and compute sum P_T as an isolation criterion**
  - Less sensitive to pile-up than calorimetric information *if* primary vertex of hard-scattering can be determined (~100 vertices total at SLHC!)

To do this requires η–ϕ information on muons finer than the current 0.05–2.5°

- **No problem, since both are already available at 0.0125 and 0.015°**

CMS Muon Rate at $L = 10^{34}$

From DAQ TDR



Note limited rejection power (slope) without tracker information

CMS SLHC Calorimeter Trigger

- S. Dasu

Electrons/Photons:

- Report on finer scale to match to tracks

τ-jets:

- Cluster in 2x2 trigger towers with 2x2 window sliding by 1x1 with additional isolation logic

Jets:

- Provide options for 6x6, 8x8, 10x10, 12x12 trigger tower jets, sliding in 1x1 or 2x2

Missing Energy:

- Finer grain geometric lookup & improved resolution in sums

Output:

- On finer-grain scale to match tracking trigger
  - Particularly helpful for electron trigger

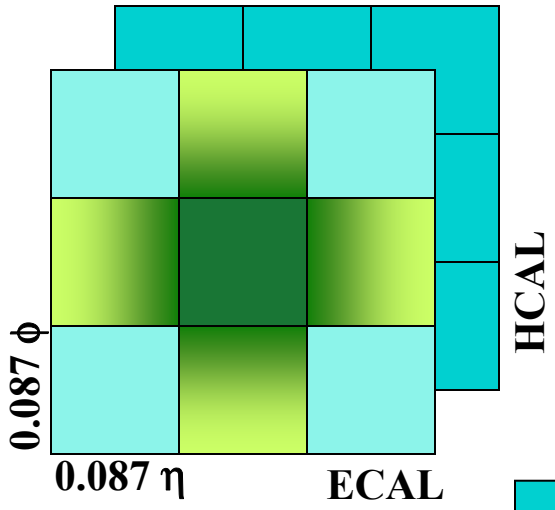
Reasonable extension of existing system

- Assuming R&D program starts soon

CMS SLHC e/γ/τ object clustering

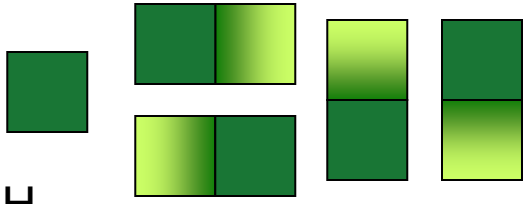
e/γ/τ objects cluster within a tower or two

- **Crystal size is approximately Moliere radius**
  - Trigger towers in ECAL Barrel contain 5x5 crystals
- **2 and 3 prong τ objects don't leak much beyond a TT**
  - But, they deposit in HCAL also

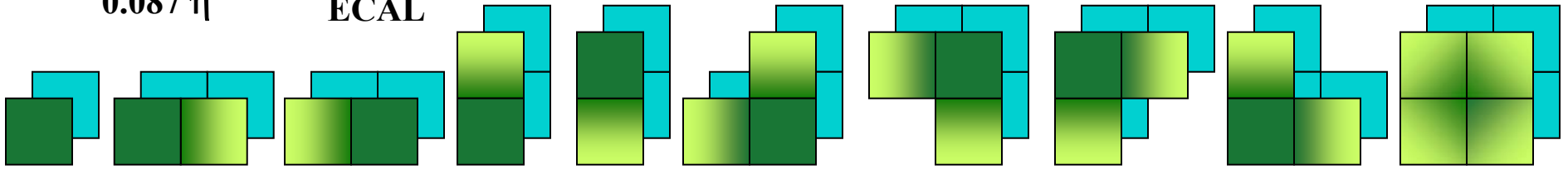


E_T scale: 8-bits

e/γ E_T = 1 x 2 or 2 x 1 sum
e/γ H/E cut for all 9 towers
e/γ isolation patterns:



τ E_T = 3 x 3 sum of E + H
τ isolation patterns include E & H:



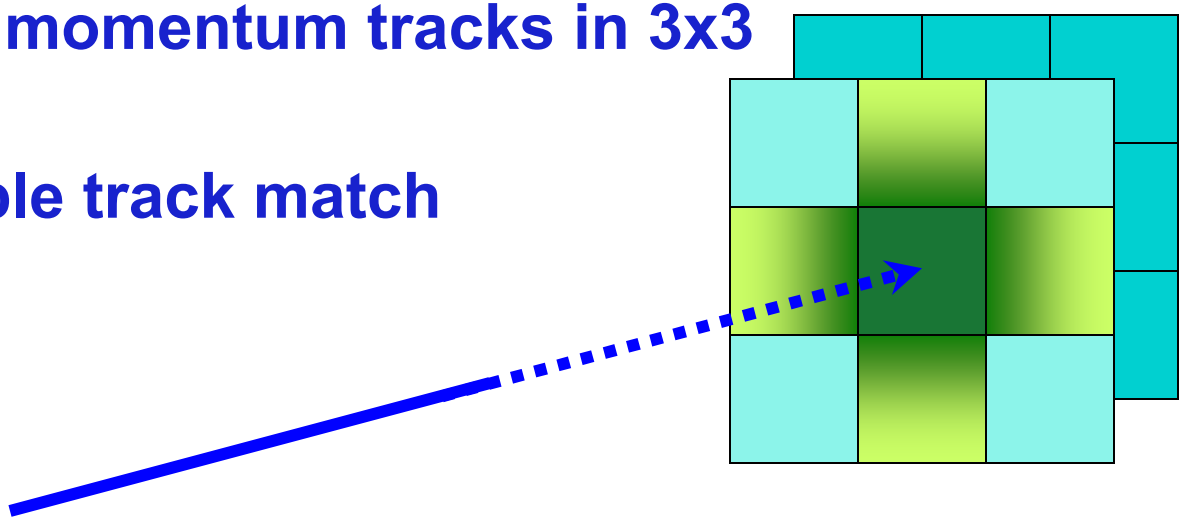
CMS SLHC e / γ / τ object ⇔track correlation

Use e / γ / τ objects to seed tracker readout

- Track seed granularity 0.087ϕ x 0.087η ⇔ 1 x 1
- Track seed count limited by presorting candidates
  - e.g., Maximum of 32 objects?

Tracker correlation

- Single track match in 3x3 with crude P_T (8-bit ~ 1 GeV)
  - Electron (same for muons)
- Veto of high momentum tracks in 3x3
  - Photon
- Single or triple track match
  - Tau



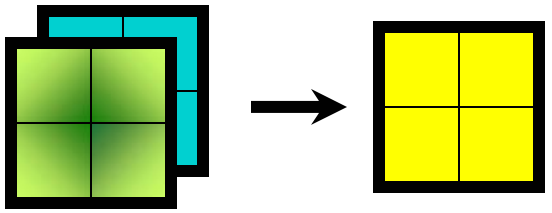
CMS SLHC Jet Clustering

Cluster jets using 2x2 primitives: 6x6, 8x8, 10x10

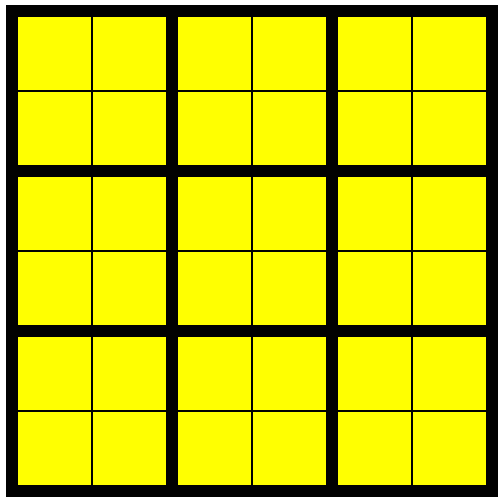
- Start from seeds of 2x2 E+H (position known to 1x1)
- Slide window at using 2x2 jet primitives
- E_T scale 10-bits, ~1 GeV

Jet Primitive is sum of E_T in E/HCAL

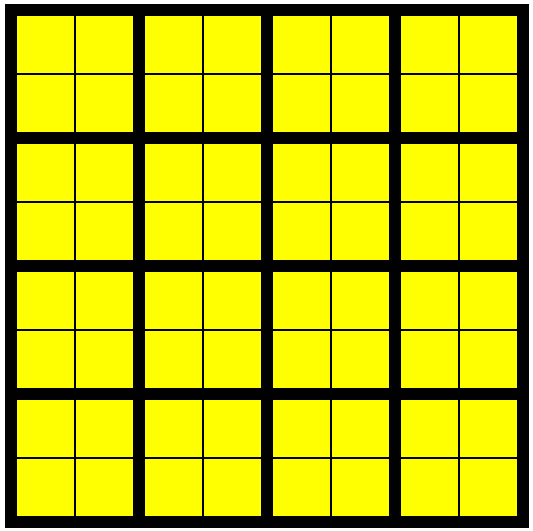
Provide choice of clustering?



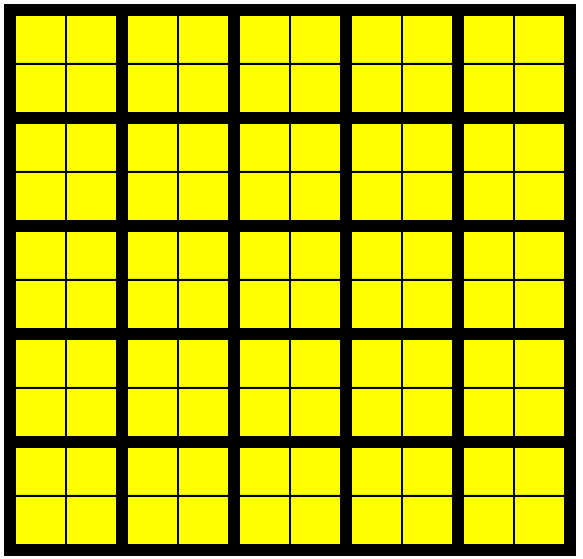
6x6 Jet



8x8 Jet



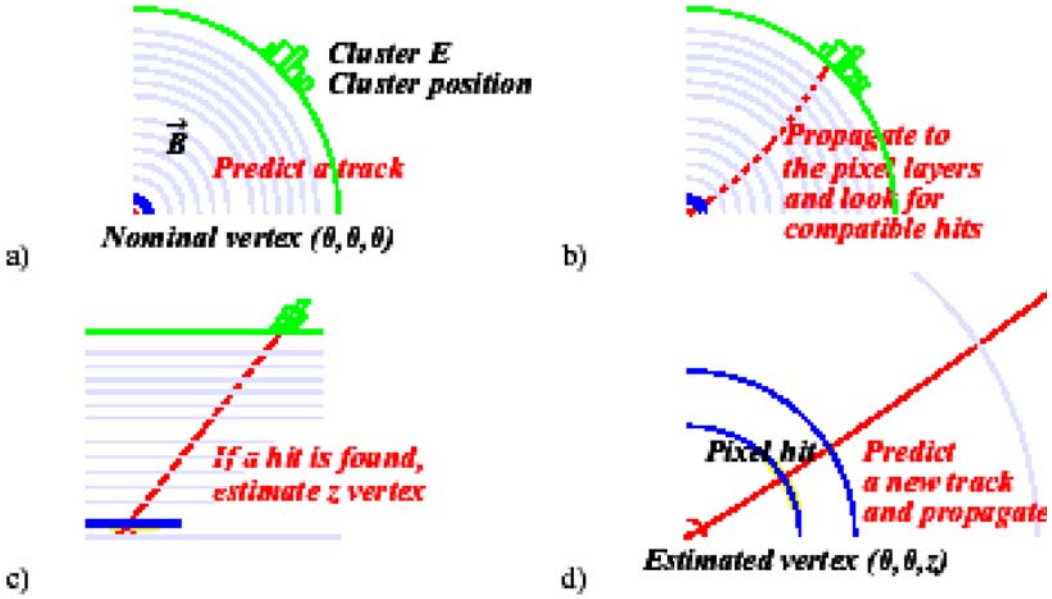
10x10 Jet

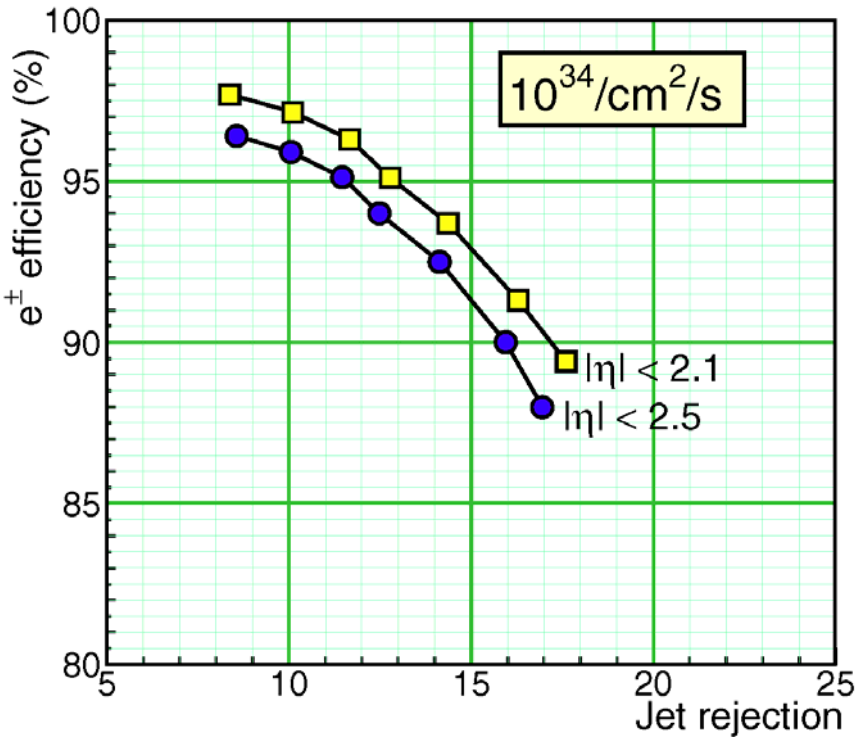


CMS tracking for electron trigger

Present CMS electron HLT

- C. Foudas & C. Seez

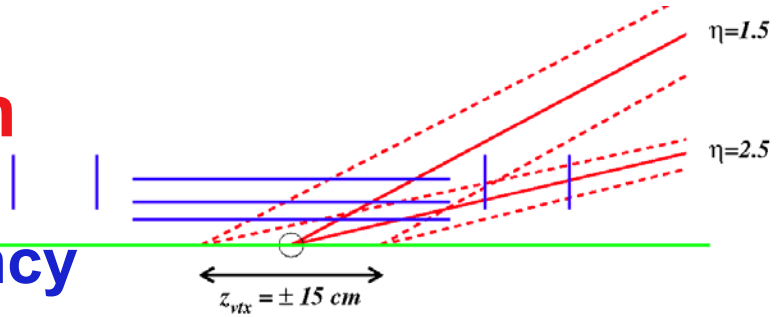




Factor of 10 rate reduction

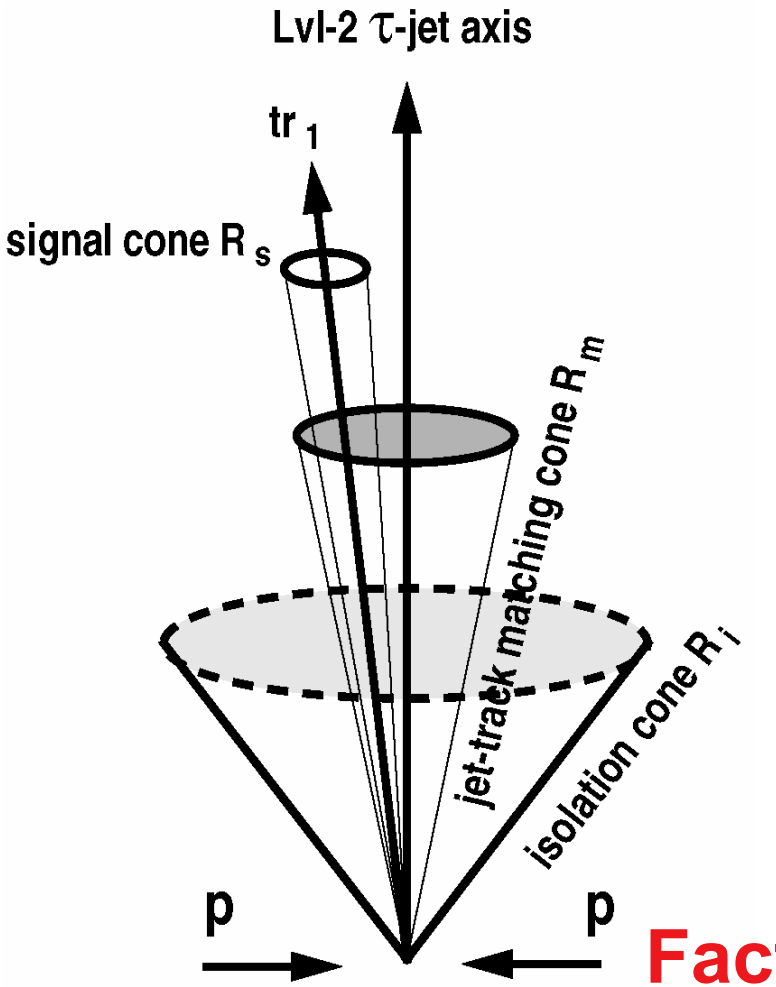
γ: only tracker handle: isolation

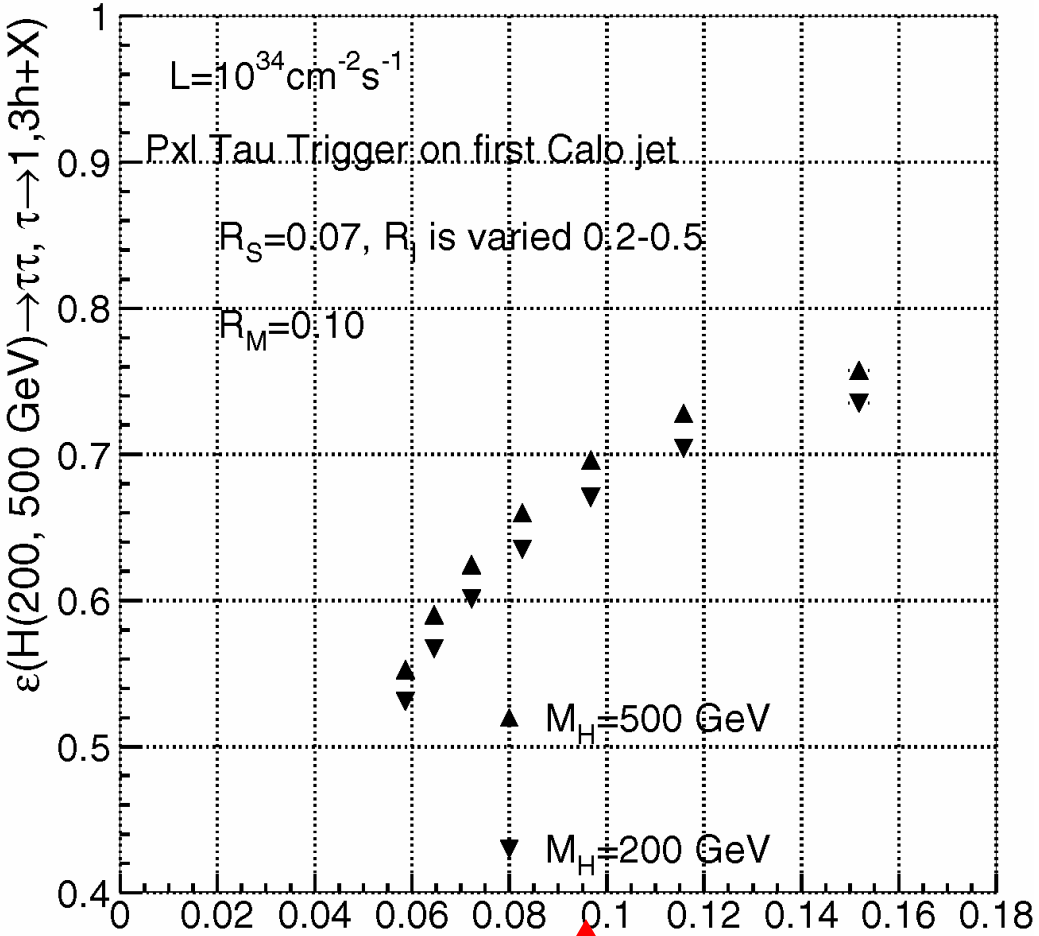
- **Need knowledge of vertex location to avoid loss of efficiency**



CMS tracking for τ-jet isolation

τ-lepton trigger: isolation from pixel tracks outside signal cone & inside isolation cone





Factor of 10 reduction

e / μ / γ / τ / jet object selection

Additional isolation and ghost suppression

- Correlate:1x1 (0.087ϕ x 0.087η) e / μ / γ / τ / jet objects
- Select e / μ / γ / τ / jet candidates with quality bits

H_T determination

- Sum E_T of all objects above threshold

Sorting

- Sort and reduce to top 4 candidates of each type

Output

- Reduced (~ 6 bit?) E_T
- Position information at 1x1 granularity
- Quality bits

CMS SLHC Cal. Trig. Hardware

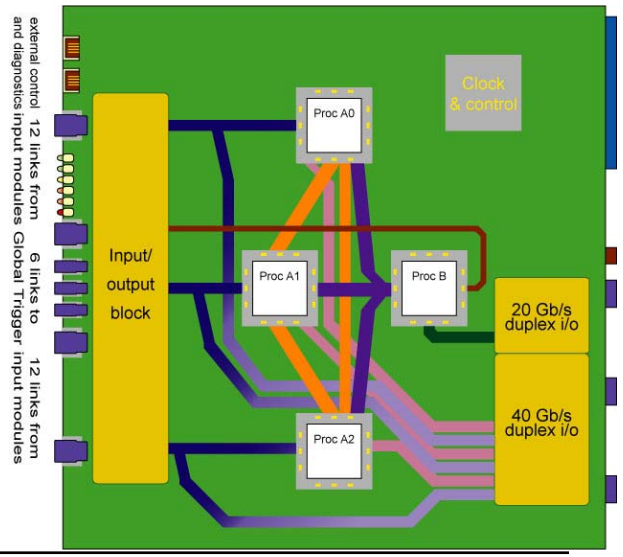
Cards will involve

- **High speed serial input, 32 ~10 Gbps**
- **High performance FPGA for processing**
- **Data routing to FPGA and inter-card sharing**
  - This can vary widely depending on the application
  - We need to generalize this even at the expense of wasting backplane bandwidth on some cards
- **High speed serial output, 4 ~10 Gb/s**

Prototype

- **Extrapolation of Bristol CMS Global Cal. Trig. Processor Module**
  - High density links, new FPGAs: gate count x2-3, I/O speed x2-4

- G. Heath & D. Newbold



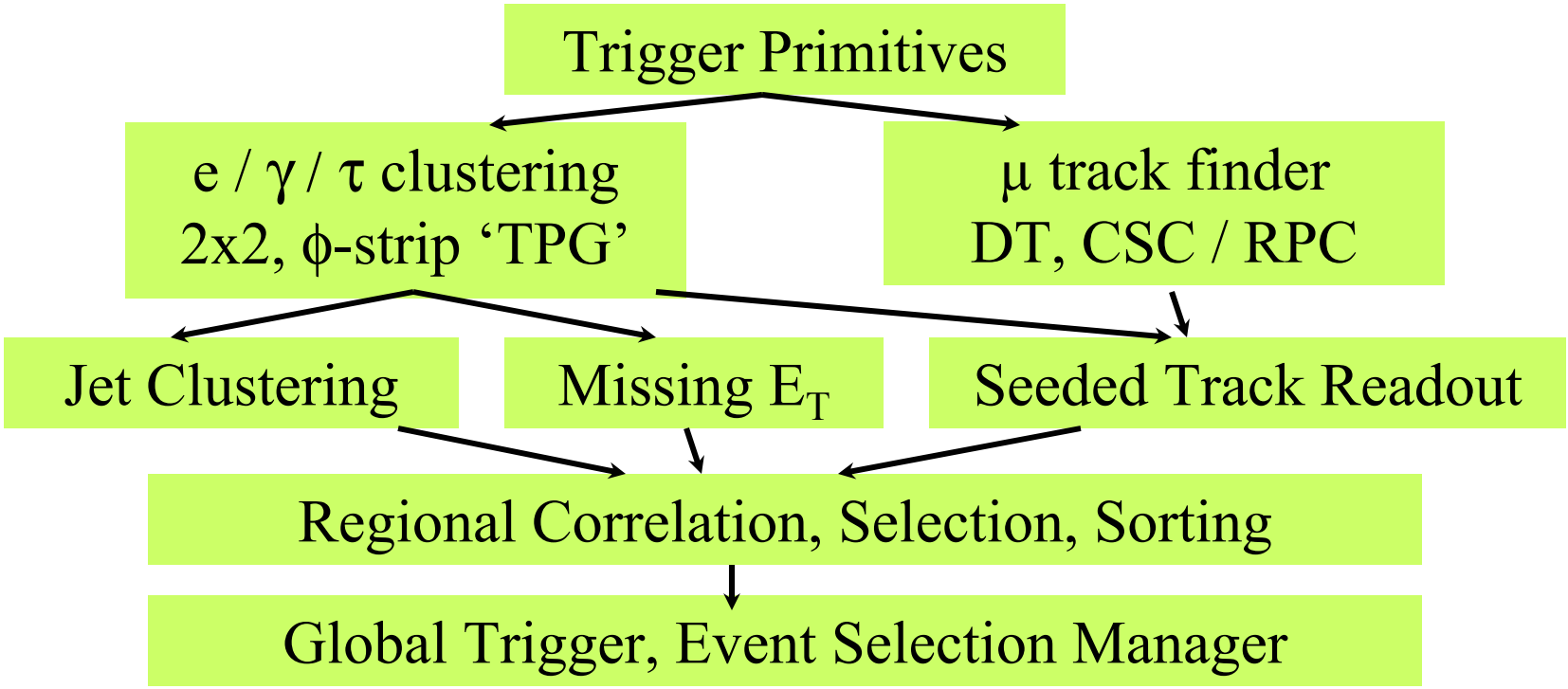
CMS L1 Algorithm Stages

Current for LHC:

TPG ⇒ RCT ⇒ GCT ⇒ GT

Proposed for SLHC:

TPG ⇒ Clustering ⇒ Correlator ⇒ Selector



CMS SLHC Trigger Architecture

LHC:

- Level 1: Regional to Global Component to Global

SLHC Proposal:

- Combine Level-1 Trigger data between tracking, calorimeter & muon at Regional Level at finer granularity
- Transmit physics objects made from tracking, calorimeter & muon regional trigger data to global trigger
- Implication: perform some of tracking, isolation & other regional trigger functions in combinations between regional triggers
  - New “Regional” cross-detector trigger crates
- Leave present L1+ HLT structure intact (except latency)
  - No added levels --minimize impact on CMS readout

CMS Level-1 Latency

CMS Latency of 3.2 μsec becomes 256 crossings @ 80 MHz

- Assuming rebuild of tracking & preshower electronics will store this many samples

Do we need more?

- Yield of crossings for processing only increases from ~70 to ~140
  - It's the cables!
- Parts of trigger already using higher frequency

How much more? Justification?

- Combination with tracking logic
- Increased algorithm complexity
- Asynchronous links or FPGA-integrated deserialization require more latency
- Finer result granularity may require more processing time
- ECAL digital pipeline memory is 256 40 MHz samples = 6.4 μsec
  - Propose this as CMS SLHC Level-1 Latency baseline

CMS SLHC L-1 Trigger Summary

Attempt to restrict upgrade to post-TPG electronics as much as possible where detectors are retained

- **Only change where required -- evolutionary -- some possible pre-SLHC?**

New Features:

- **80 MHz I/O Operation**
- **Level-1 Tracking Trigger**
  - Inner pixel track & outer tracker stub
  - Reports "crude" P_T & multiplicity in ~ 0.1x 0.1 $\Delta\eta \times \Delta\phi$
- **Regional Muon & Cal Triggers report in ~ 0.1 x 0.1 $\Delta\eta \times \Delta\phi$**
- **Regional Level-1 Tracking correlator**
  - Separate systems for Muon & Cal Triggers
  - Separate crates covering $\Delta\eta \times \Delta\phi$ regions
  - Sits between regional triggers & global trigger
- **Latency of 6.4 μsec**

Technologies for SLHC Trig.

Complicated Algorithms & Low Latency:

- FPGA's: faster, more logic
  - Less custom logic -- programmable
- Faster and larger memories

Moving more data at higher speed:

- Link technology: speed & integration
- Backplane technology: connectors & newer interconnect technology

Higher Crossing Frequency:

- High speed clocking: low jitter - design for links

Overall Complexity:

- Design for test, diagnostics, algorithm validation

FPGA Technology

Available Now from Xilinx & Altera (- M. Matveev) :

- 8M Usable Gates
- 1500 Fine Pitch Ball Grid Array Pacakges
- 1200 (Altera) or 1100 (Xilinx) I/O pins
- Core Voltage 1.5 V
- Flexible internal clock management
- No problem to run at 80 MHz

Upgrade:

- Logic Speed, Usable Gates, Logic Volume plenty
- Use of these devices becomes difficult, limiting factor
  - Packaging, routing, mounting, voltages all difficult
  - Need to explore new I/O techniques - built in serdes?

Data Link Architecture

Synchronous or Asynchronous?

- **Do we keep all links running synchronously at 80 MHz or do we allow arbitrary link frequencies as high as available and put FIFOs for resynchronization at input and output**
- **Advantage: use the latest link and low jitter crystal clocking technology**
- **Disadvantage: requires extra synchronization circuitry**
  - Latency for synchronization
  - Need to keep bunch crossing number with data, check it and report/correct errors
  - Extra circuitry and failure points

Data Link Technology

Integration:

- Discrete deserializers vs. integration in FPGAs
- Issue: deserializer latency

Connections:

- CAT6,7,8 cables for 1G and 10G Ethernet
- Parallel Optical Links
- Parallel LVDS at 160 MHz

Backplanes:

- Use cable deserializer technology
- Issues: latency for deserialization and circuitry for synchronization

Power:

- Providing power & cooling infrastructure a challenge

SLHC DAQ

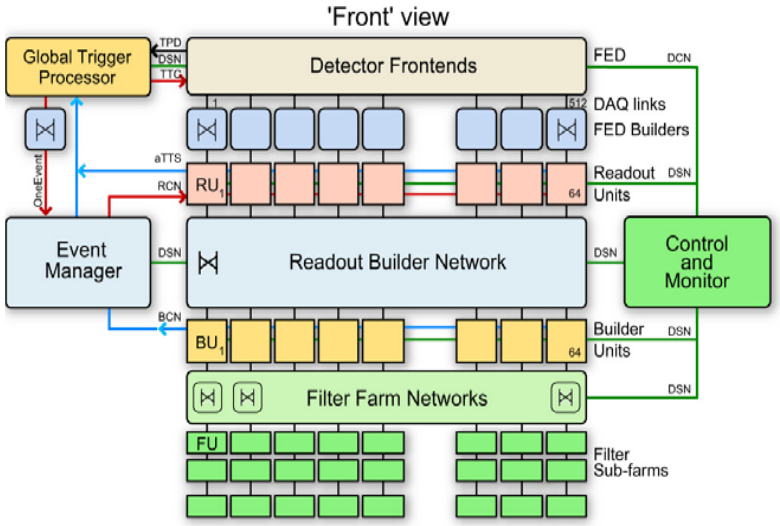
SLHC Network bandwidth at least 5-10 times LHC

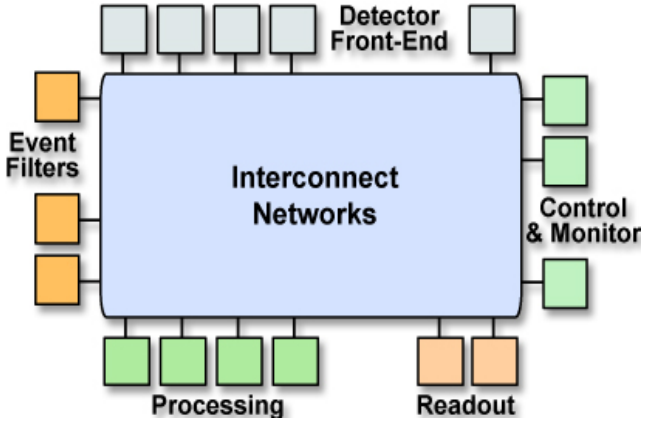
- Assuming L1 trigger rate same as LHC
- Increased Occupancy
- Decreased channel granularity (esp. tracker)

Upgrade paths for ATLAS & CMS can depend on present architecture

- ATLAS: Region of Interest based Level-2 trigger in order to reduce bandwidth to processor farm
  - Opportunity to put tracking information into level-2 hardware
  - Possible to create multiple slices of ATLAS present RoI readout to handle higher rate
- CMS: scalable single hardware level event building
  - If architecture is kept, requires level-1 tracking trigger

CMS DAQ: Possible structure upgrade





- S. Cittolin

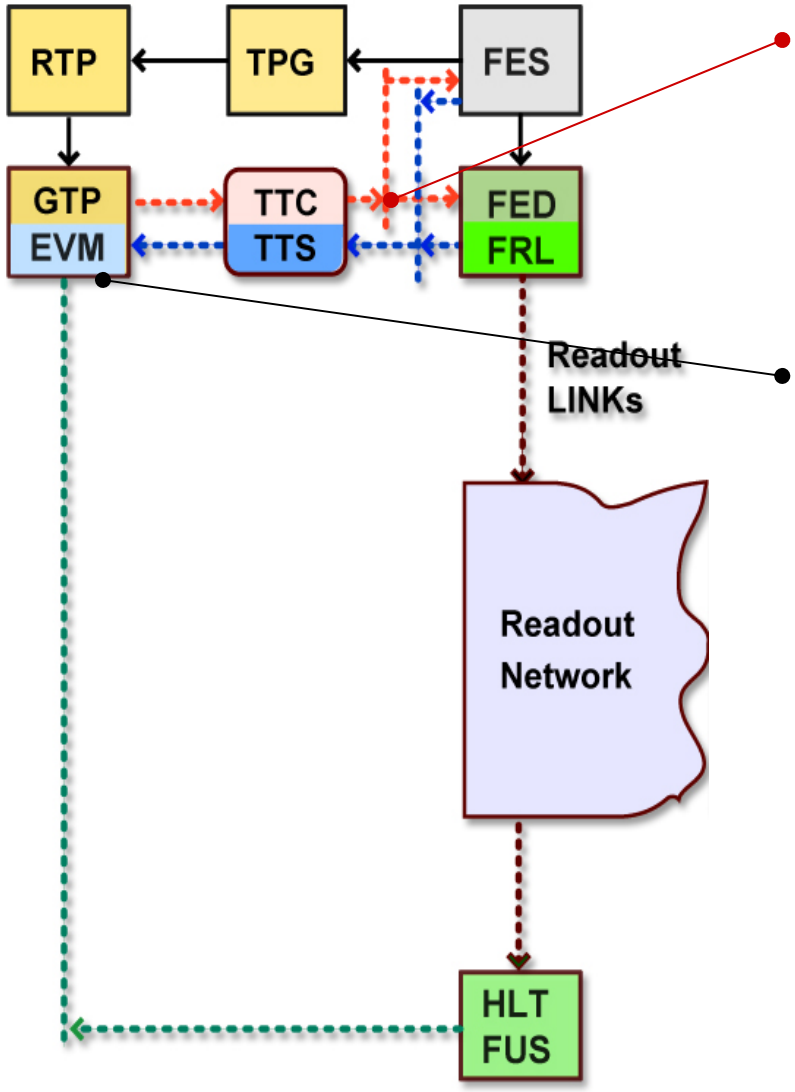
LHC DAQ design:

A network with Terabit/s aggregate bandwidth is achieved by two stages of switches and a layer of intermediate data concentrators used to optimize the EVB traffic load.
RU-BU Event buffers ~100GByte memory cover a **real-time interval of seconds**

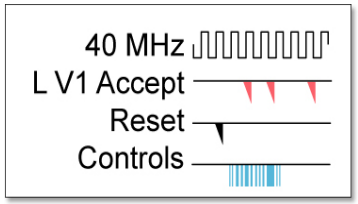
SLHC DAQ design:

A **multi-Terabit/s network** congestion free and scalable (as expected from communication industry).
In addition to the Level-1 Accept, the Trigger has to transmit to the FEDs additional information such as the event type and the event destination address that is the processing system (CPU, Cluster, TIER..) where the event has to be built and analyzed.
The event fragment delivery and therefore the **event building will be warranted by the network protocols** and (commercial) network internal resources (buffers, multi-path, network processors, etc.)
Real time buffers of Pbytes temporary storage disks will cover a **real-time interval of days**, allowing to the event selection tasks a better exploitation of the available distributed processing power.

Distribute Time, L-1,Trigger INFO



LHC-TTC signals from GTP to FED
+ INFO: Trigger type Filter ID…



The Event Manager and Global Trigger Processor must have a tight interface
The EVM will update the 'list' of the available event filter services (CPU-IP, Farms, Tiers, etc.) where to send the events in function of their type.
This information will be embedded in the event fragment and sent into the DAQ net which, by construction, will take care of the event building at destination.

This control logic must process new events at 100 kHz → R&D

TTC for SLHC

80 MHz:

- Provide this capability "just in case" SLHC can operate at 80 MHz
- Provide output frequencies close to that of logic
  - What frequencies are needed?

Drive High-Speed Links

- Design to drive next generation of links
  - Build in very good peak-to-peak jitter performance

Transmit additional data with the Level-1 accept?

- Trigger type: special immediate readout handling?
- Even more…event building…CMS DAQ upgrade

New SLHC TTC System

Fast Controls (TTC-TTS trigger/readout signal loop):

- **Provides Clock, L1A, Reset, BC0 in real time for each crossing**
- **Transmits and receives fast control information**
- **Provides interface with Event Manager, Trigger Throttle System**
  - With each L1A (@ 100 kHz), each front end buffer receives IP address of node to transmit its data fragment to.
  - The event manager transmits event building information in real time at the crossing frequency using the new TTC system.

Upgrade:

- **Extend Level-1 information distribution to/from front-end, TTC and Trigger Throttle System (TTS)**

R&D:

- **Develop a Trigger Information Distribution System**
- **A GHz TTC system or an ancillary fast message distribution system (Mega messages/s)**

SLHC DAQ: Readout

Front End: more processing, channels, zero suppression

- Expect VLSI improvements to provide this
- But many R&D issues: power reduction, system complexity, full exploitation of commercial data-communications developments.

Data Links: Higher speeds needed

- Rx/Tx available for 40G, electronics for 10G now, 40G soon, accepted protocols emerging: G-ethernet, Fibre Channel, SDH/Sonet
- Tighter integration of link & FE --R&D on both should take place together

Radiation tolerance: major part of R&D

- All components will need testing
- SEU rate high: more error detection & correction

SLHC DAQ R&D

Data Sources & Readout Buffers

- Use of busses for data transfer: backplanes & cables
- R&D on high speed backplanes & serial links

Higher Level Triggers

- More selective algorithms since HLT algorithms move to Level-1 must perform with higher occupancy & poorer isolation ⇒ needs physicist work.
- Needs increased CPU, I/O, local storage, memory ⇒ depend on industry developments

Increasing complexity

- Increasing numbers of components, operations, stages
- Needs more sophisticated controls & diagnostics ⇒ needs industrial tools ⇒ suggests adoption of commercial designs where possible

SLHC Trigger & DAQ Summary

SLHC Program has much promise

Creative ideas already appearing for SLHC Trigger & DAQ

- Fast tracking triggers at RoI or L1
- New DAQ architectures
- Evolutionary: some could be implemented pre-SLHC

Timescale of 2014 means R&D needs to start soon

- e.g. CMS efforts combining new tracker & trigger designs, micro-electronics & power management, opto-electronics & system architectures
- Realistic simulation of physics signals
- Technologies: FPGAs, Data-Links, Clocking, Backplanes…