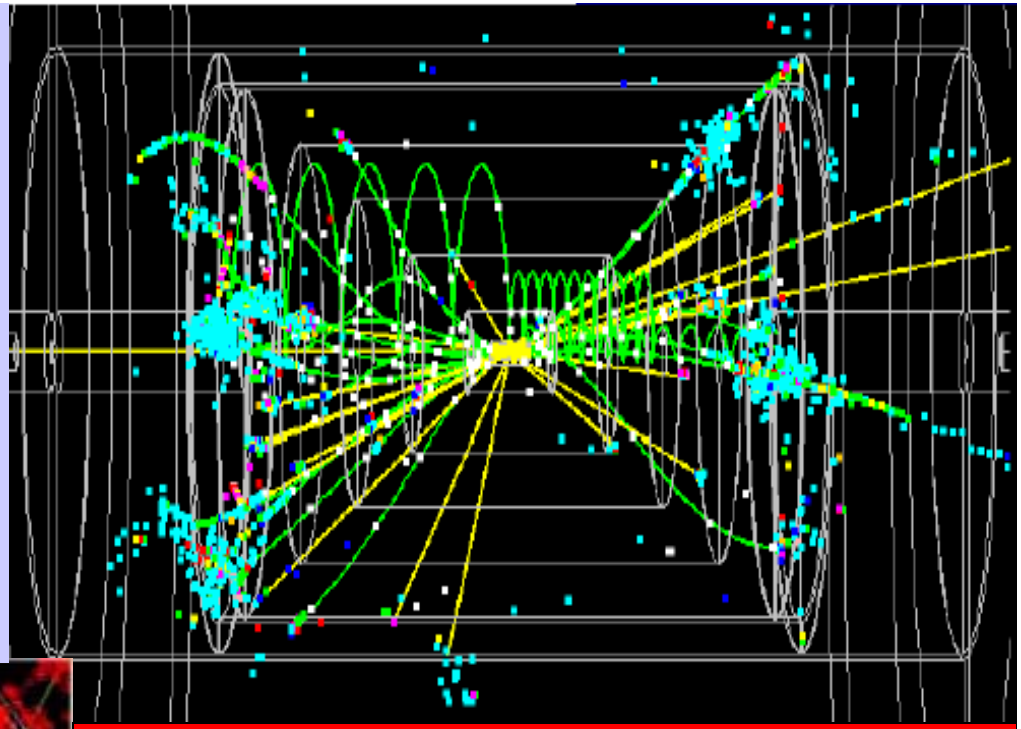
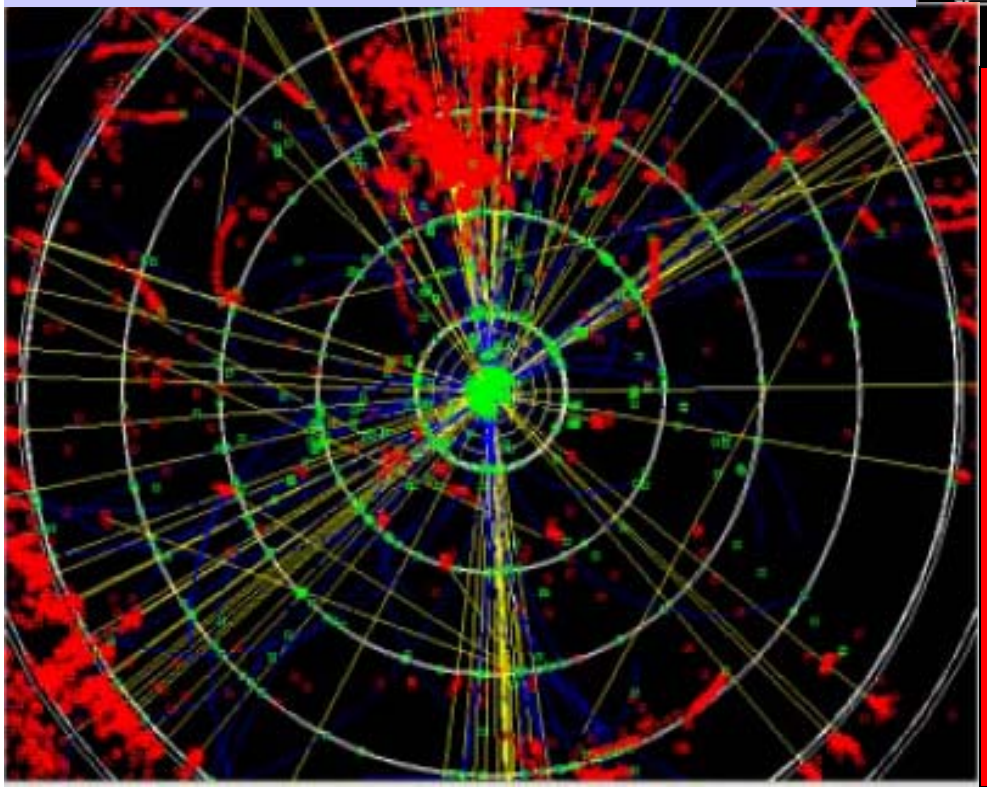
R&D on Front-End Electronics for Linear Collider Detector Applications



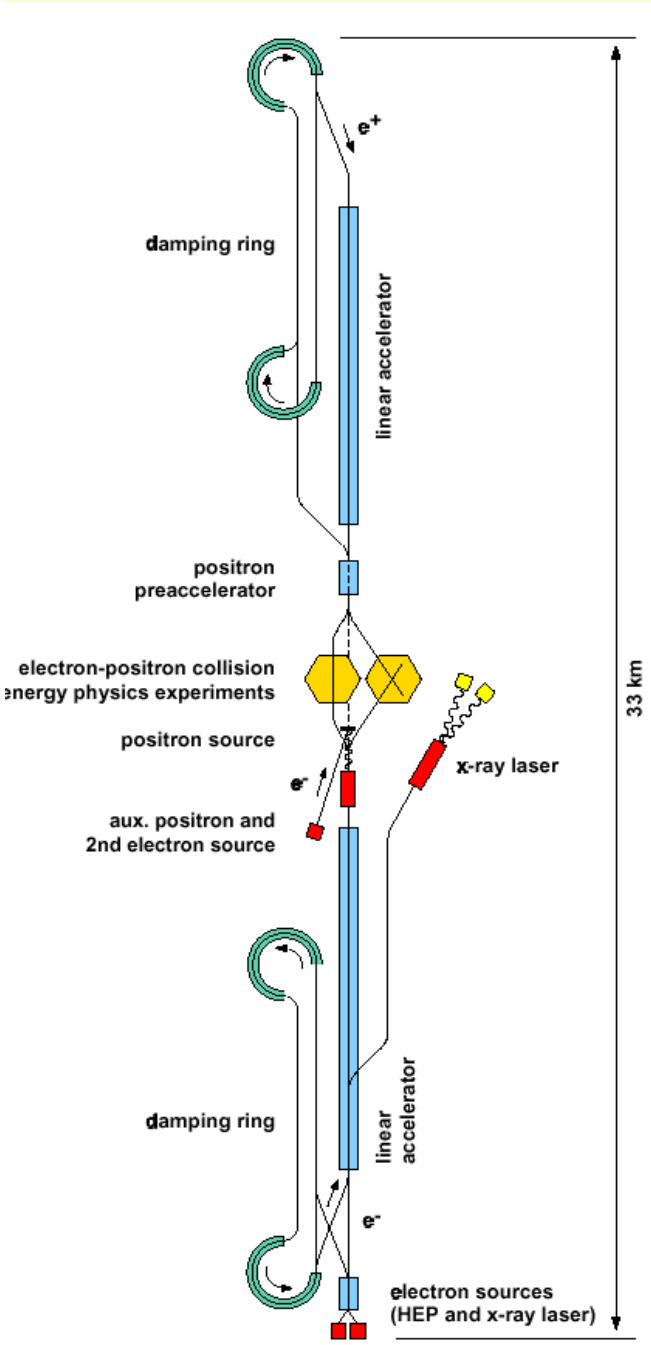


Bruce Schumm

LECC2004 Workshop

Boston, Mass.

September 13, 2004



Principle 1:

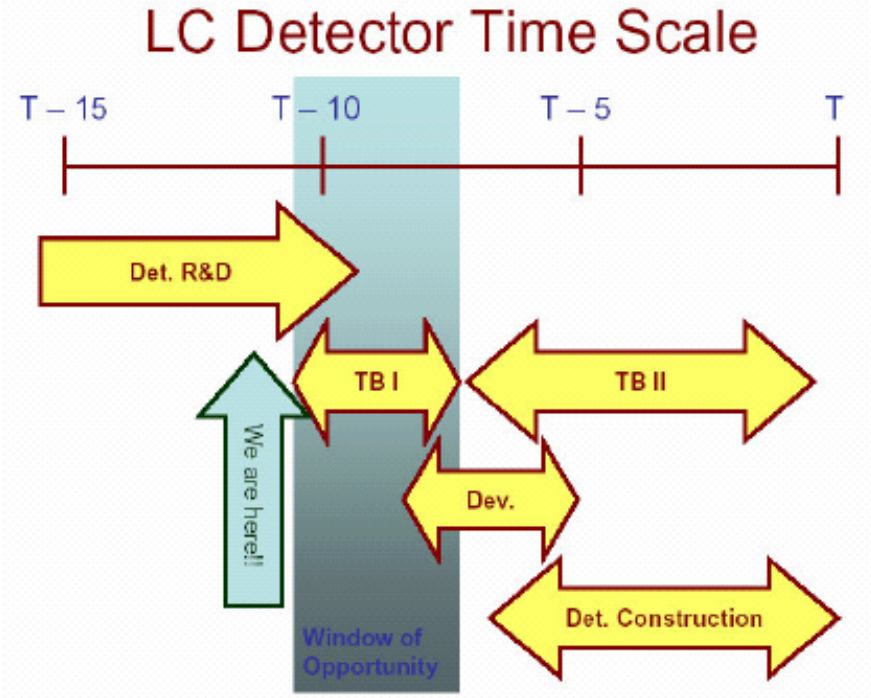
The Linear Collider is not the LHC.

$$E_{cm}^{LHC} = 14\,TeV \qquad E_{cm}^{LC} \approx 0.5\,TeV$$

What the LC lacks in brute-force discovery reach, it must make up with finesse ➔ the LC requires a precision detector, and the electronics to instrument it.

To understand the need for R&D on front-end electronics for the Linear Collider, it is essential to consider the physics one wants to do.

By the way… the time frame for this R&D is surprisingly current

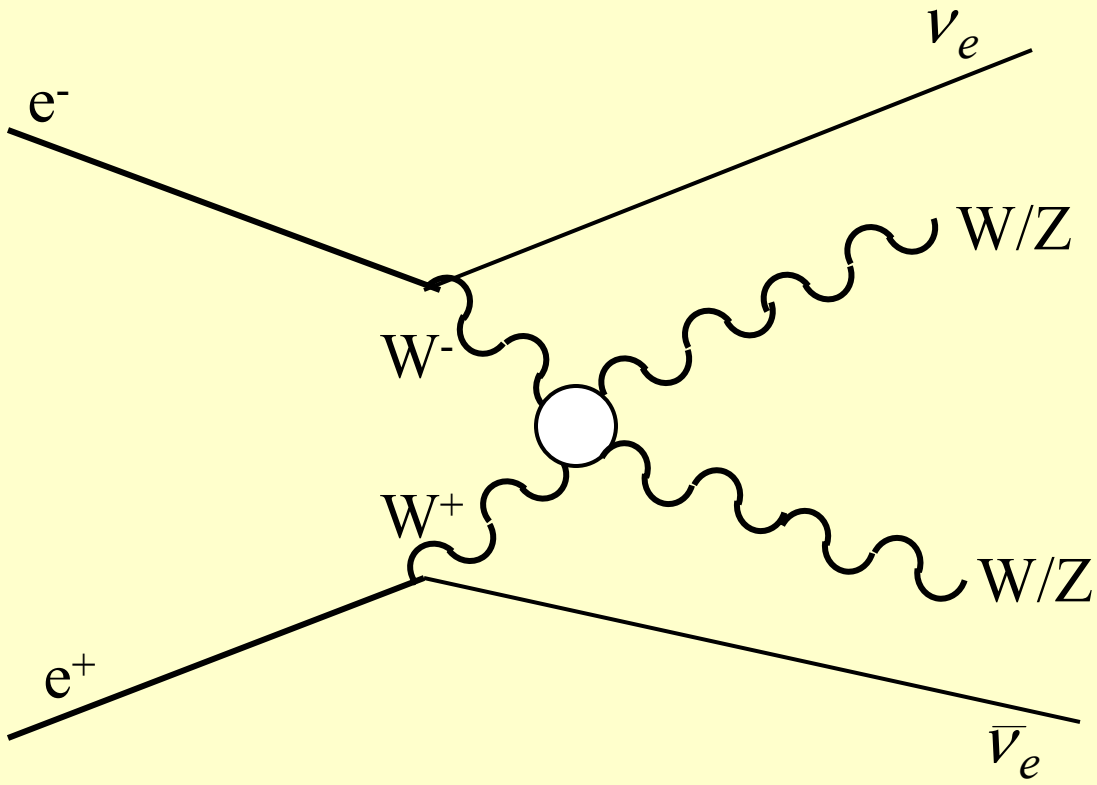


Jae Yu, UT Arlington

Time	T=2015	Tasks
T – >10~11	Before 2005	Detector R&D
T – 10~11	2005~6	Test Beam I
T – 8~9	2006~7	•Detector Technology chosen. •Detector Development and design begins
T – 6	2009	Detector Construction begins Test Beam II (Calibration)
T	2015	LC and Detector ready

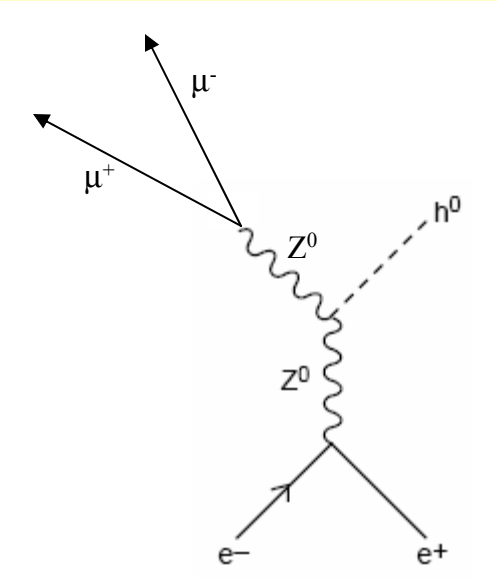
Linear Collider Physics

Given what we have discovered so far, for high enough energy, this process will happen with greater than unit probability. ➔ Our current understanding is incomplete!



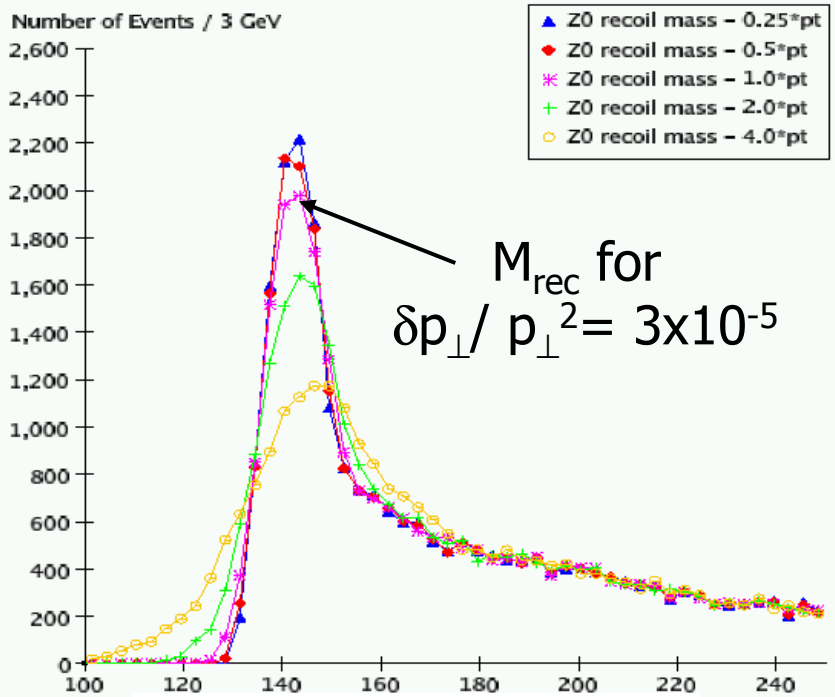
We need some-thing new to put in the circle. Here are some thoughts…

THE HIGGS (h^0)

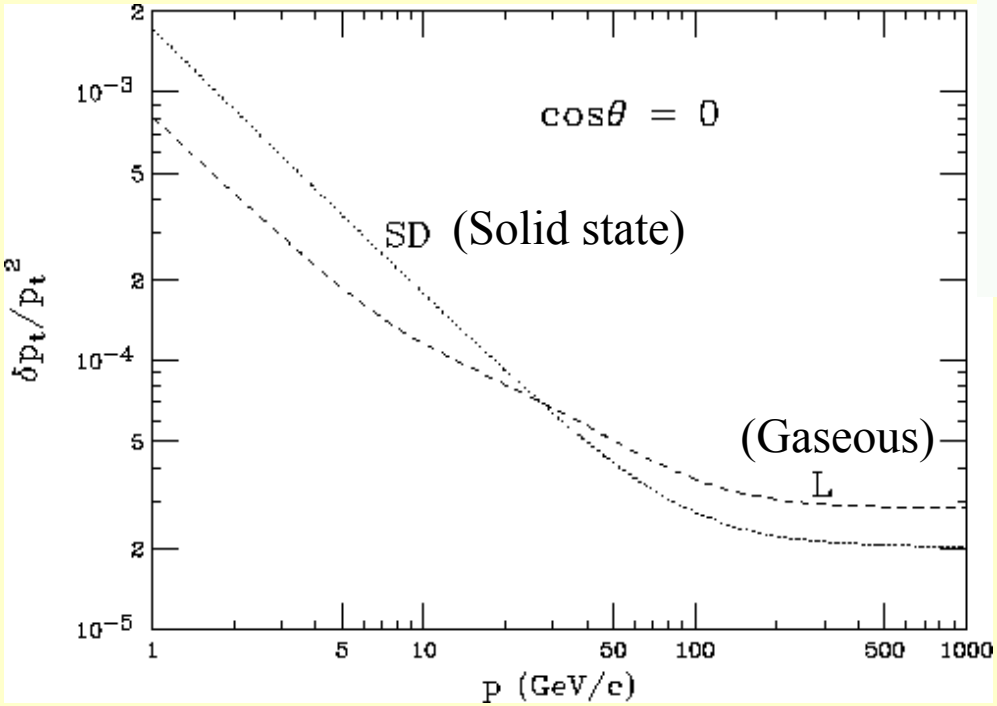


LC Physics demands precise tracking

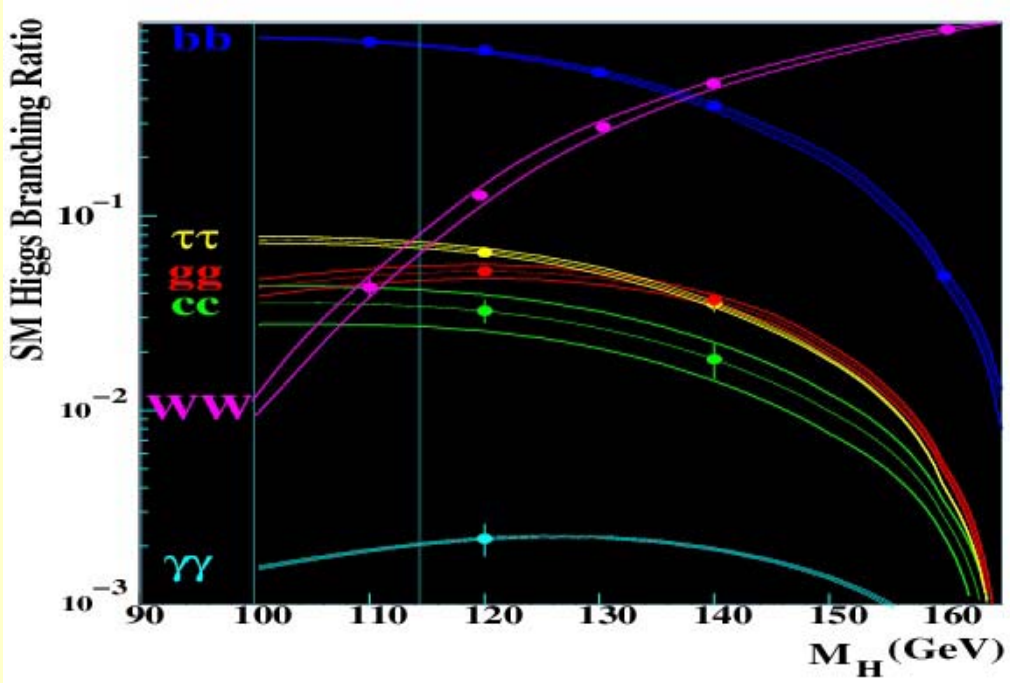
Haijun Yang, Michigan



Mass Recoiling against Z^0

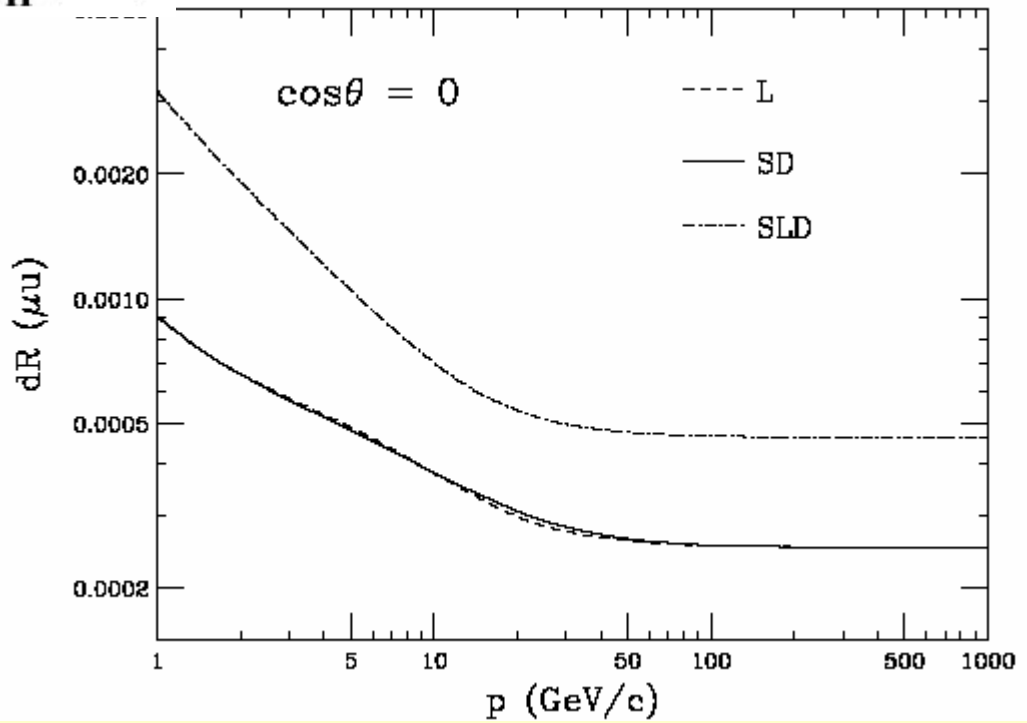


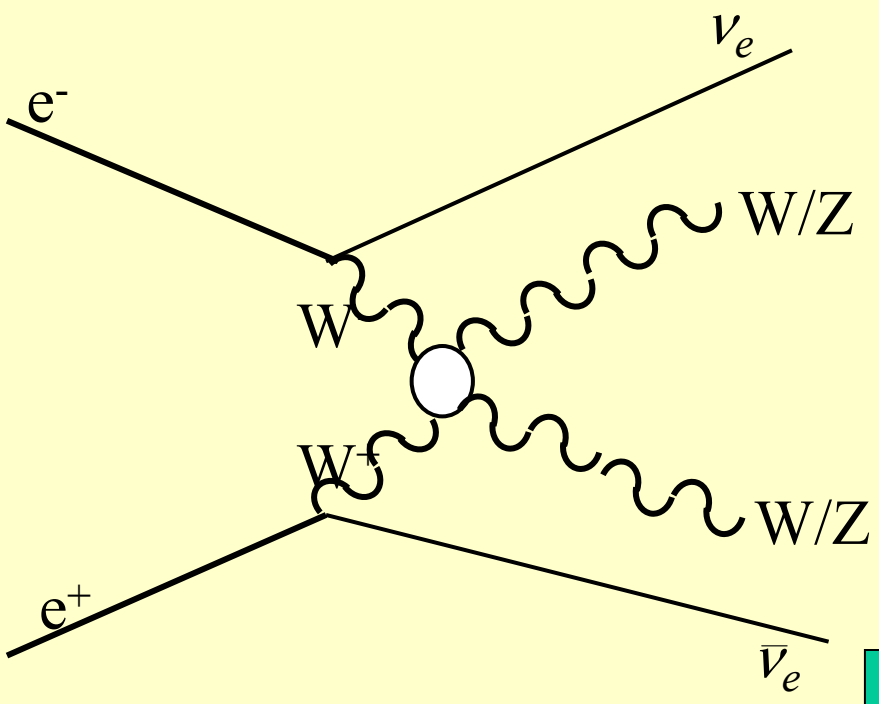
Precision demands state-of-the-art central tracker resolution



The LC must do more than just confirm LHC's Higgs discovery. It must probe Higgs properties with the precision needed to detect subtle new physics scenarios (SUSY, Little Higgs, etc.)

Model-independent branching fractions require unprecedented bottom and charm tagging ➔ ultraprecise three-dimensional vertexing

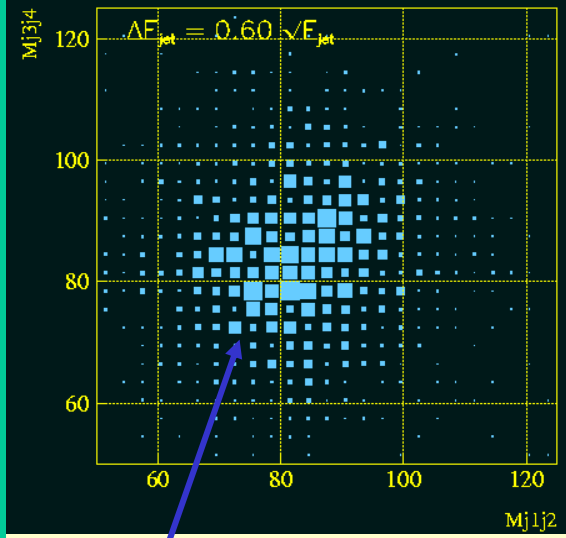


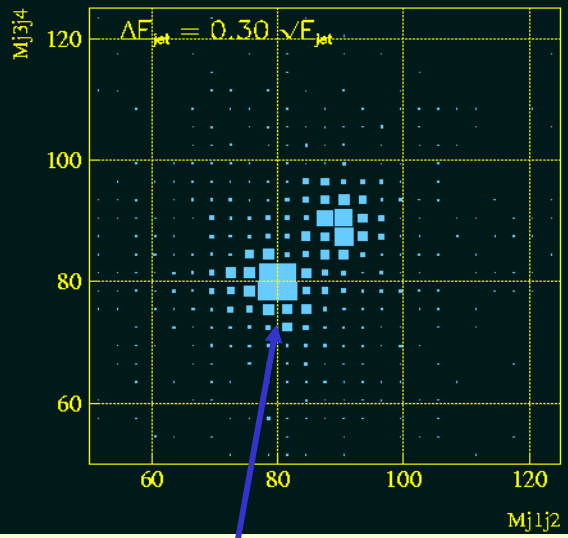


If Higgs is just a fairy tale, then more exotic states must play a role ➔ 'Strong WW Scattering'

Henri Videau; Ecole Polytechnique

Essential final-state discrimination must be done calorimet-rically ➔ 'Energy-flow reconstruction' places demands on calorimeter design





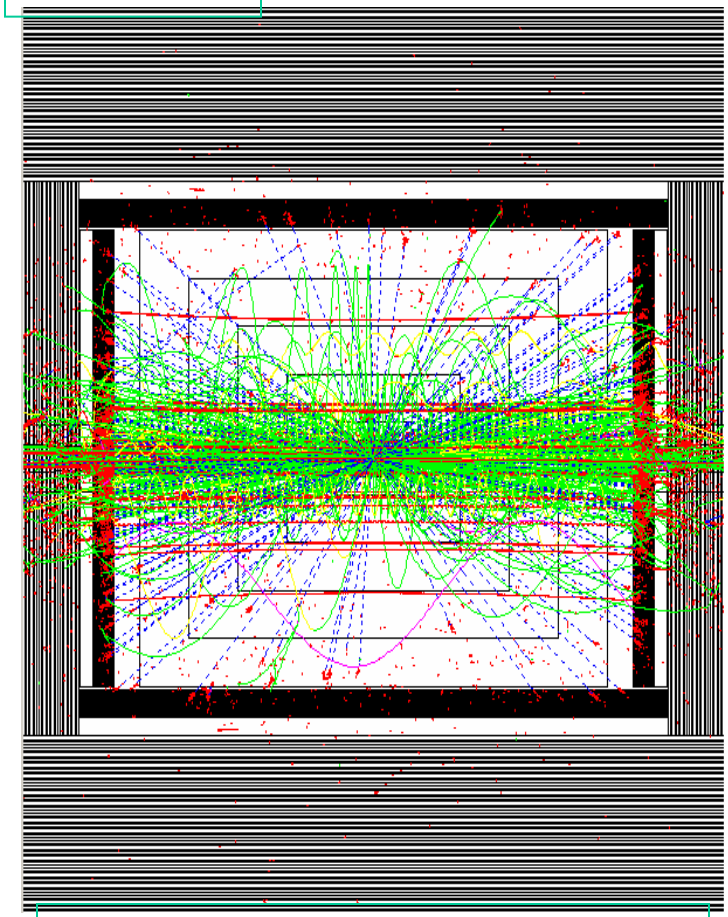
$\Delta E_{jet} = 0.60\sqrt{E_{jet}}$

$\Delta E_{jet} = 0.30\sqrt{E_{jet}}$

Timing is Important

Pileup of $\gamma\gamma \rightarrow$ hadrons for ~200 beam crossings

T. Barklow

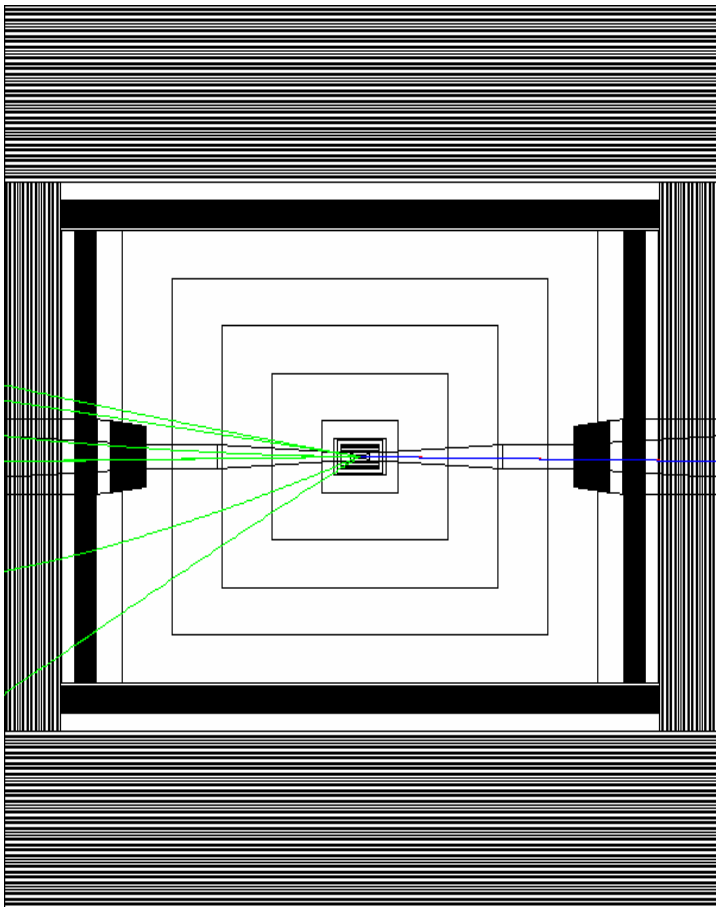


Pileup from 192 crossings
(56 Hadronic Events)

Timing in Cal and Tracking

→

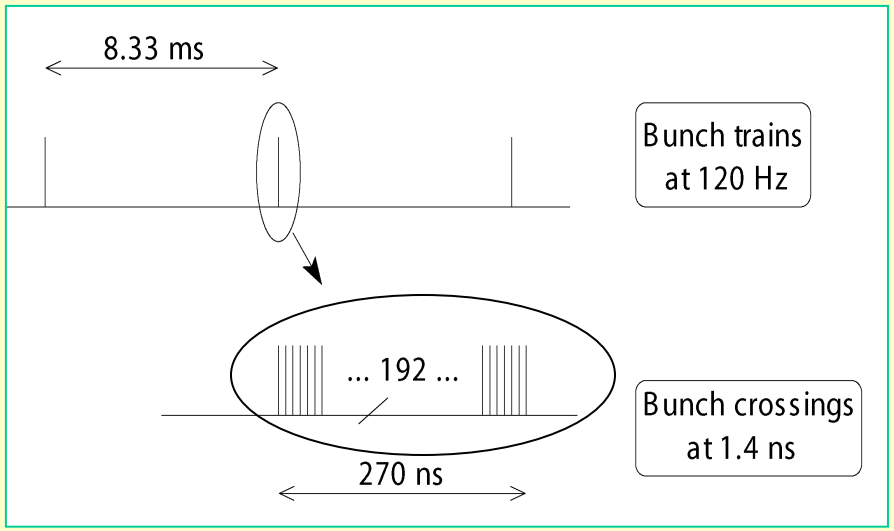
Systems needs to be considered



Pileup from 3 crossings

So… what do we mean by ‘timing’?

The Technology Choice

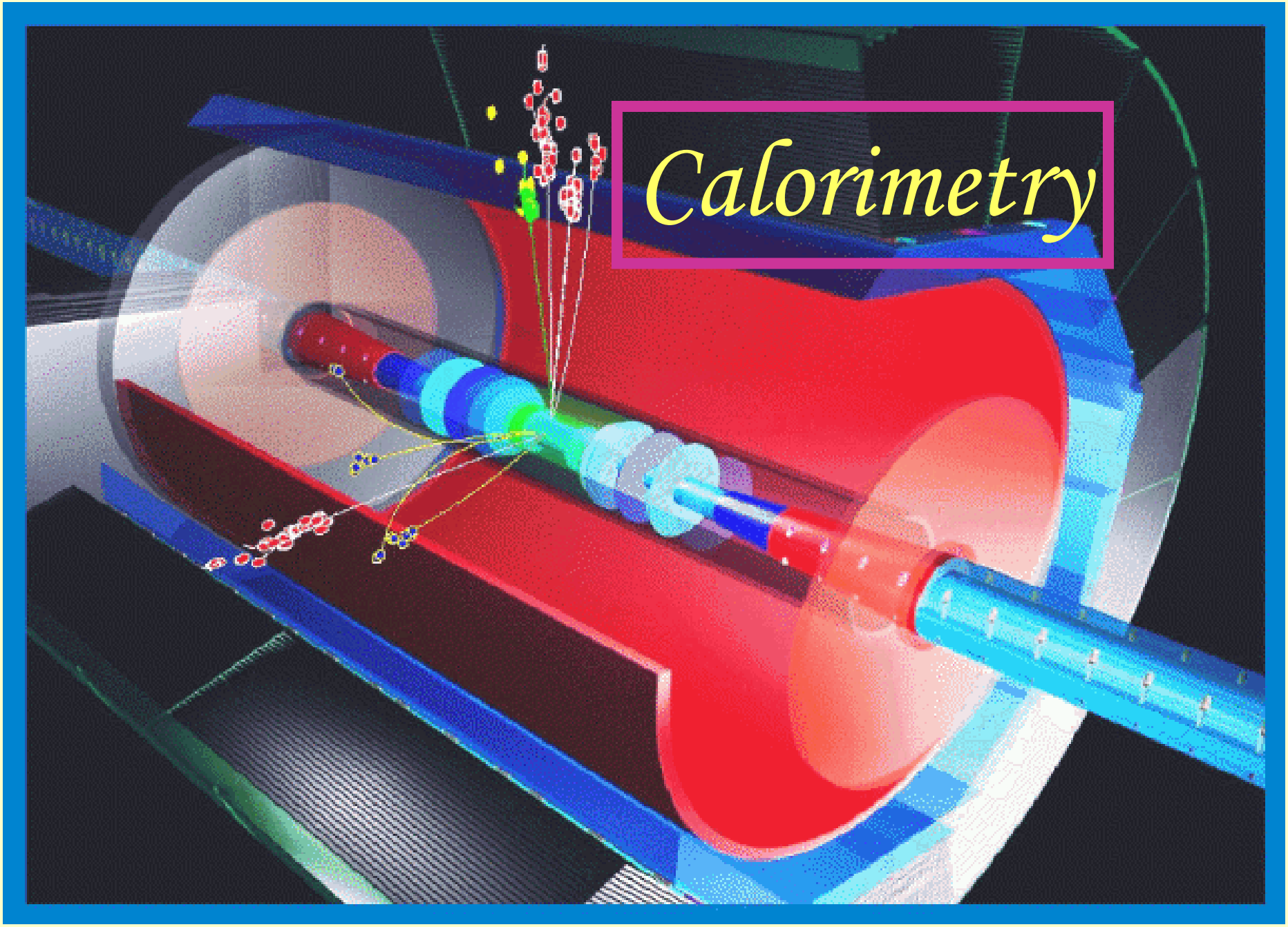


Duty Cycle: 5×10^{-3}

WARM: Short, intense spill (192 pulses separated by 1.4 ns), and often (120 Hz)

COLD: Relaxed but persistent spill (2820 pulses separated by 337 ns); occasional (5 Hz)

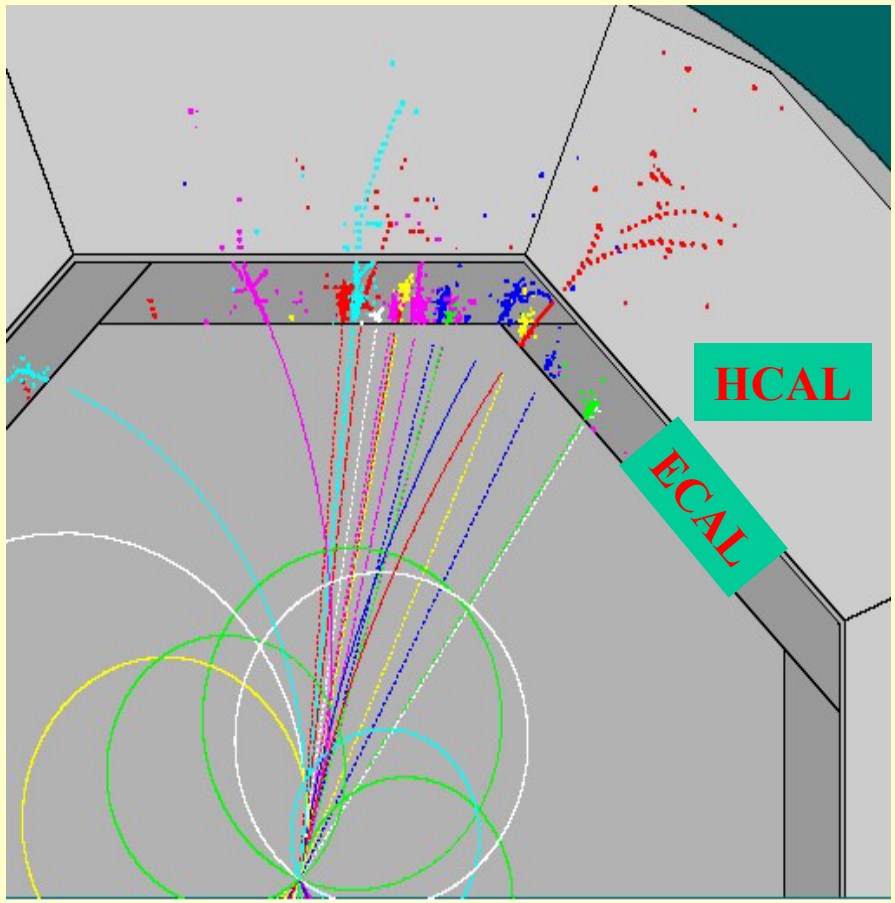
And the choice is… **COLD**


Calorimetry

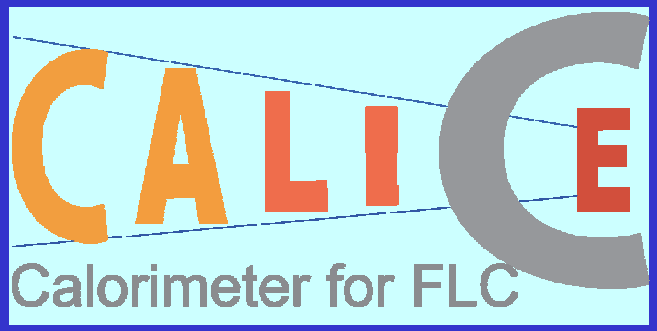
The Energy-Flow Concept

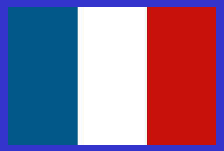
- Photons and high-energy electrons measured best with calorimetry (ECAL)
- Charged hadrons measured best in tracker

➔ Separate clusters in calorimeter and decide what to hand back to tracker



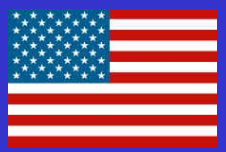
Requires ‘tracking calorimeter’ with minimal shower spread and maximal segmentation (Moliere radius of W is about 1 cm)









CALICE is a consortium of 28 institutions from 8 nations

The SD Si/W Group

M. Breidenbach, D. Freytag, N. Graf, G. Haller, O. Milgrome

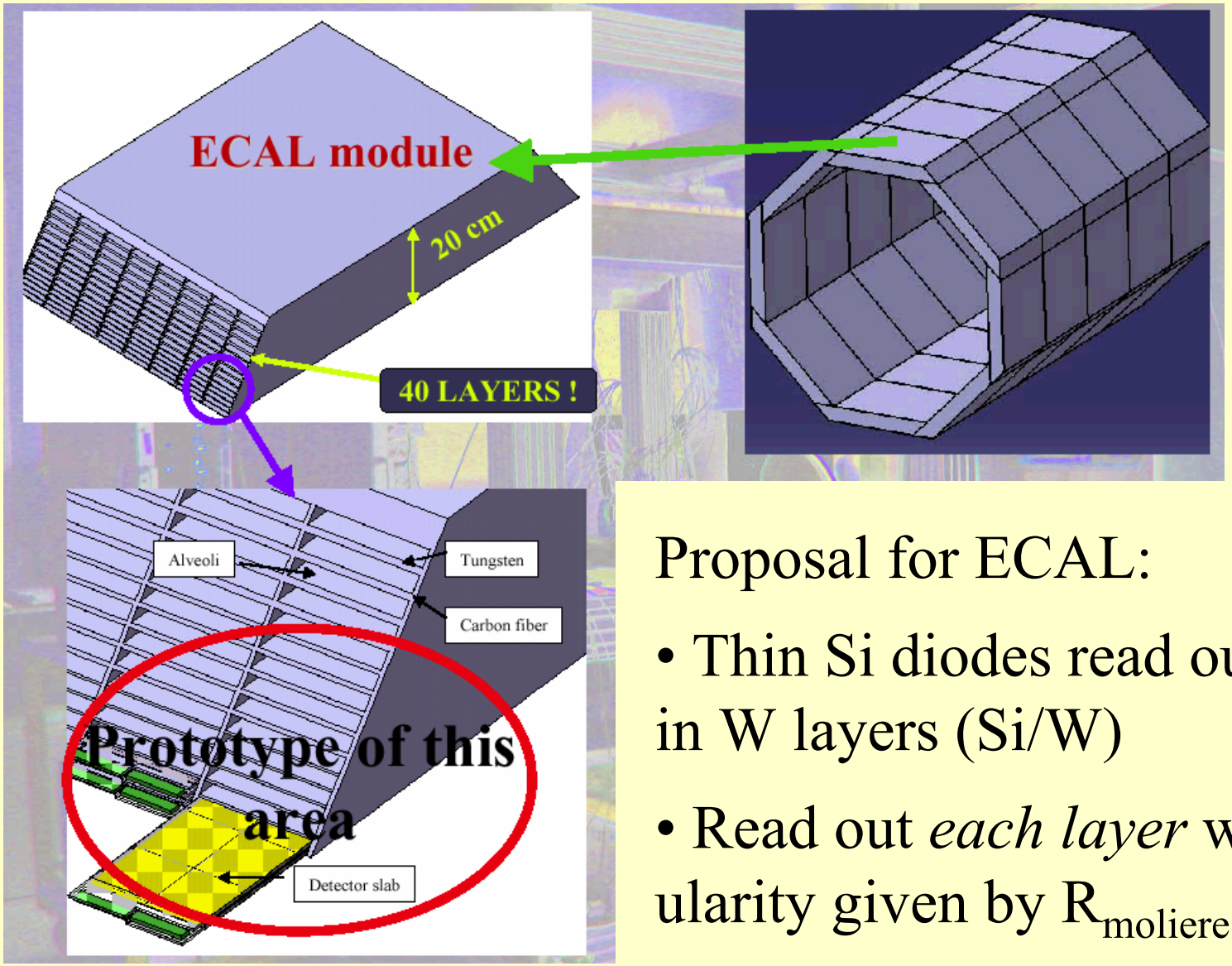
Stanford Linear Accelerator Center

R. Frey, D. Strom

U. Oregon

V. Radeka

Brookhaven National Lab



(TESLA TDR)

Proposal for ECAL:

- Thin Si diodes read out showers in W layers (Si/W)
- Read out *each layer* with granularity given by $R_{moliere}$ (1 cm^2)

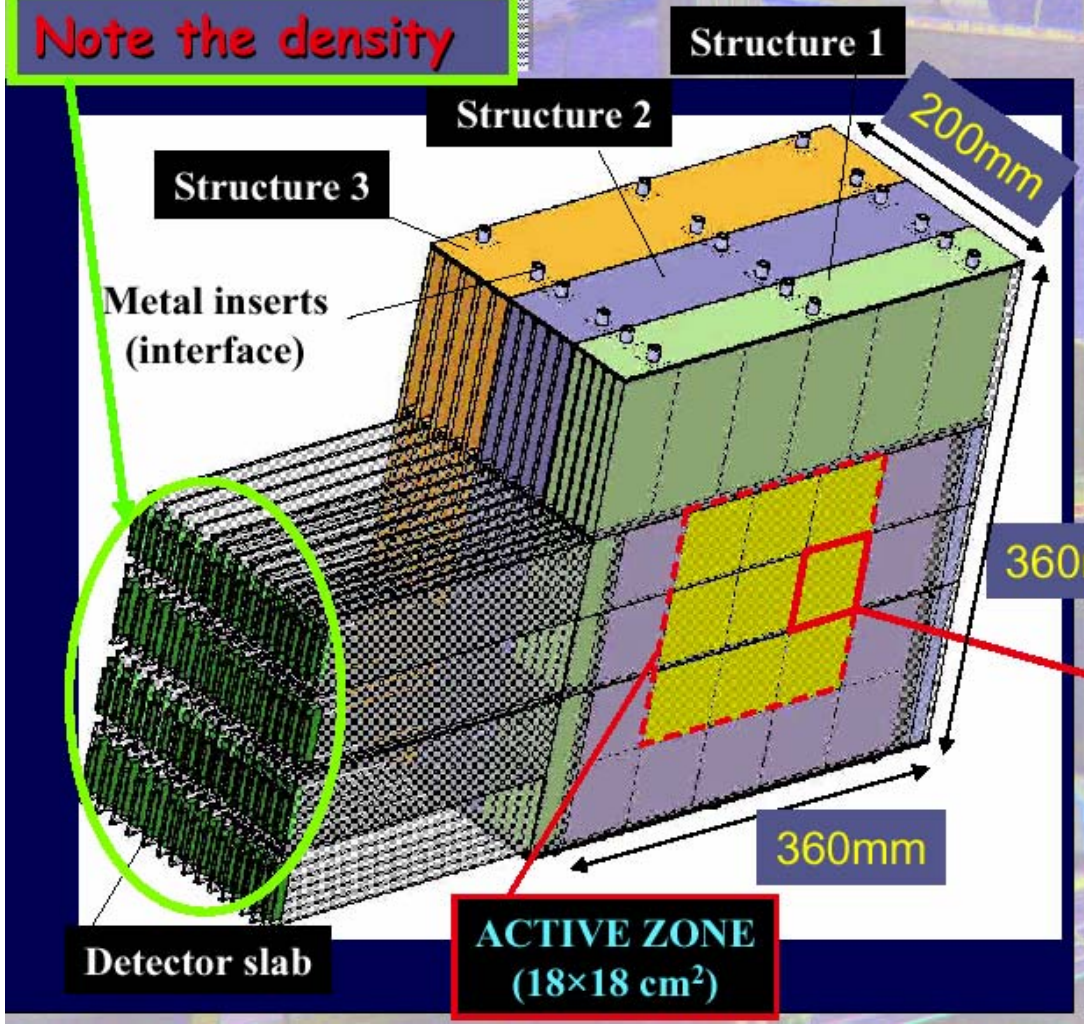
Challenge: This implies a few $\times 10^7$ channels

The ECAL prototype

CALICE ECAL

- LAL,LLR,LPC,PICM
- Imperial College, UCL, Cambridge, Birmingham, Manchester, RAL
- ITEP,IHEP,MSU
- Prague (IOP-ASCR)
- SNU,KNU

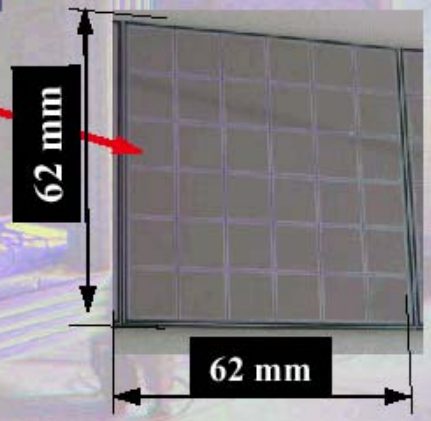
Note the density



- 3 structures W-CFi (1,2,3 x1.4mm)
- 15 « detector slabs »
- Dimension 200x360x360 mm

➔ 9720 channels in prototype

Silicon wafers with 6×6 pads (10×10 mm²)



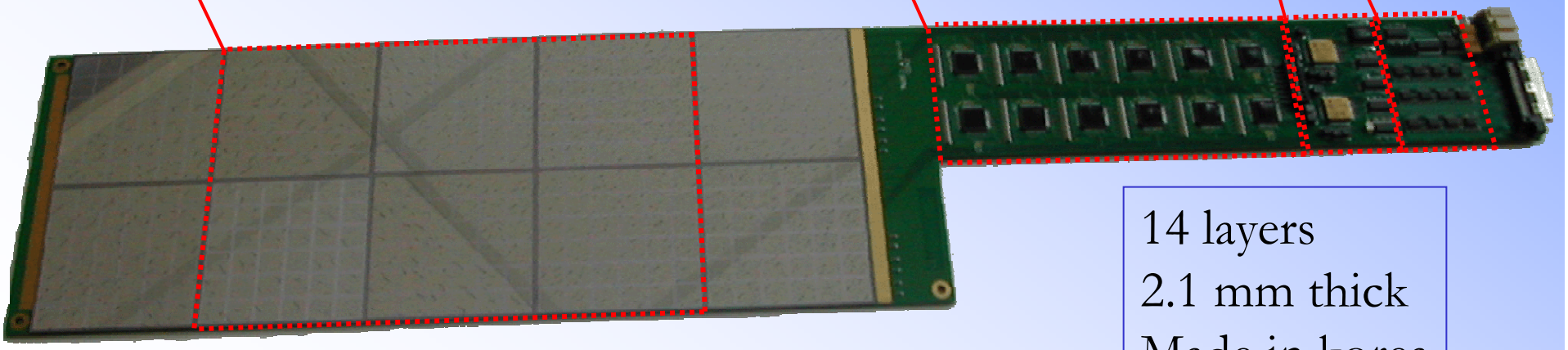
Presentation of the front-end electronic (J. Fleury, LAL Orsay)

6 active wafers
Made of 36 silicon PIN diodes
→ 216 channels per board
Each diode is a 1cm² square

2 calibration switches chips
6 calibration channels per chip
18 diodes per calibration channel

12 FLC_PHY3 front-end chip
18 channels per chip
13 bit dynamic range

Line buffers
To DAQ part
Differential



14 layers
2.1 mm thick
Made in korea

FLC_PHY3 overview (J. Fleury, LAL Orsay)

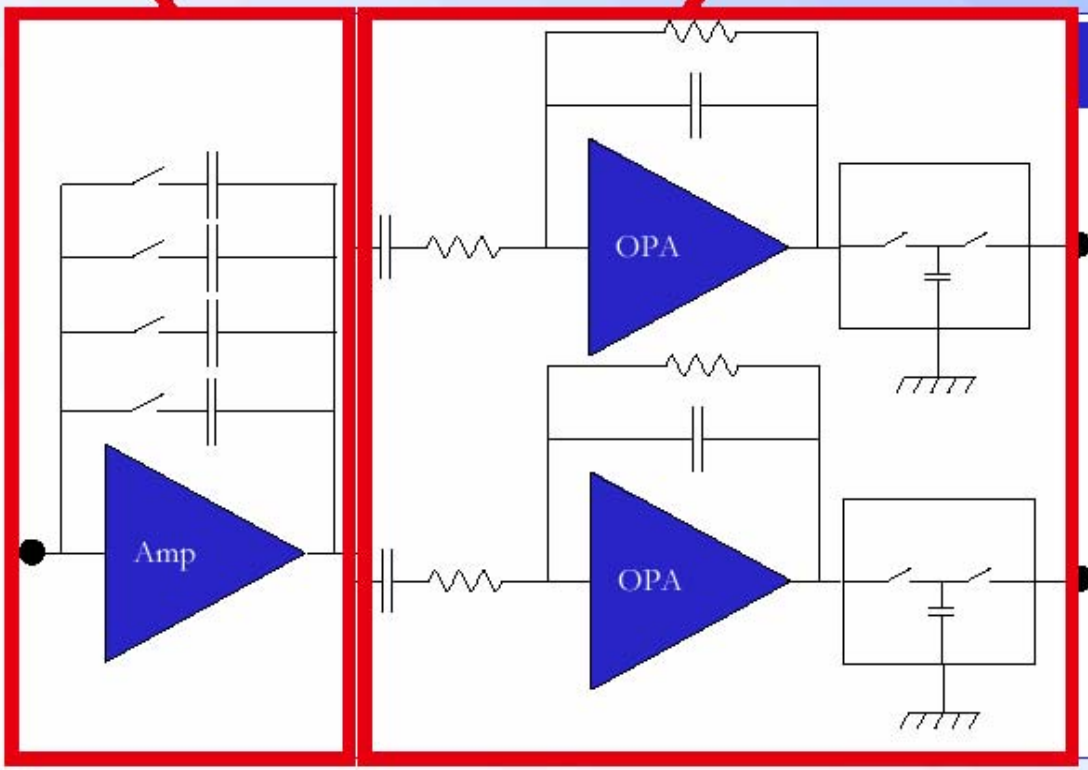
Multi-gain charge preamp

- 4 bits for gain selection
- Gain from 0.3 to 5 V/pC
- Gain selected offline

Dual shaper & track and hold

- Gain 1 and gain 10
- Work in parallel to select gain *a posteriori*

Process: 0.8 µm BiCMOS



1 channel

MUX out Gain=10

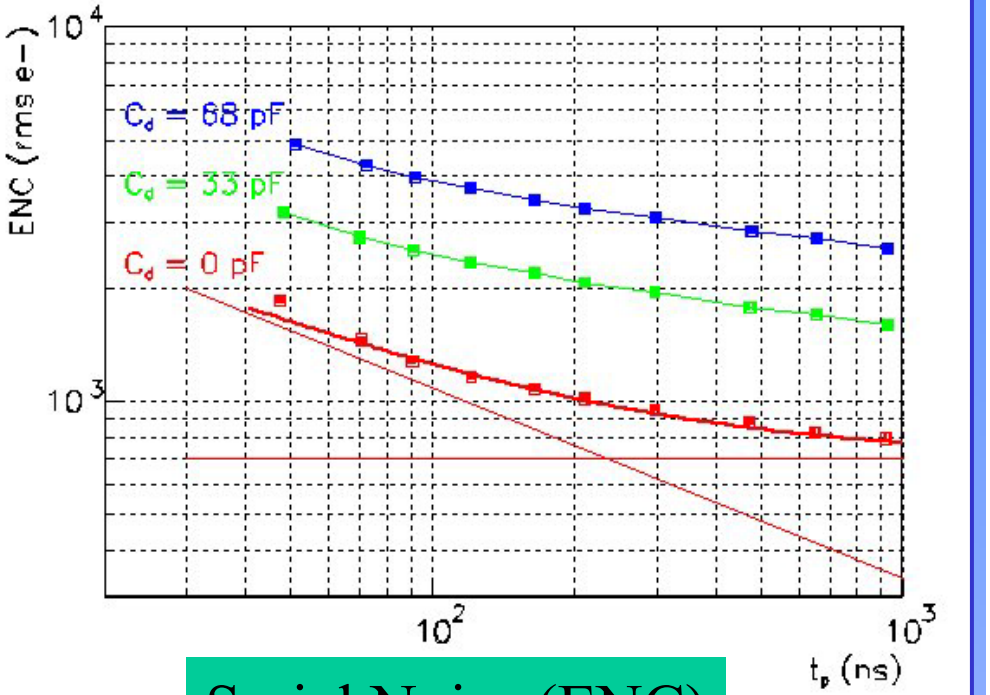
MUX out Gain=1

Global characteristcs

- 18 channel input
- 1 mux output

FLC-PHY3 Chip (LAL Orsay)

Based on blocks from OPERA HPD readout ASIC



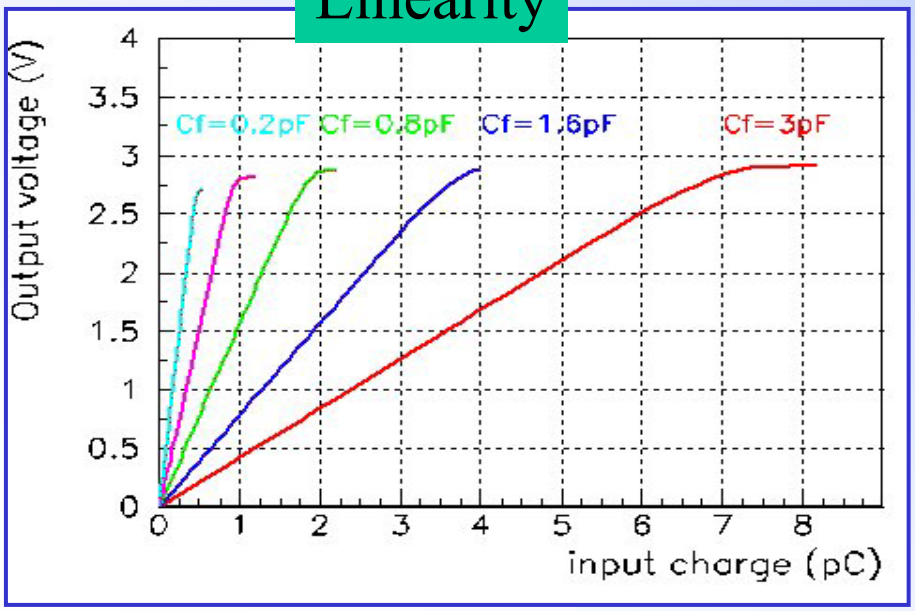
Serial Noise (ENC)

At τ~200 nsec, C_{det} in pF:

ENC = 1720 + 28*C_{det} (x1 gain)

ENC = 950 + 34*C_{det} (x10 gain)

Linearity



Now available for instru-mentation of CALICE ECAL prototype (~2000 packages)

Threads in ongoing ECAL front-end electronics Research and Development

For precision calorimetry, compactness is important

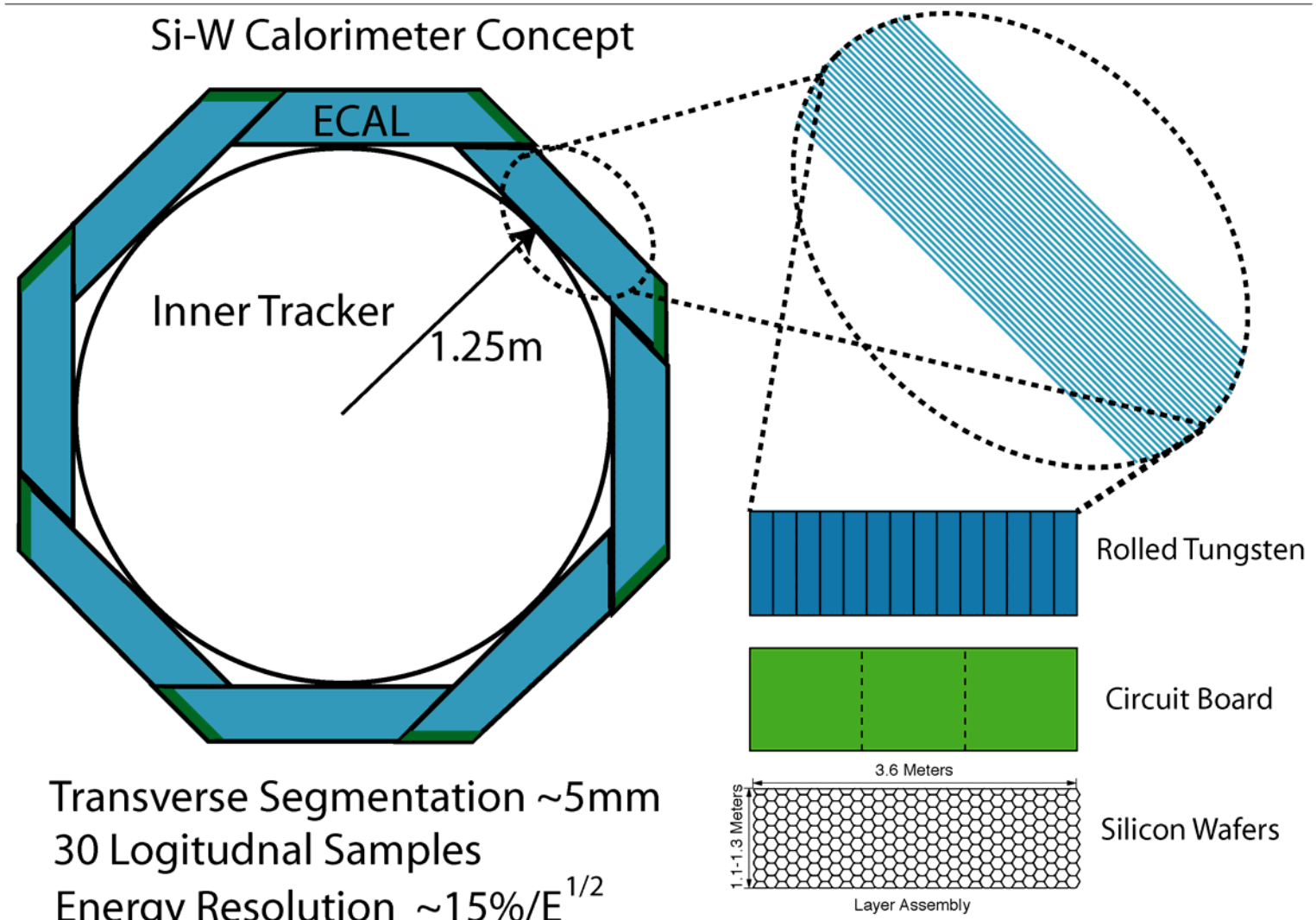
- Maintain Moliere redius
- Calorimetry inside coil
- Handle staggering channel count

➔Multi-channel electronics integrated into detector volume

➔Power cycling to avoid active cooling

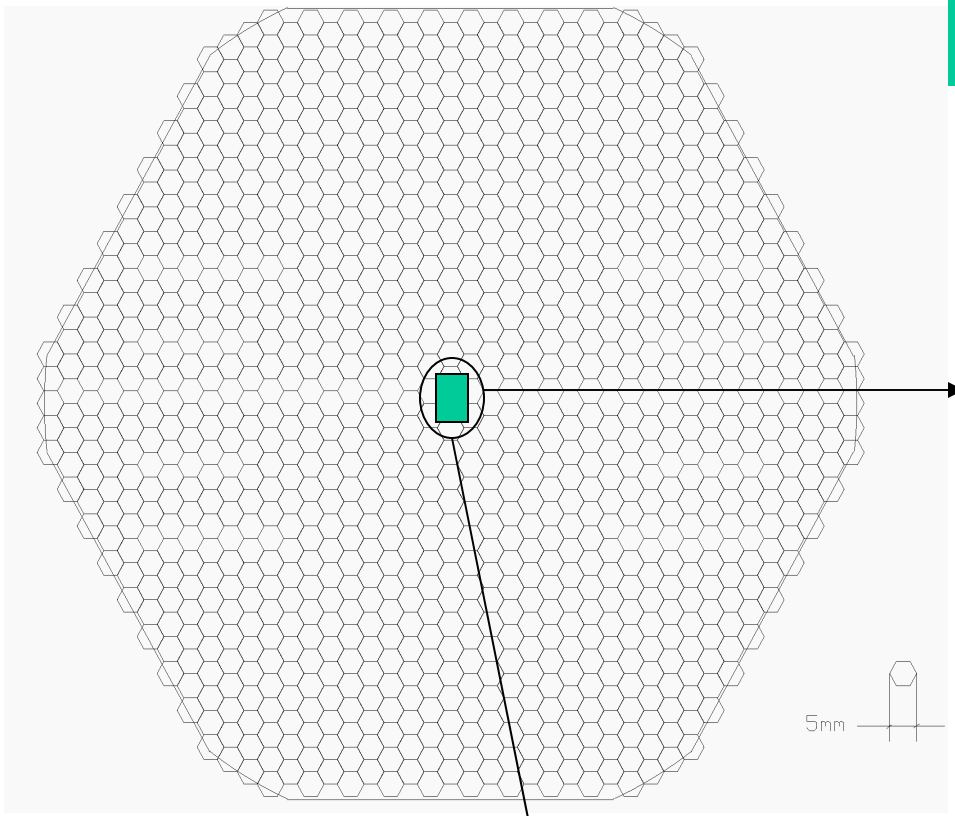
➔Zero-suppression, timing to avoid pile-up

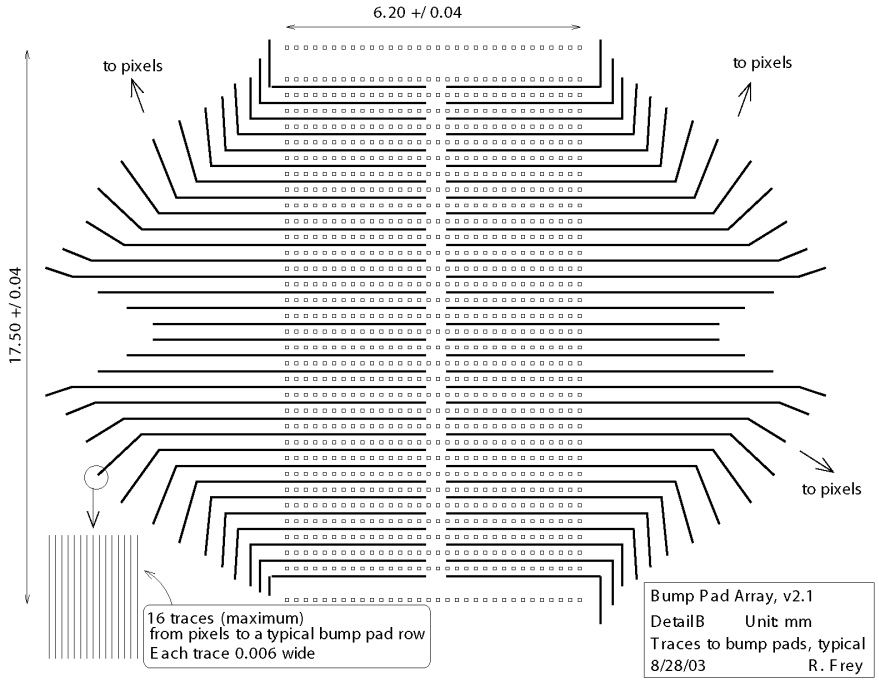
SD Si/W Ecal Concept (R. Frey, SD Si/W group)

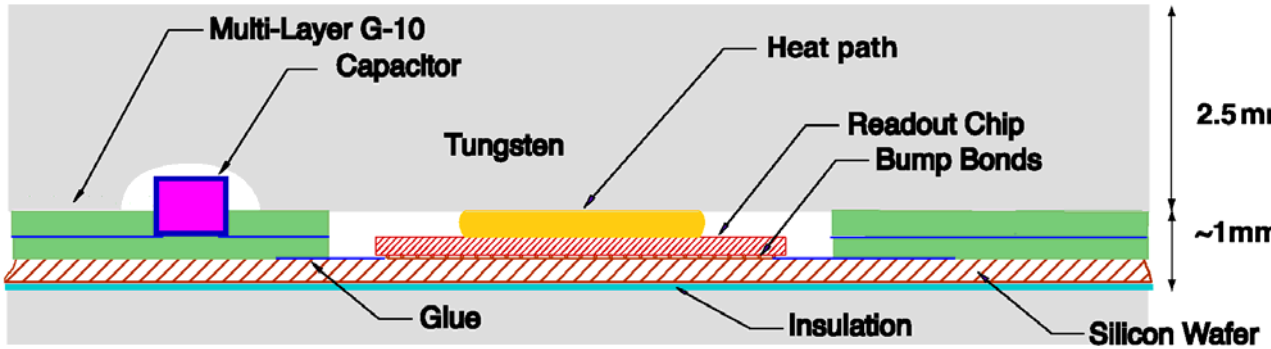


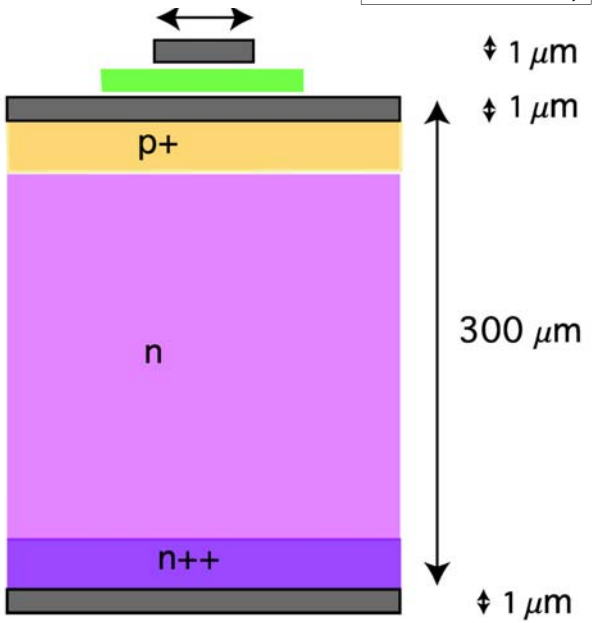
Transverse Segmentation ~5mm
30 Logitudnal Samples
Energy Resolution ~15%/$E^{1/2}$

Wafer and readout chip





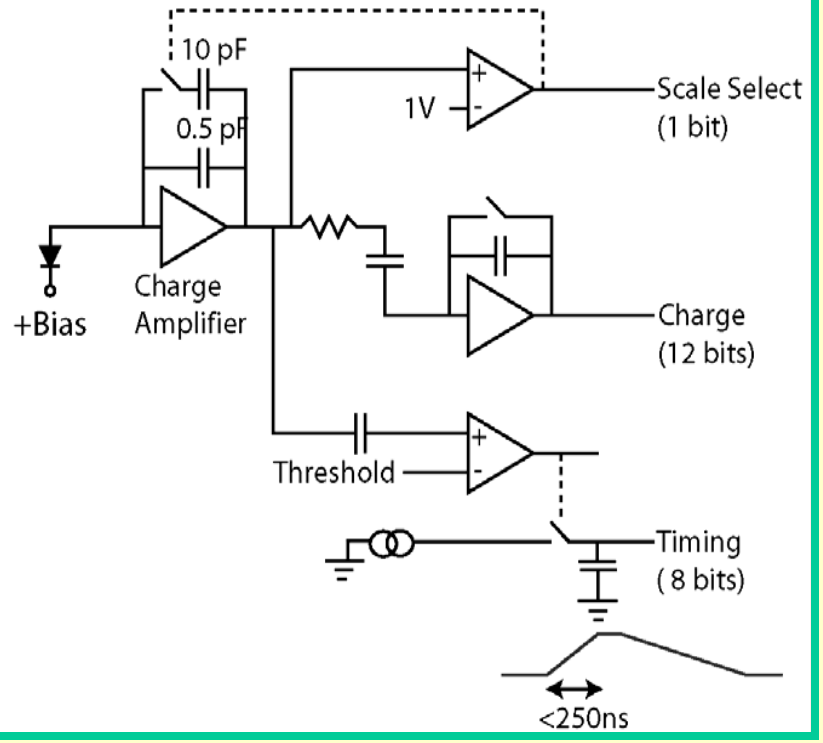




(R. Frey, SD Si/W group)

SD Si/W ASIC

- Capacitance
  - Pixels: 5.7 pF
  - Traces and pre-amp: 22 pF
- Resistance
  - 300 ohm max
- Power
  - < 40 mW/wafer ⇒ power cycling
    (An important LC feature!)
- Signal Processing
  - Provide fully digitized, zero suppressed outputs of Q and T
  - One ASIC per wafer
- Signals
  - <2000 e noise
  - Require MIPs with S/N > 7
  - Max. signal 2500 MIPs (5mm pixels)



Dynamically switched C_f

- Signals after 1st stage larger
  - ~0.1 mV → 6.4mV for MIP
- Much reduced power
  - Large currents in 1st stage only

CALICE will pursue similar development

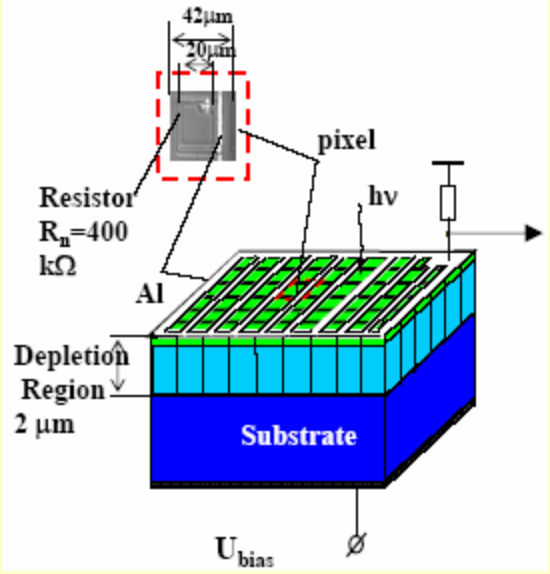
Hadronic Calorimeter (HCAL)

Need to maintain longitudinal and transverse segmentation:

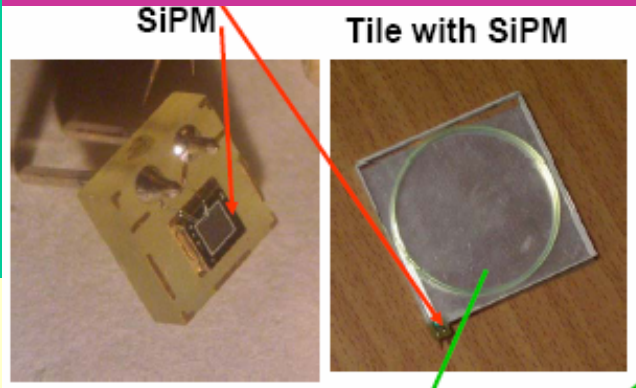
- 5x5 cm^2 ➔ 'Analog HCAL'
- 3x3 cm^2 ➔ 'Semi-digital HCAL'
- 1x1 cm^2 ➔ 'Digital HCAL'

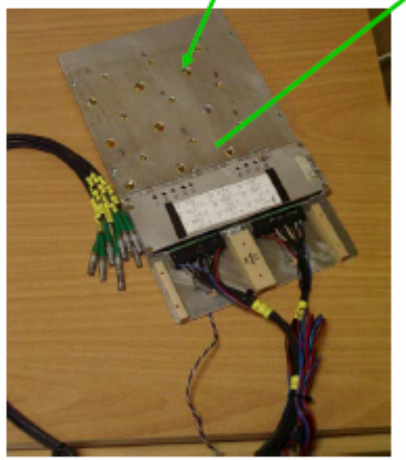
Silicon Photomul-tiplier (SiPM)

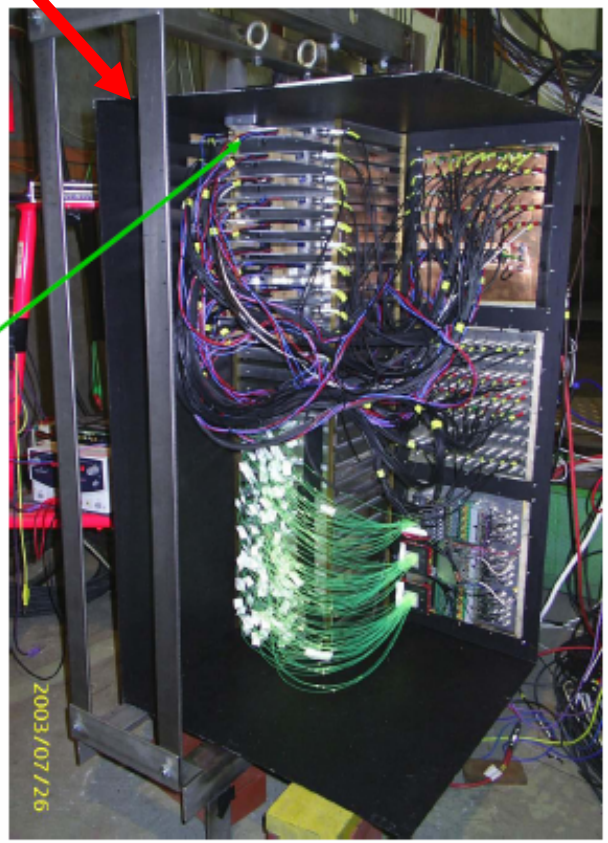
Ganged Geiger-mode pixels



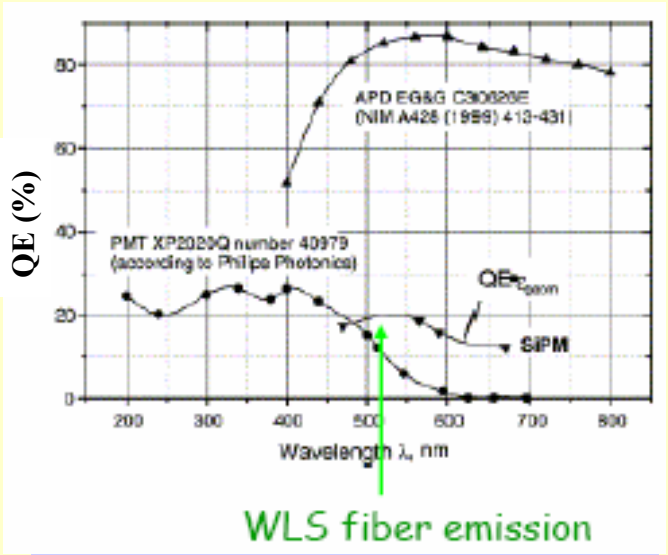
Moscow Engineering and Physics Institute







SiPM Electronics Development



Quantum Efficiency similar to PMT, but single-stage gain, so better statistically than PMT or APD (single-PE statistics)

SiPM signals:

gain 10^6:	1 photo electron = 160 fC
MIPs	~ 25 p.e. = 4 pC
dyn range:	Max signal = 400 pC
fast:	few ns rise time

pulse shape set by wavelength shifter fiber

SiPM noise:

2MHz noise rate (signal every 500ns)
dominated by 1 pixel signals
necessary calibration signal
But could pile up with slow shaping

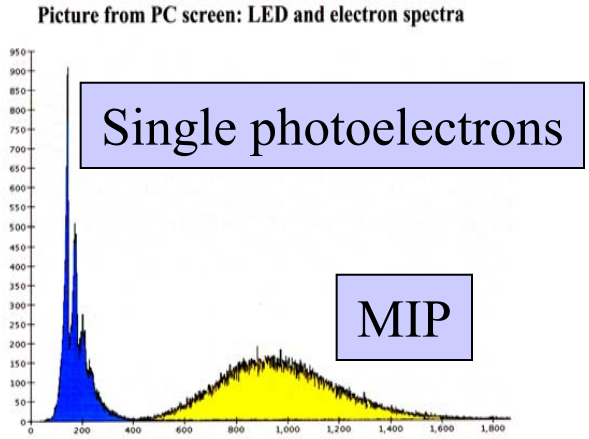
SiPM calibration

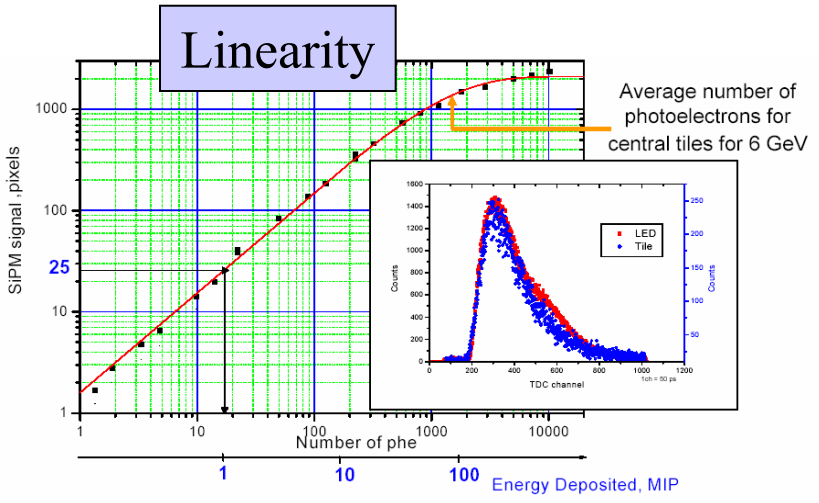
Felix Sefkow, DESY

- The **MIP** signal determines the **energy scale**
  - monitor overall response
    - scint, SiPM, FEE
- **LED**: inject UV into scintillator:
  - **Single photon peak spacing** *a must!*
    - **non-linearity correction (**together with MIP and universal response function)
    - **gain monitoring:**

      SiPM temperature sensitivity:

      Gain: 3%/K, Signal: 4%/K
  - **Medium** LED signals: **stability** between MIP calibration runs
  - **Large** LED signals: direct **non-linearity** monitoring
- Charge injection: electronics calibration





Two Shaping-Time/Two Gain Solution

Calibration mode (short shaping)

Single photoelectron response

Cf=0.2pF ; τ =12ns

1 spe = 8.9 mV ; tp=40 ns

Noise : 720 µV rms

Physics mode (longer shaping)

MIP (=16pe) response

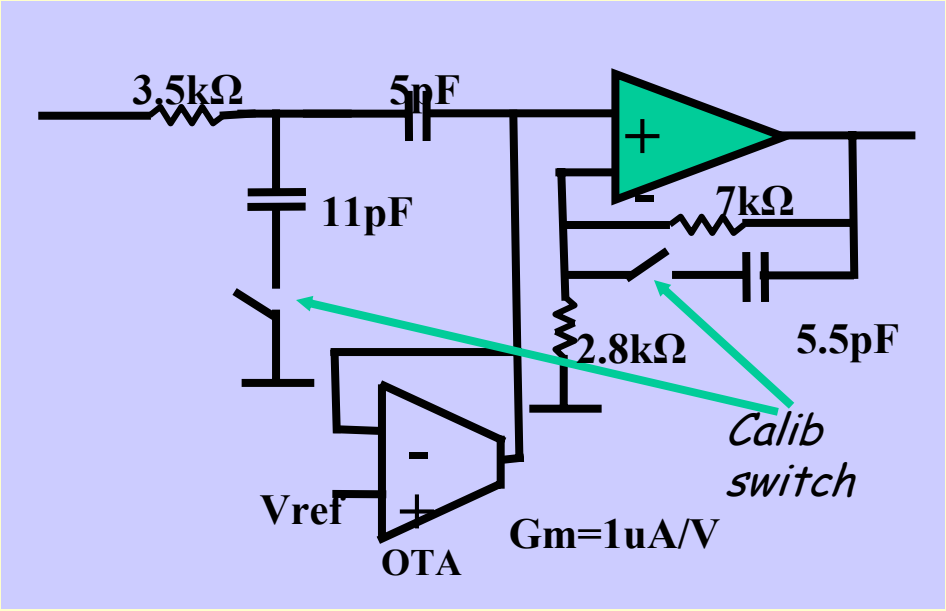
Cf=0.4pF ; Rc=5k ; τ =120ns

Gain = 12 mV/MIP ; tp=186ns

Noise = 570 µV rms

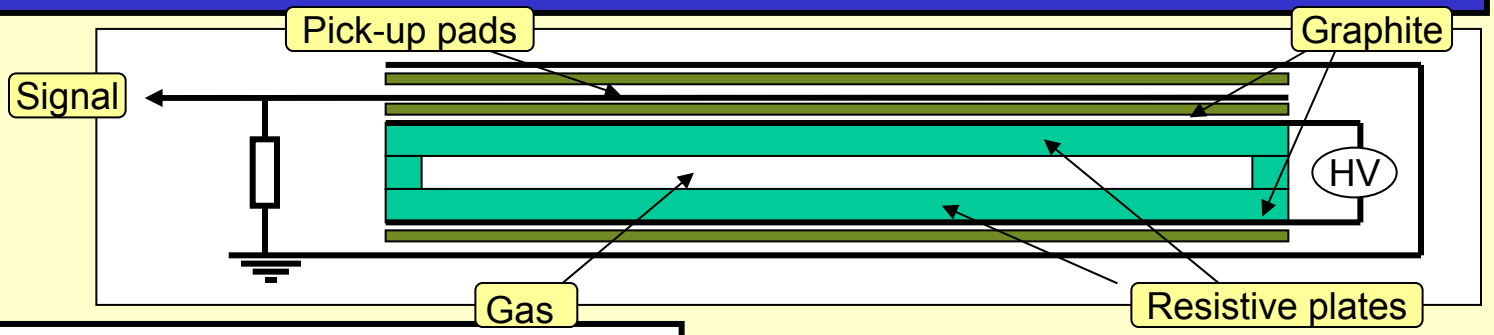
Unipolar/Two Gain Solution

(avoid overshoot that can lead to single PE pile-up)



Both on same prototype ASIC; to be submitted

ASIC for 'Digital HCAL' – 1 cm^2 RPC's



American Linear Collider Physics Group

Conceptual Design of the Amplifier/Discriminator/Timestamp (ADT) ASIC

Gary Drake, José Repond, Dave Underwood, Lei Xia
Argonne National Laboratory

Charlie Nelson
Fermilab

Version 1.20
February 23, 2004

- 64 inputs with choice of input gains
- RPCs (streamer and avalanche), GEMs…
- Triggerless or triggered operation
- Output: hit pattern and time stamp

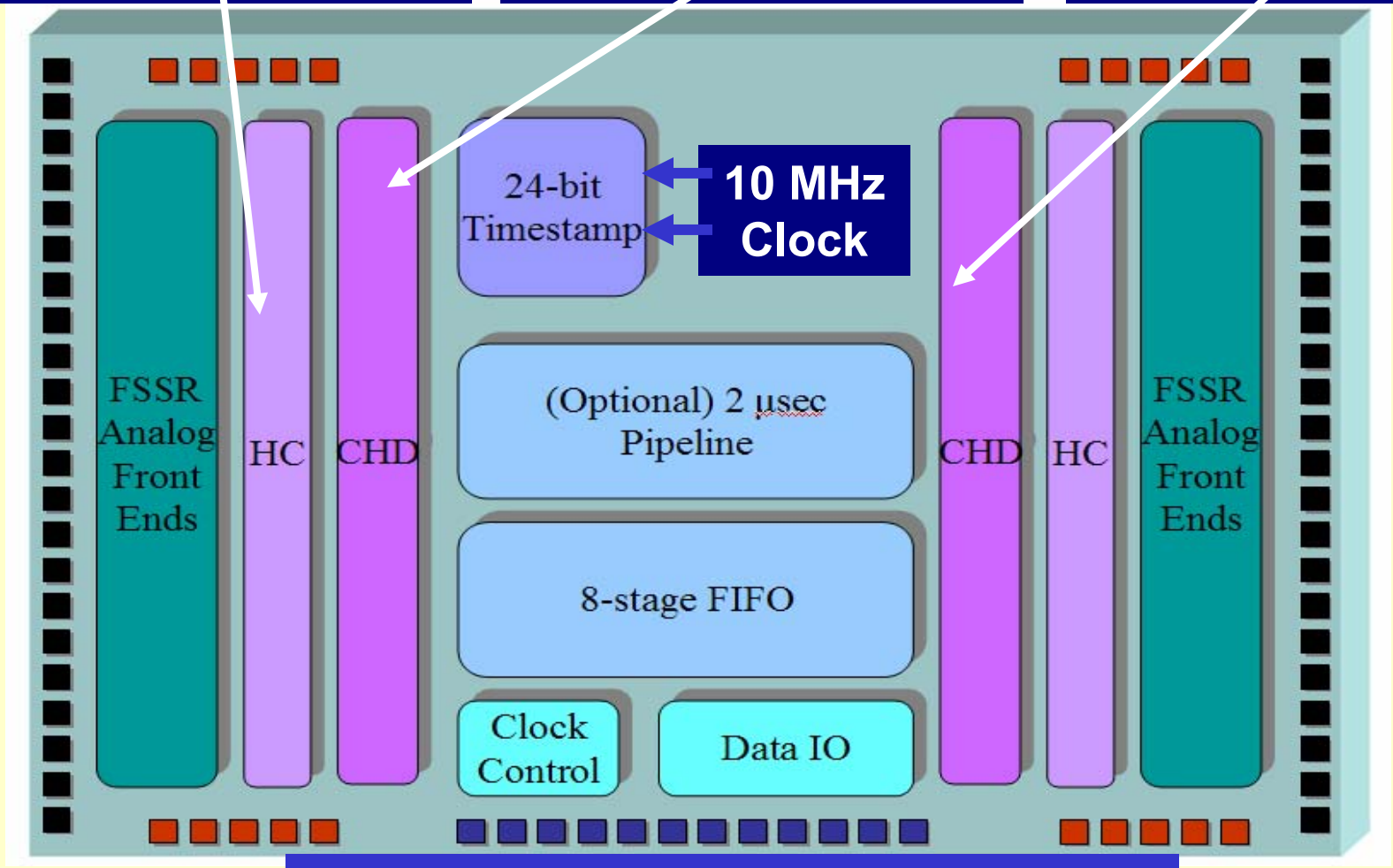
J. Repond, Argonne

Digital HCAL ASIC

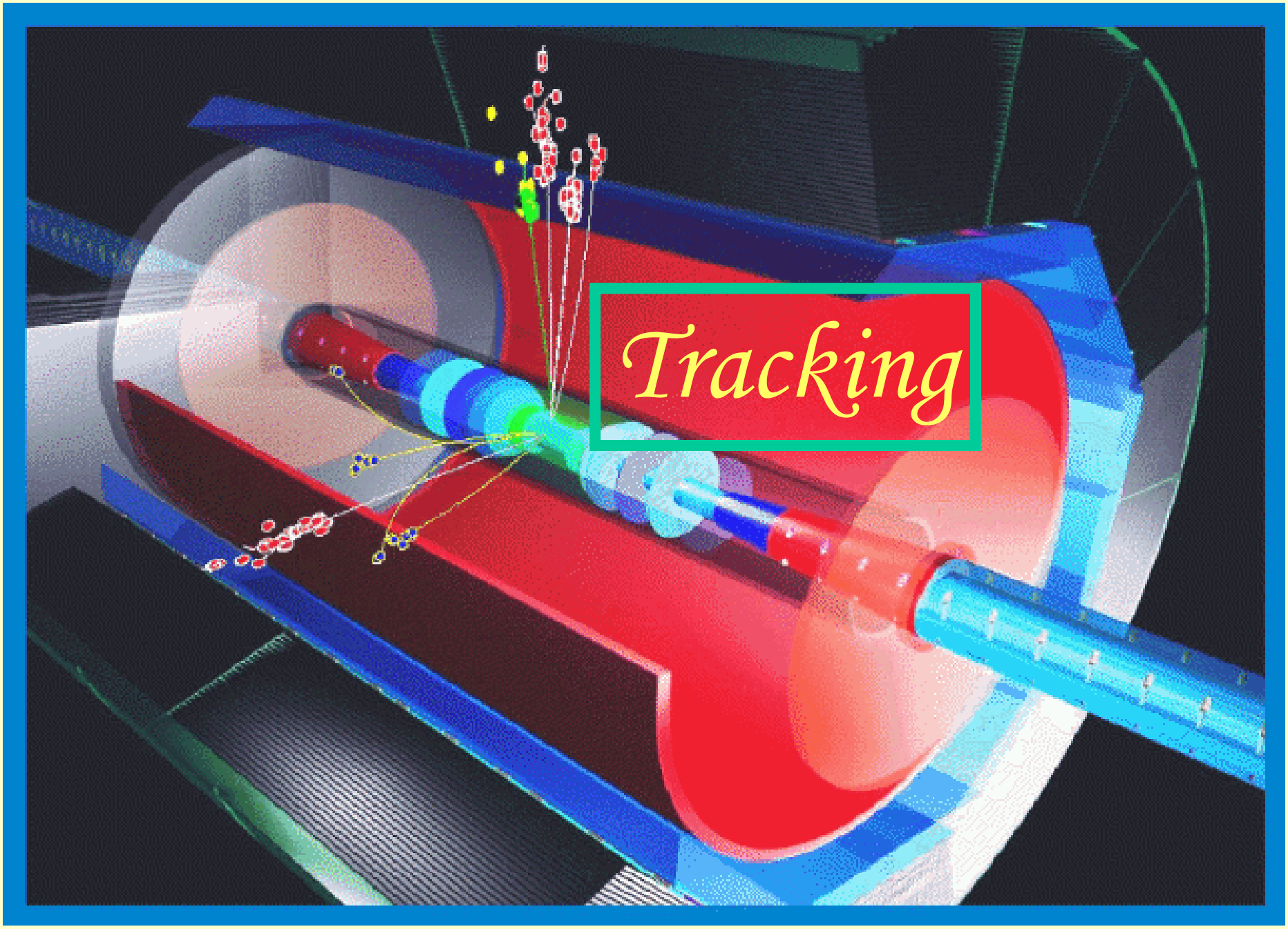
Analog circuitry taken from recently built FSSR chip (BTeV)

Hit catcher with possibility to mask noisy channels

Chip has data indicator (essentially a fast OR)

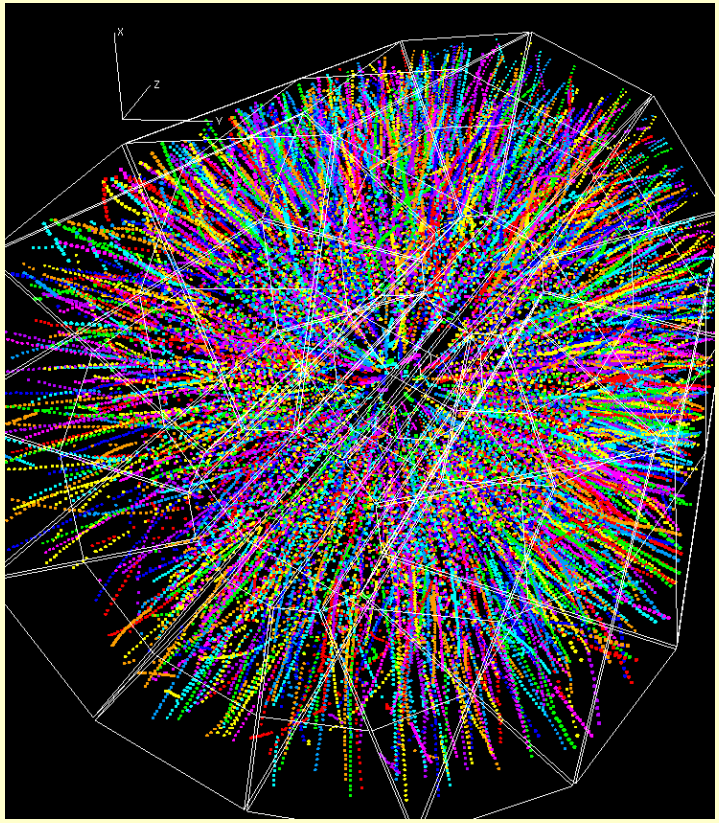


Hope to submit by end of 2004


Tracking

Gaseous Tracking in the Third Millennium

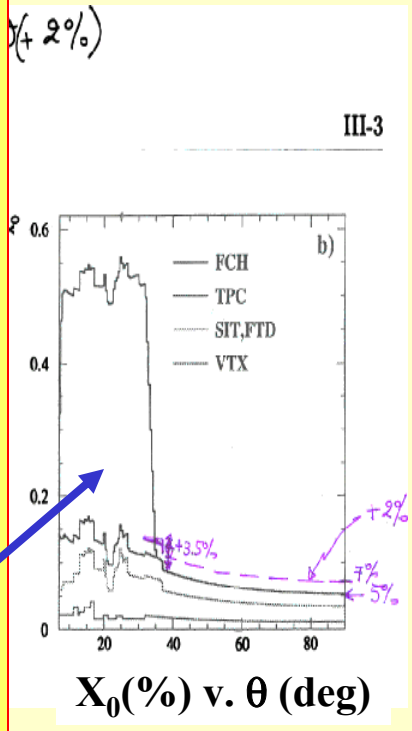
A TPC event from STAR at RHIC



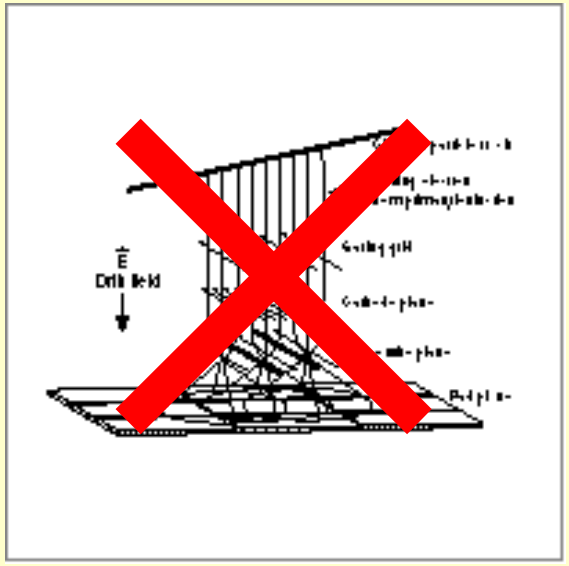
Tracking in heavy ion collisions is messy, but TPC's are highly pixellated

For the Linear Collider Detector:

- Track *densities* are actually higher
- Baseline performance implies x3 improvement in point resolution
- Must avoid excessive material in endcaps (energy flow into forward calorimetry

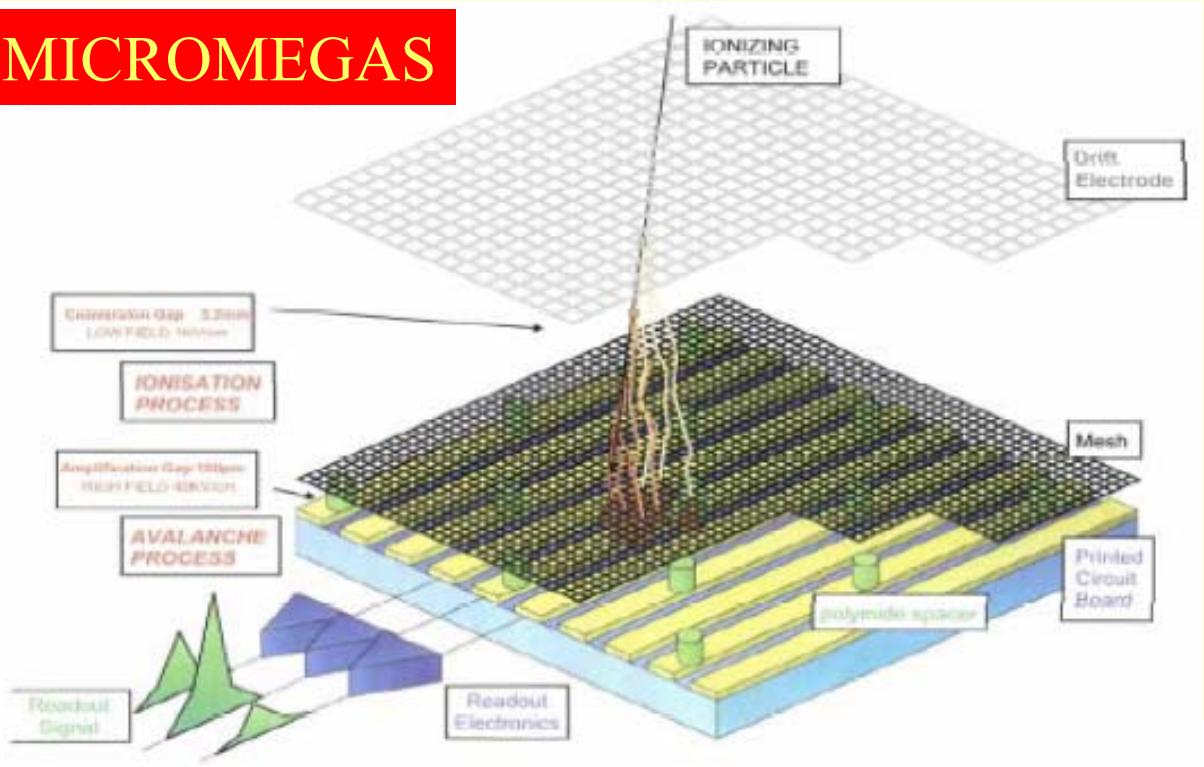


X_0(%) v. θ (deg)



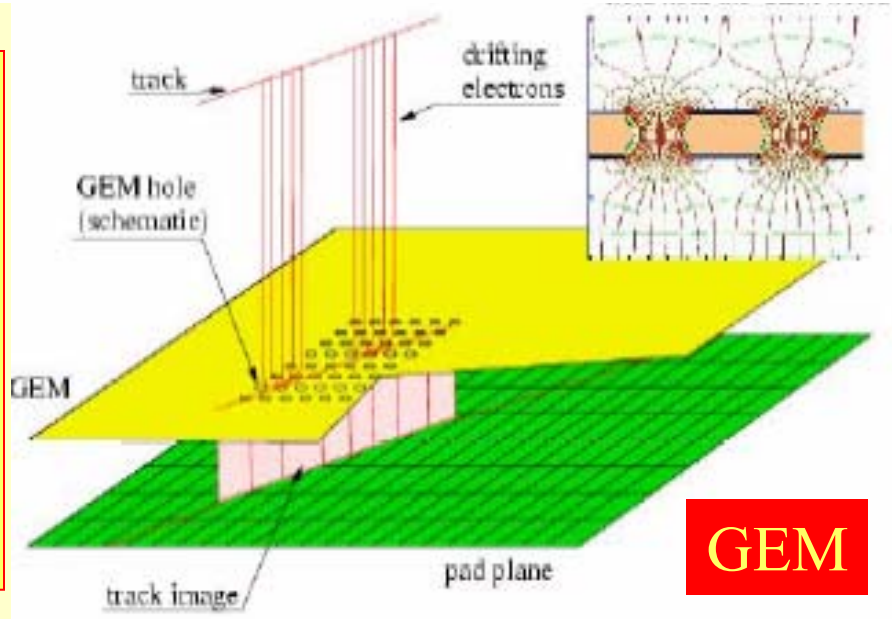
Traditional wire-plane readout too course

MICROMEGAS



Micro-Patterned Gas Detectors

- Finer segmentation ➔ better resolution
- Ion feedback into tracking volume is small if gain is kept low (~10^2 per layer)



GEM

TPC Electronics Issues

Low Noise: want to keep gain low to avoid excessive feedback of ions into the drift volume

Channel Count: 2mm^2 pads (to achieve 100 μm resolution) implies > 10^6 channels; if limited (350 μm) transverse diffusion is exploited, would reach 10^8

Flash ADC: Exploiting longitudinal diffusion (z drift) resolution limit implies ~100 MHz sampling

Signal Processing: Zero suppression, buffering, waveform processing, power cycling, etc. to keep electronics compact and material down

Begin upgrade of STAR/ALICE FEL or…

Readout of a TPC using the Medipix2 CMOS pixel sensor

(detection of single electrons on a direct pixel segmented anode)

NIKHEF: Alessandro Fornaini
Harry van der Graaf
Jan Timmermans
Jan Visschers
Peter Kluit

Saclay (CEA/DAPNIA): Paul Colas
Ioannis Giomataris
Arnaud Giganon

Univ. Twente/Mesa+: Jurriaan Schmitz

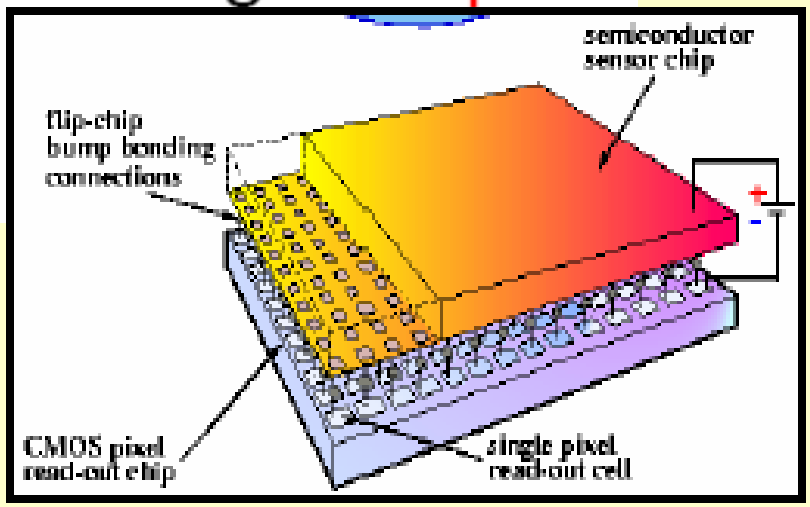
CERN/Medipix Collaboration: Erik Heijne

Thanks to: Wim Gotink
Joop Rovenkamp
Max Chefdeville

Goals

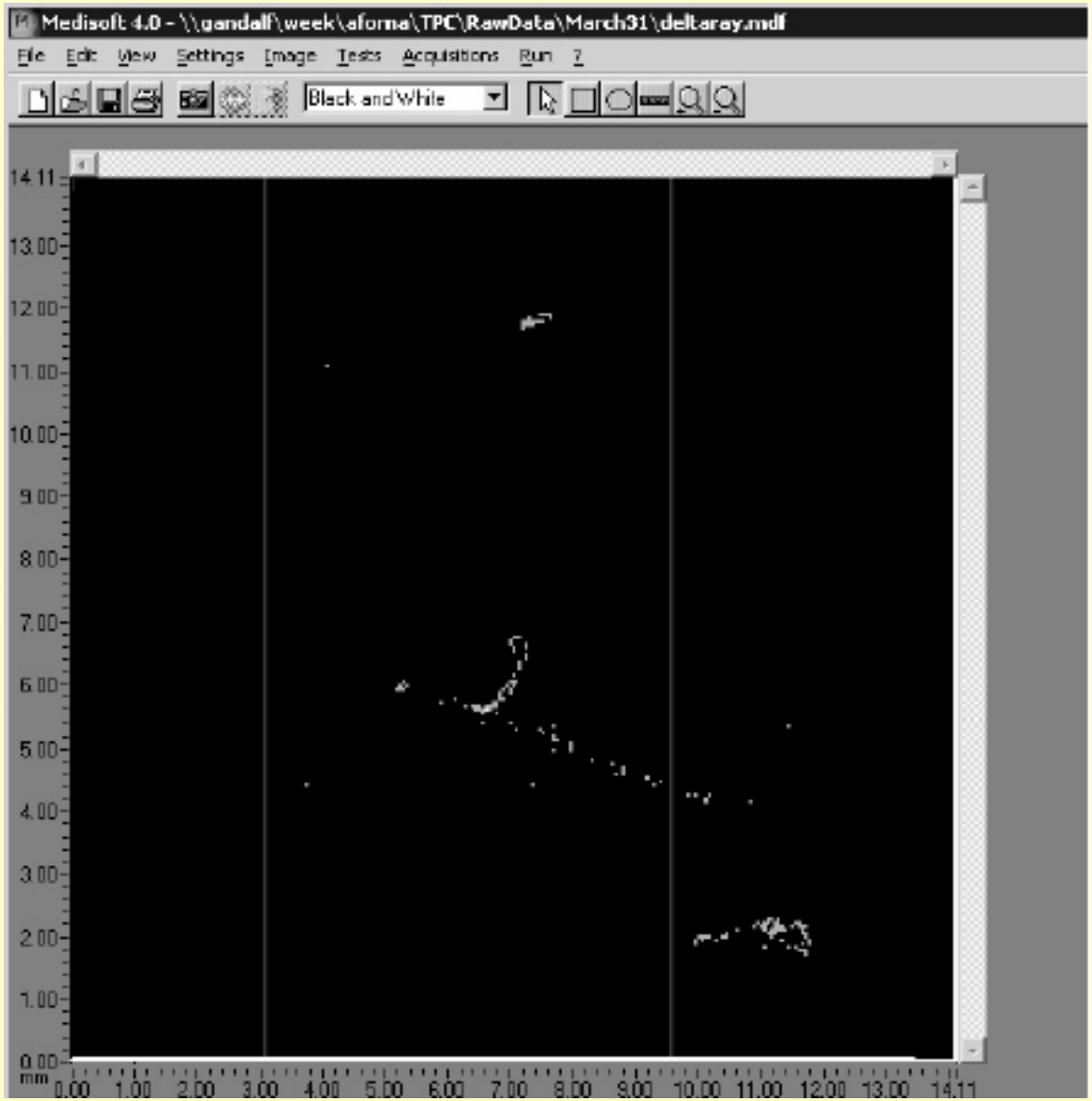
- Gas multiplication GEM or Micromegas foil(s)
- Charge collection with granularity matching primary ionisation cluster spread
- Needs sufficiently low diffusion gas
- dE/dx using cluster counting?
  ($\rightarrow$ M. Hauschild)

- Proof of principle based on existing Medipix2 readout chip



Jan Timmermans, Nikhef

Jan Timmermans, Nikhef



Readout microMegas detector with 55x55 μm^2 pixel MediPix chip

Clear depiction of ionization path, δ-ray

Optimal for pattern recognition, two-track separation, dE/dX

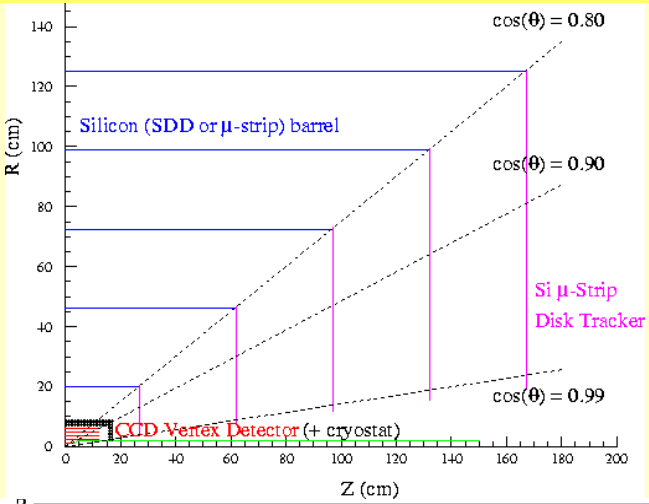
But: Approaches $\mathbf{10^{10}}$ channels!!

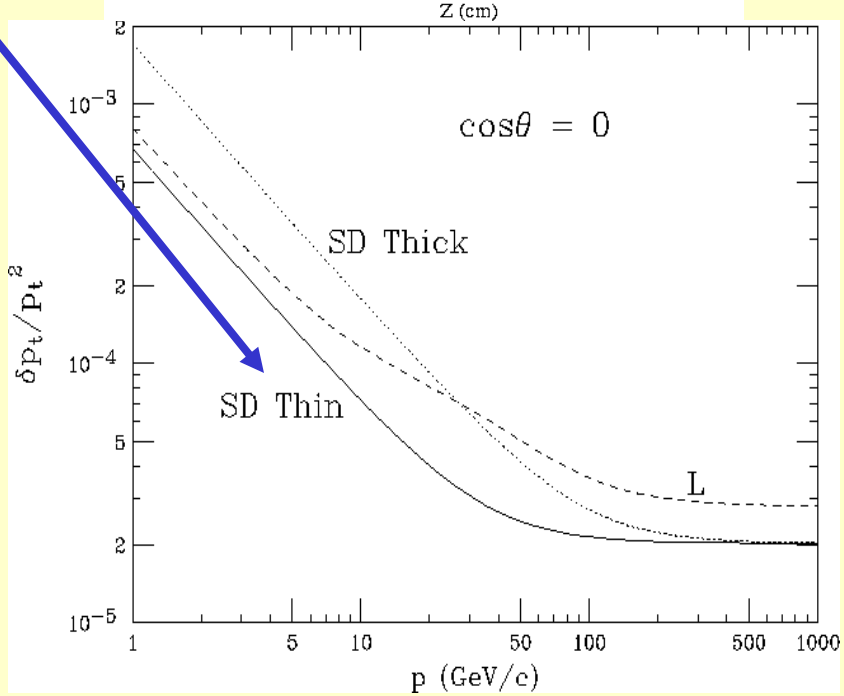
Solid-State Tracking: the 'Gossamer Tracker' Concept

What if the *only* material in the tracker was the minimum necessary thickness of Si?

- No support structure
- No cooling
- No electronics and servicing
- Thinner detectors towards lower radius

No – pigs can't fly. But…

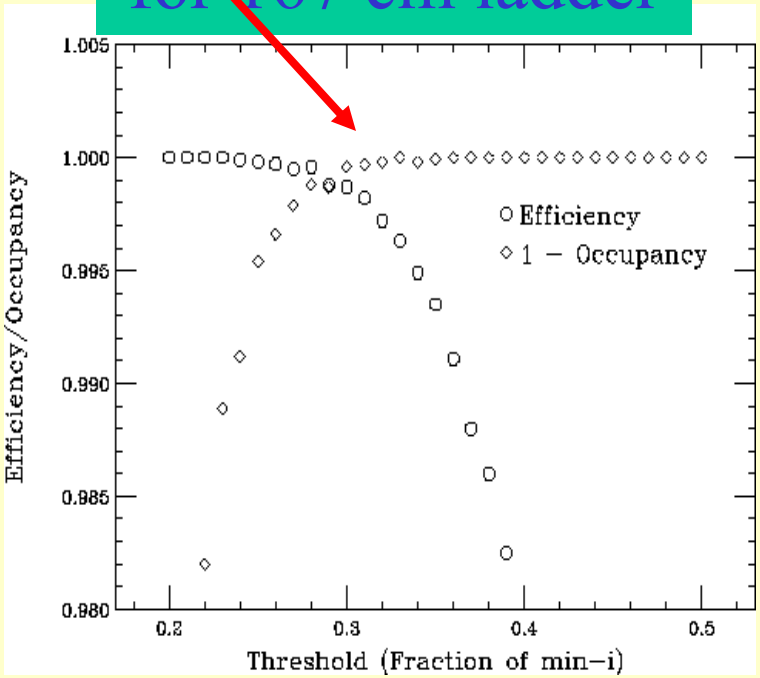




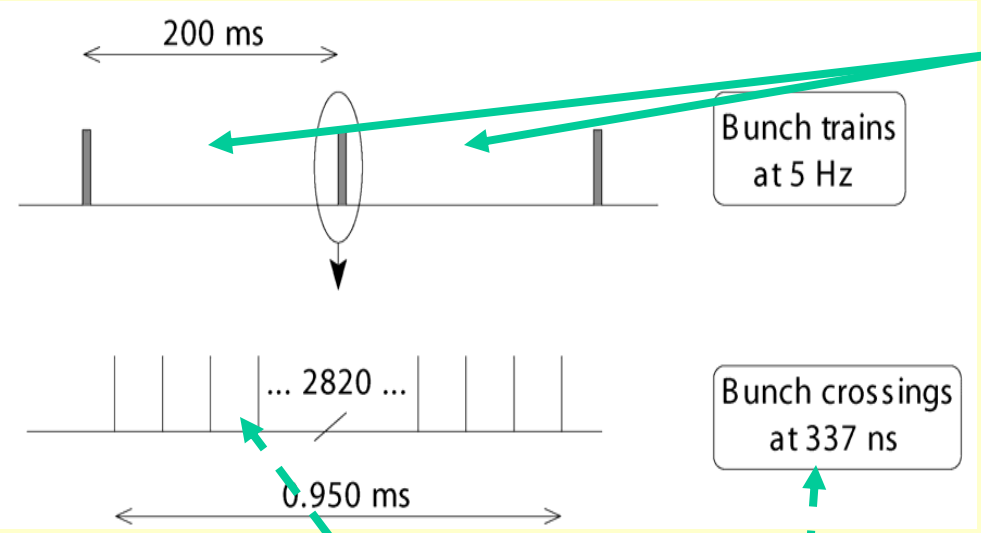
Shaping (μs)	Length (cm)	Noise (e^-)
1	100	2200
1	200	3950
3	100	1250
3	200	2200
10	100	1000
10	200	1850

Minimum-ionizing for 300μm of silicon is about 24,000 electrons

Operating point for 167 cm ladder



Simulations suggest that 3 μs shaping time allows ladders to be read from end only
➔ no electronics servicing.



'Just' switch electronics off during these dead periods

➔ ~99% power savings; eliminates need for active cooling

What about event pile-up in the tracker?

$$\sigma_t \cong \frac{\tau}{SNR}$$

Where SNR = signal-to-noise ratio. For τ = 3 μs and SNR = 12,

$$\sigma_t \cong 250 \text{ nsec}$$

Gossamer Tracker FEL Characteristics

Need to develop a chip that…

- Has low intrinsic noise
- Has long (several μs) shaping
- Can switch power on/off in ~100 μs
- Analog readout (centroid, dE/dX)
- Time stamping and pipeline

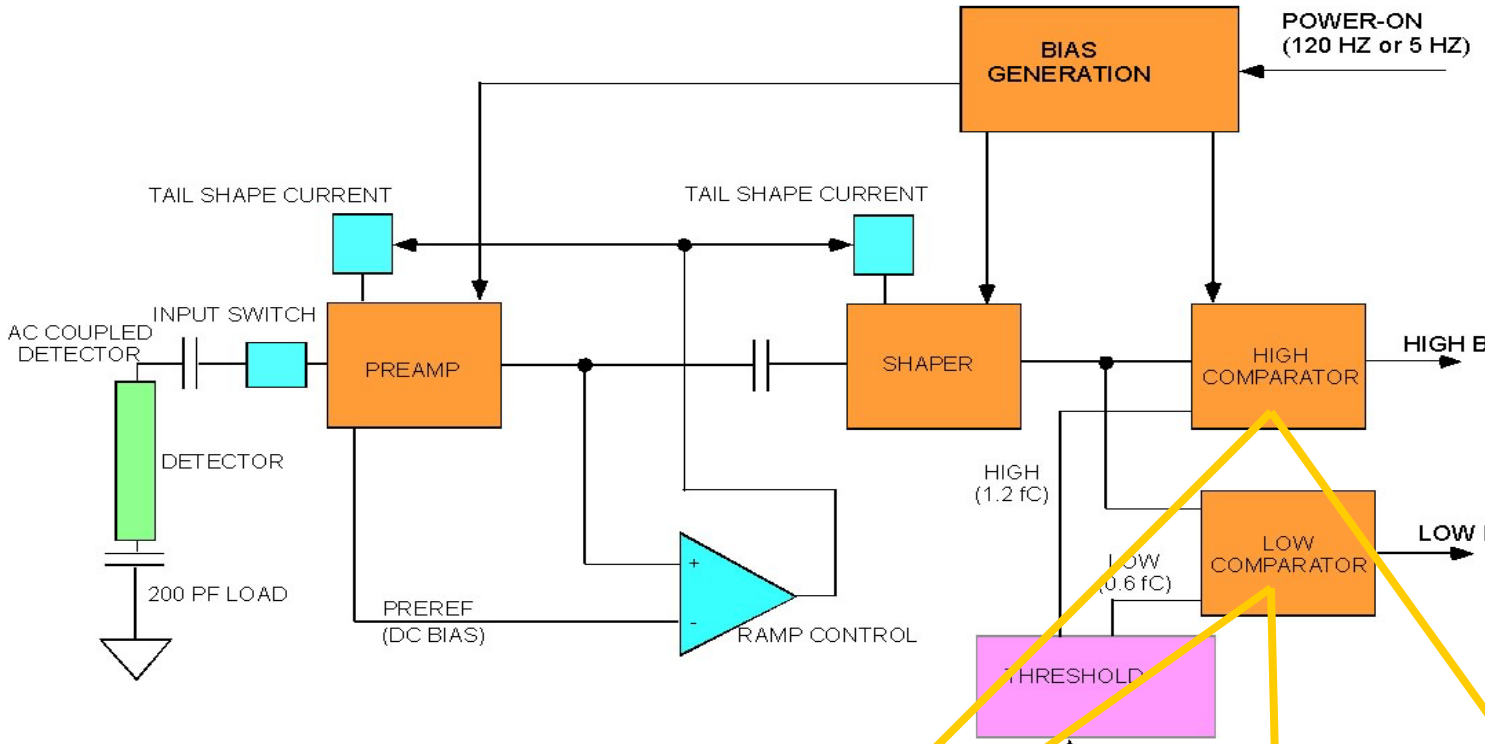
Complementary efforts at:

- LPNHE Paris
- UCSC (SCIPP)

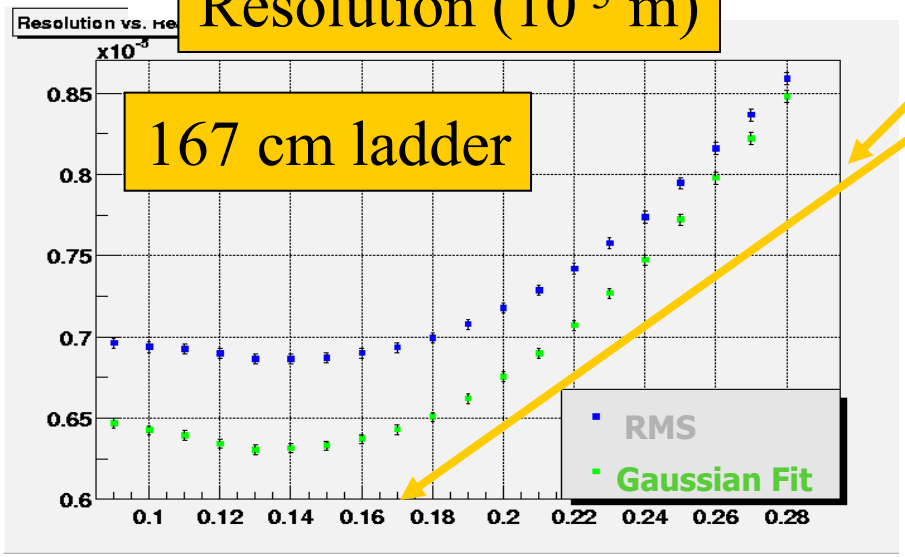
Both targeting fall prototype run

for example…

SILICON TRACKER FRONT-END ARCHITECTURE

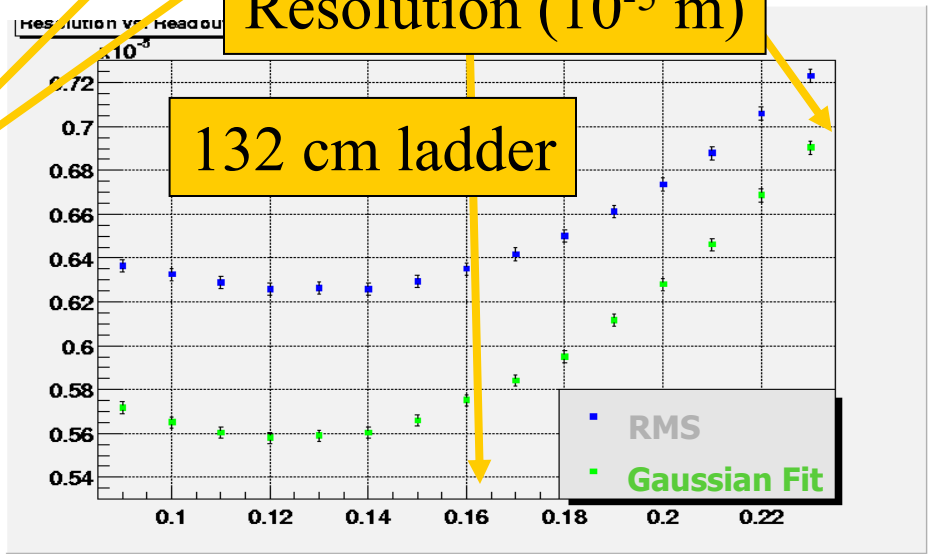


Resolution (10^{-5} m)



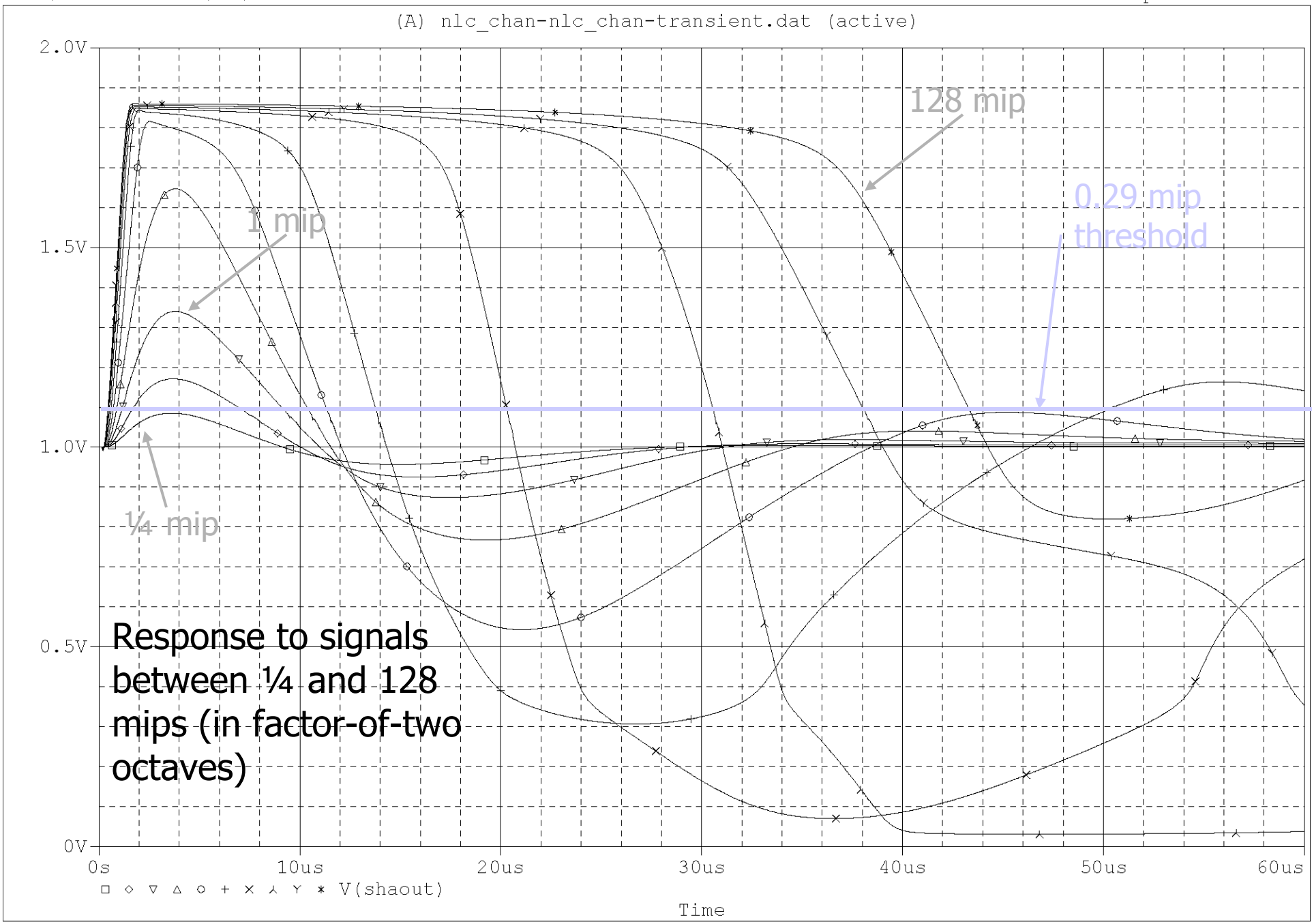
167 cm ladder

Resolution (10^{-5} m)



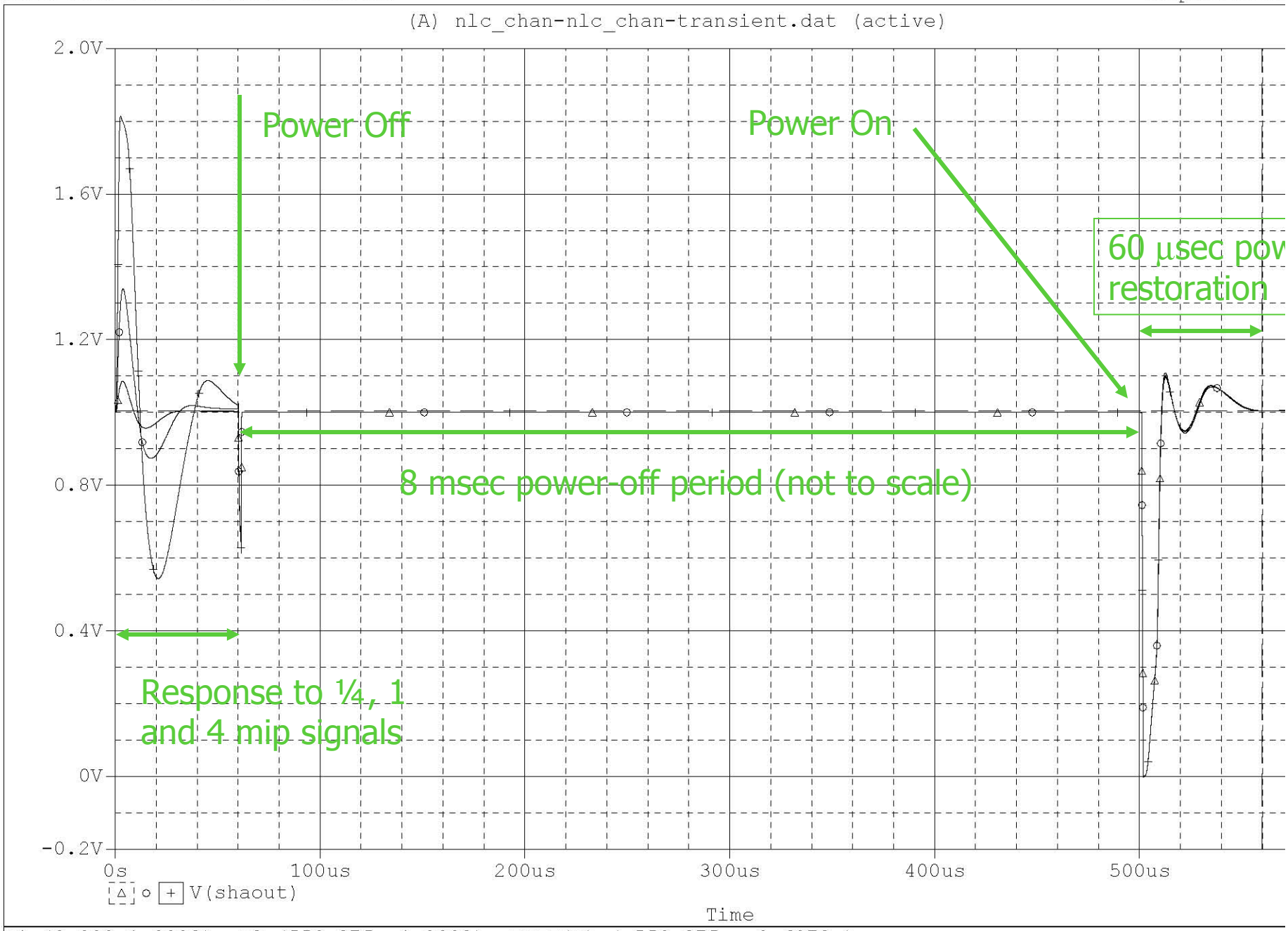
132 cm ladder

** Profile: "nlc_chan-transient" [C:\Projects\NLC\preampTSMCmodels\nlc_chan-nlc_chan-transient.sim]
Date/Time run: 01/02/04 14:15:19 Temperature: 27.0



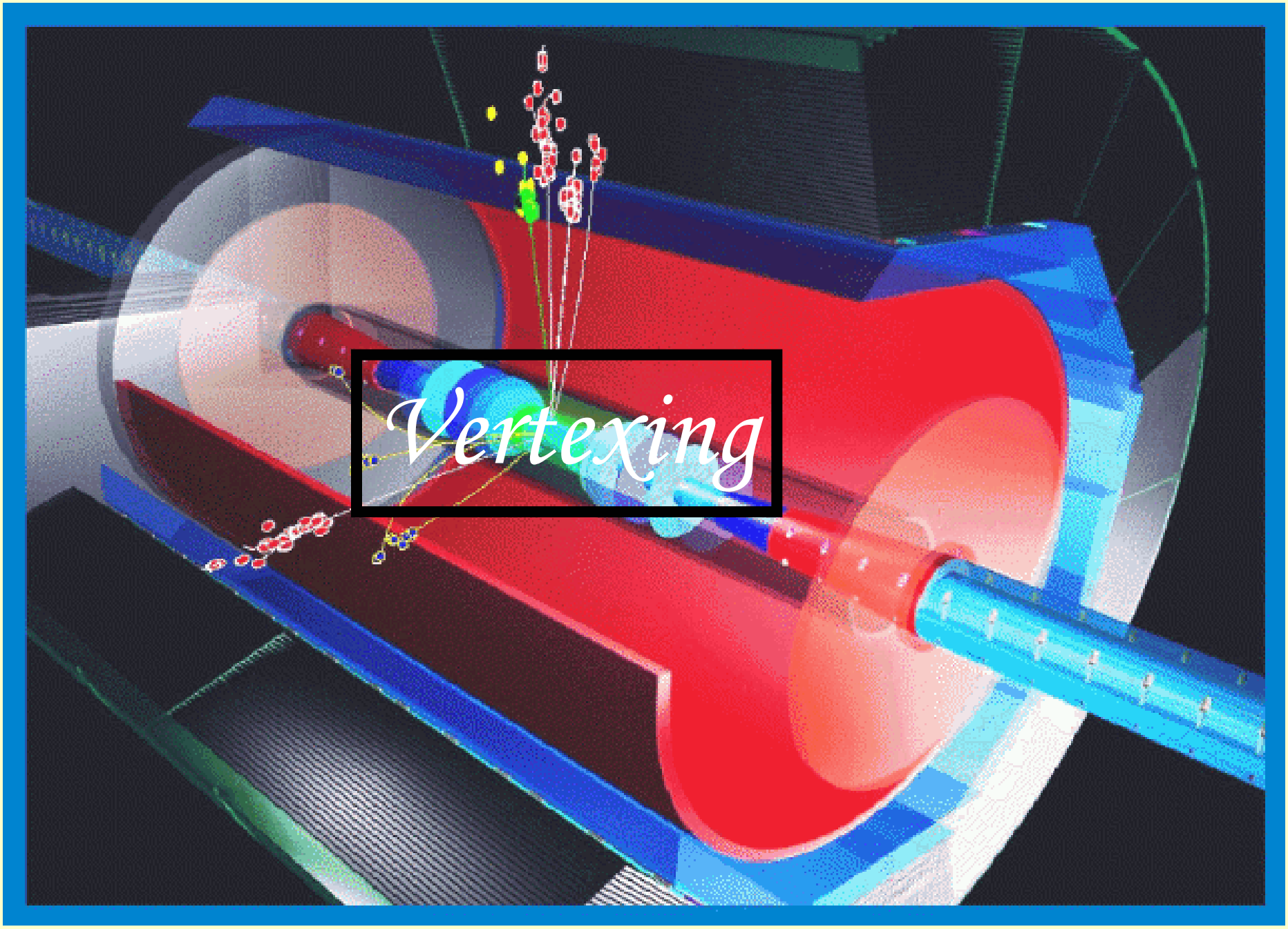
** Profile: "nlc_chan-transient" [C:\Projects\NLC\preampTSMCmodels\nlc_chan-nlc_chan-transient.sim

Date/Time run: 01/02/04 14:37:57 Temperature:

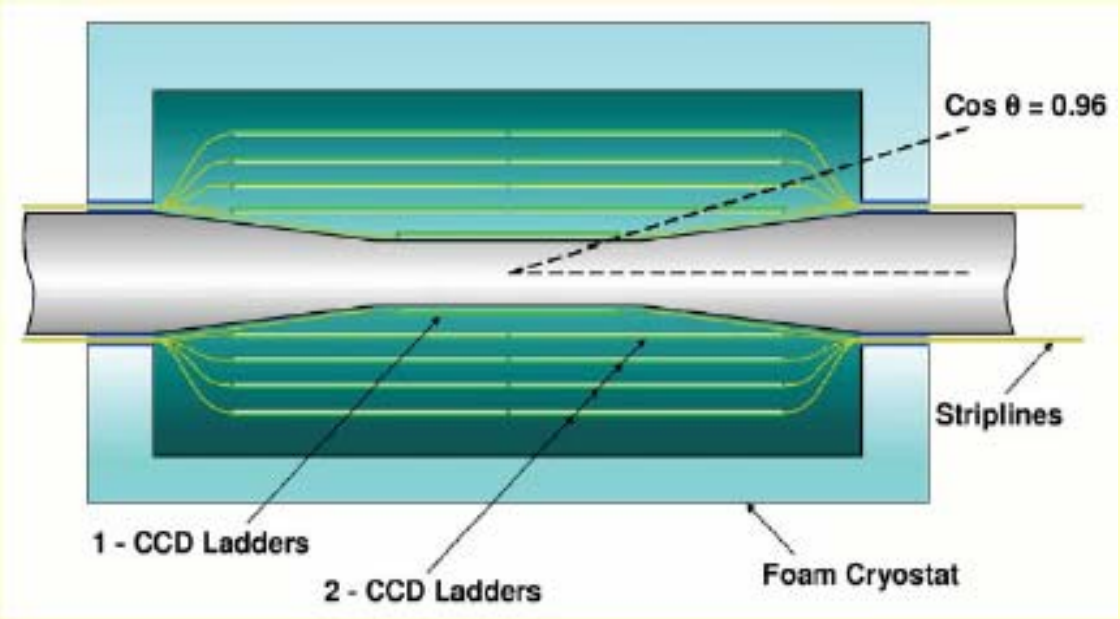


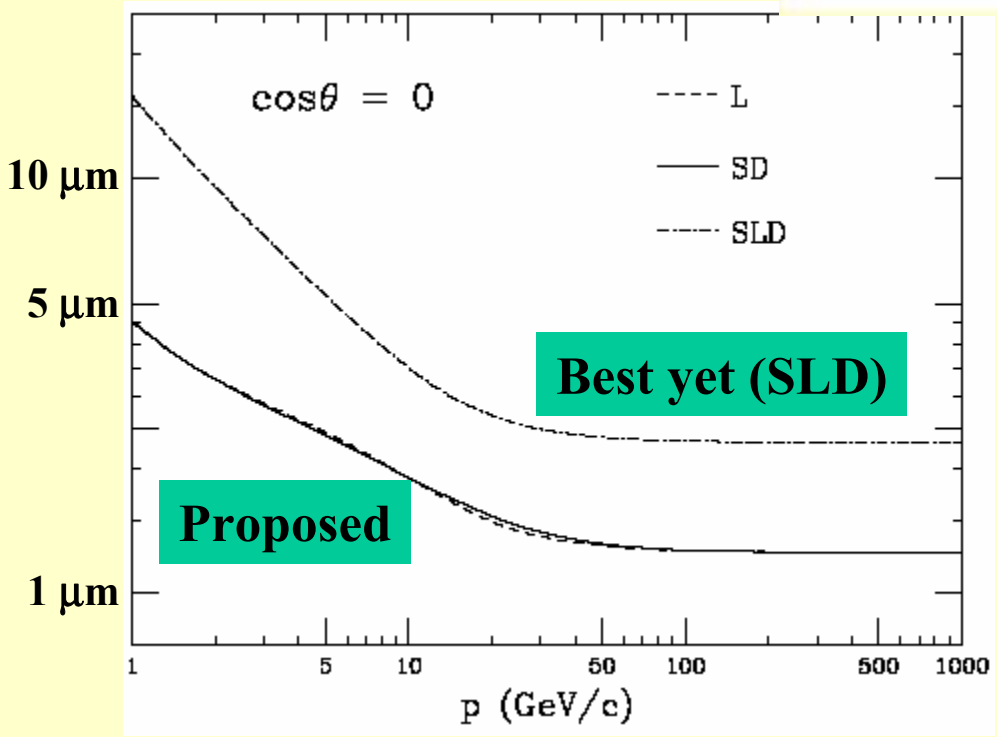
A1:(0.000,1.0002) A2:(559.875u,1.0038) DIFF(A):(-559.875u,-3.6378m)

Date: January 02, 2004 Page 1 Time: 14:


Vertexing

Global Baseline LC Vertex Detector





Optimistic projections achieved by very small (~20μm x 20μm) pixels and very thin (<0.1% X_0) layers

➔ Thinned CCD's

But: transition from SLC to LC application is not immediate…

Typical CCD sensor includes roughly ¼ million pixels and takes ~100msec to read out with a 5 MHz clock

For the LC, this would integrate over the full train of 2,820 pulses, leading to intractable backgrounds

➔ Speed up and de-serialize readout

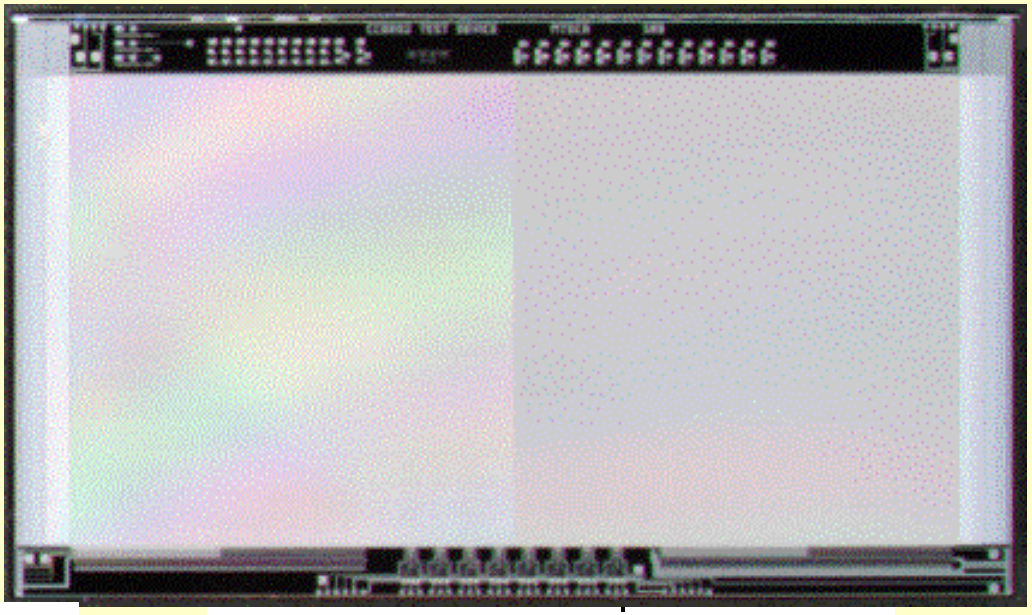
Column-parallel CCD readout architecture

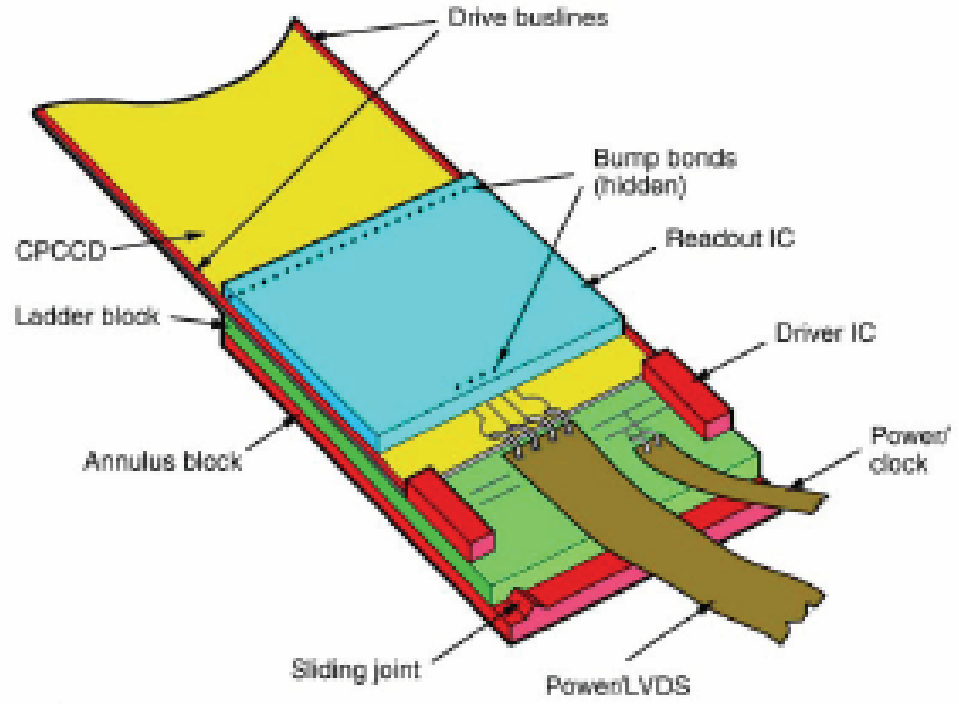
L C F I

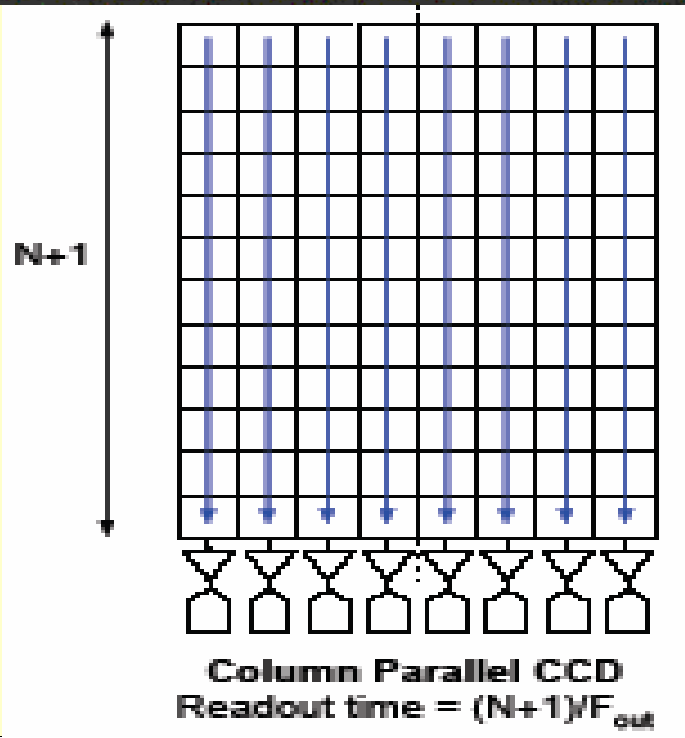
Column-parallel CCD has been developed (E2V corporation)

Readout scenarios under development

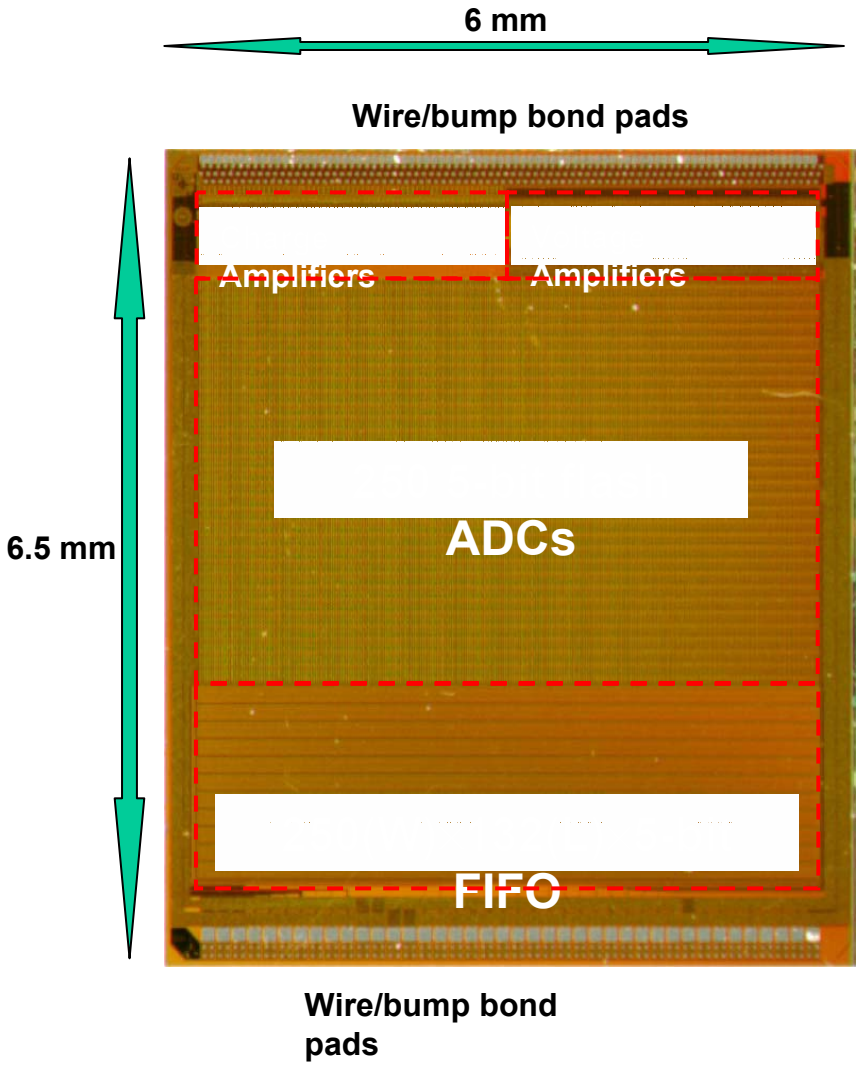
Our first CPCCD







Readout Chip CPR1

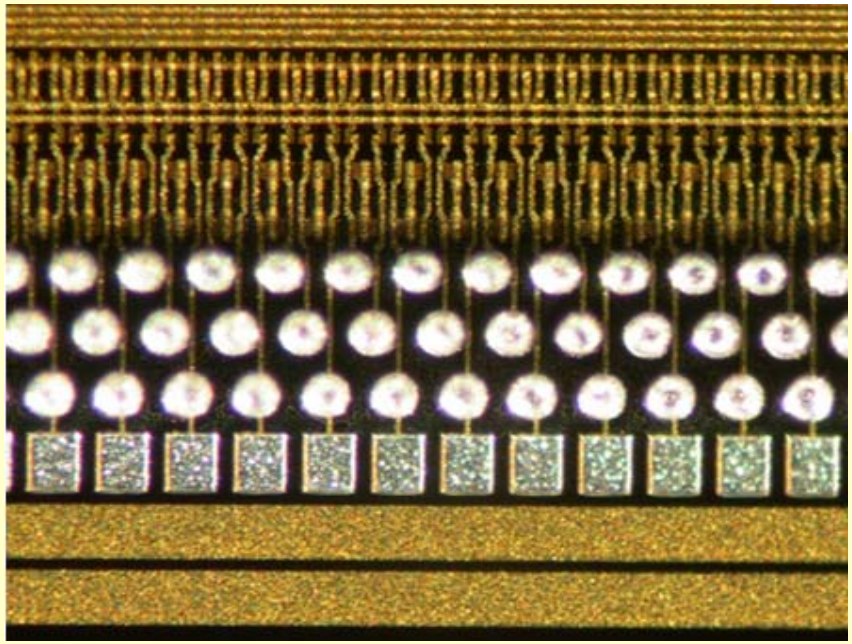


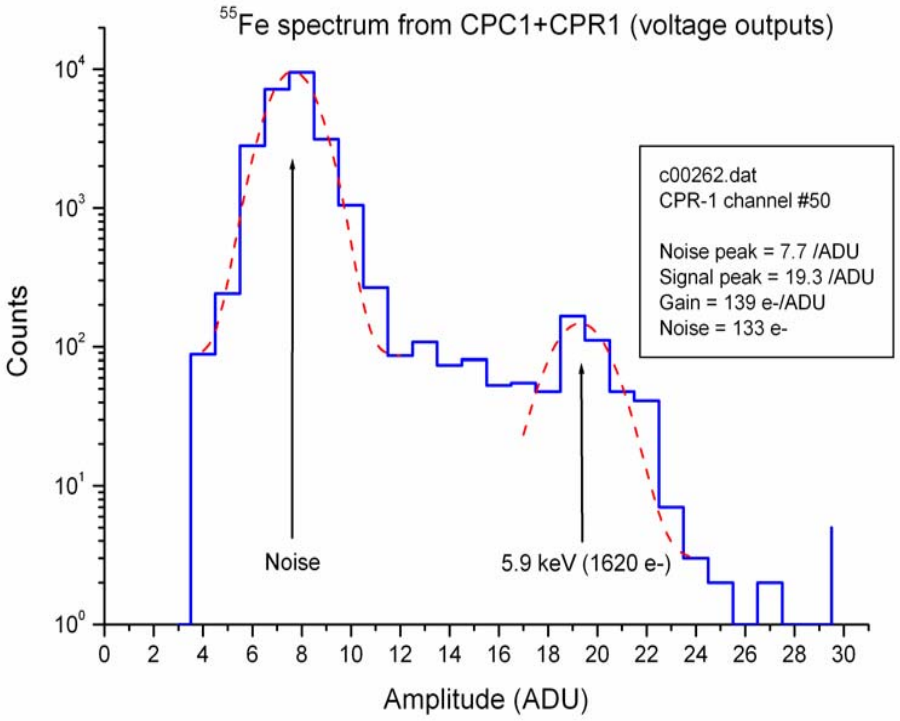
ASIC for CPC-1 readout

- design: RAL Microelectronics Group
- voltage amplifiers for 1-stage SF outputs
- charge amplifiers for direct outputs
- 20 μm pitch, 0.25 μm CMOS process
- wire- and bump-bondable
- scalable and designed to work at 50 MHz

L C F I

- **bump bonding performed by VTT (Finland)**
- **connecting to CCD channels at effective pitch of 20μm possible by staggering of solder bumps**





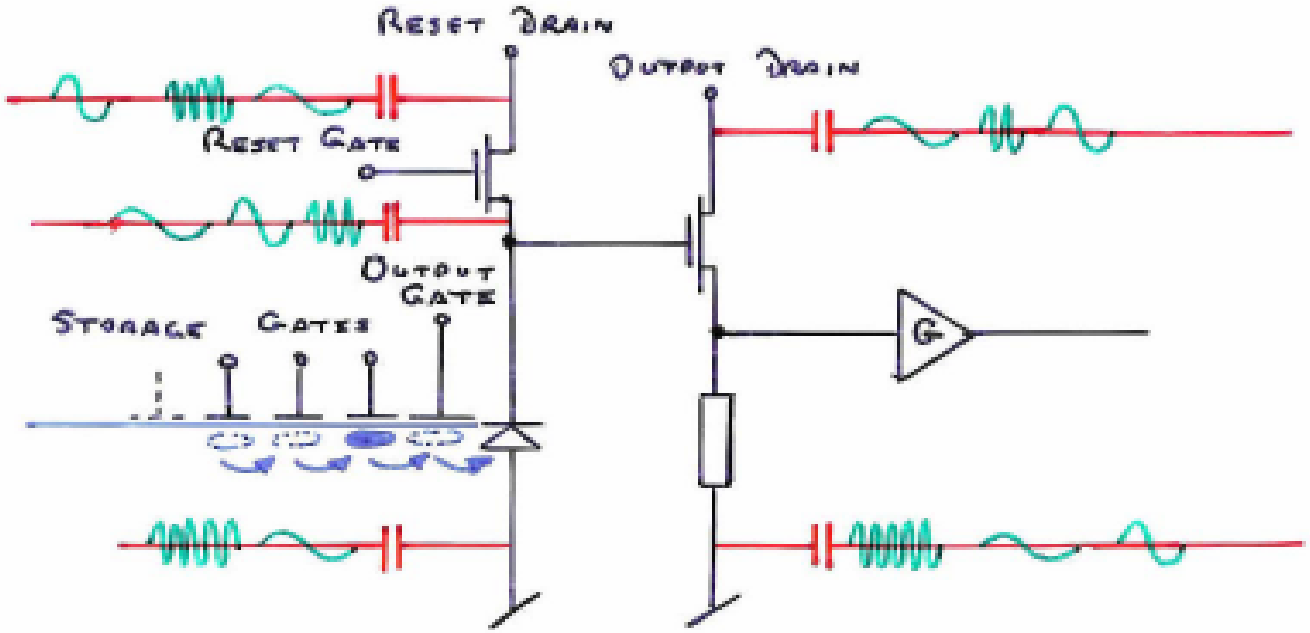
Spectrum (^{55}Fe) observed from voltage output (less aggressive) nodes; beginning to look promising

BUT: in order to avoid event pile-up, you must read out the detector (many times over!) during the spill…

L C F I

Chris Damerell, Rutherford Labs (LCWS04)

Readout at Linear Collider during bunch train:

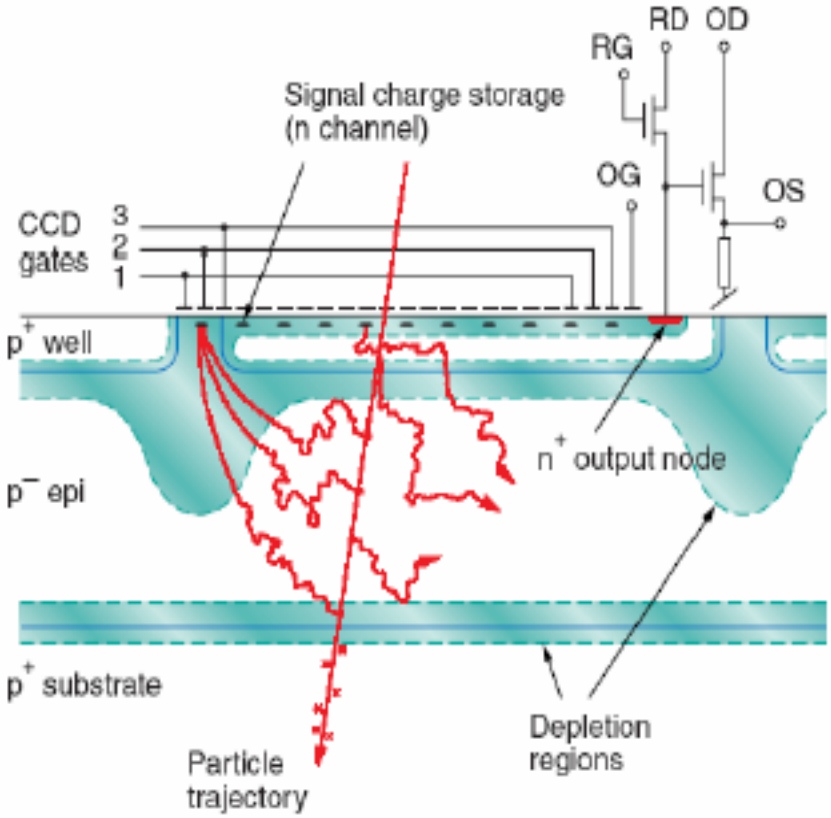


Malos's first rule of electronics: 'There is no such thing as ground …

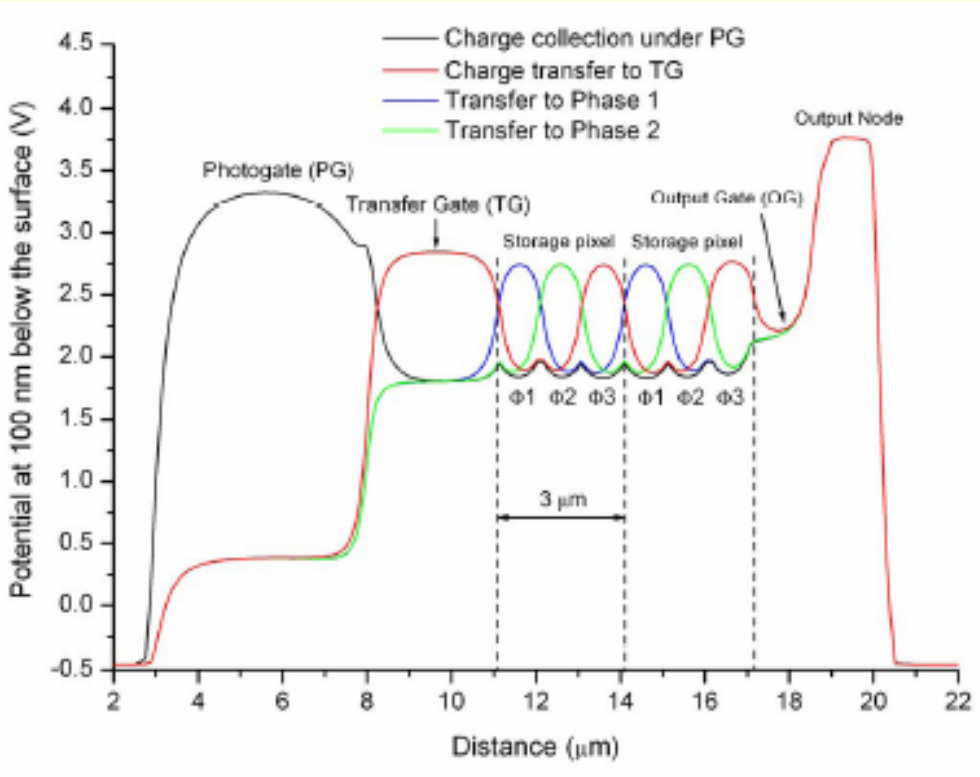
Why *whisper* just when an express train roars through the station?

In-situ storage of signal charge: a new architecture for TESLA

LCFI



Store charge in 20 slices during ~1μsec spill; read out between spills



But is there a Plan B???!

Progress in Active Pixel R&D

`Monolithic' designs (electronics deposited directly onto sensors) – why?

Typical current active pixel detector:

- Large-pitch pixel sensor (~100 μm or more)
- Readout circuitry with fill-factor ~1
- Bump bonds
- Servicing and cooling

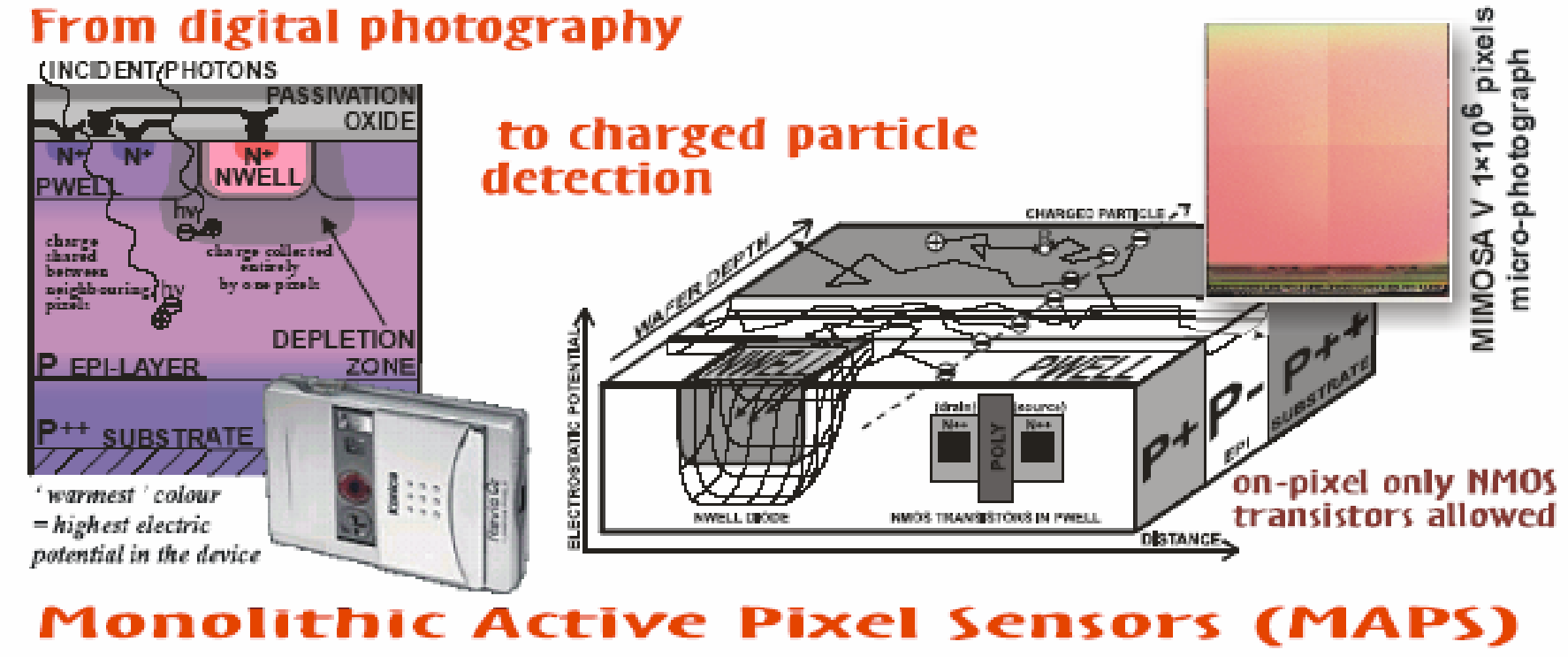
➔ Does not achieve ideal impact parameter resolution due to pitch and material burden

A number of different approaches are being explored…

- MAPS (Monolithic Active Pixel Sensor)
- FAPS (Flexible Active Pixel Sensor)
- DEPFET (Depleted Field Effect Transistor) APS
- SOI (Silicon on Insulator) APS

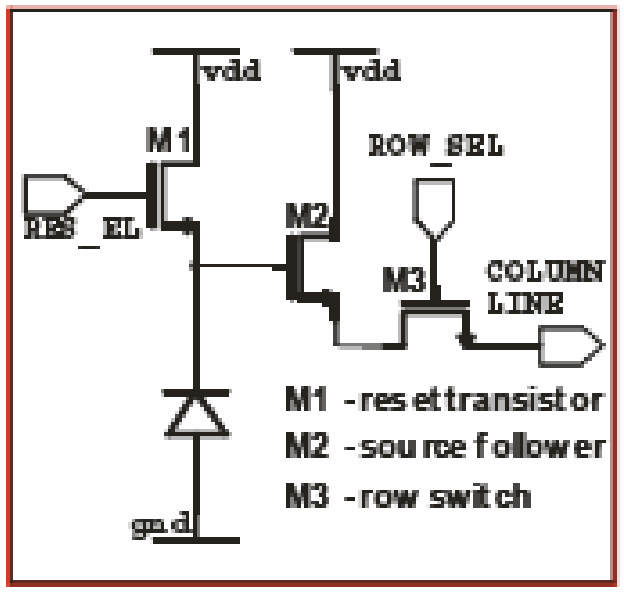
Active Pixel Sensors (APS)

Existing application in high-end digital photography; development for particle physics detection led by LEPSI electronics consortium at IRES Strasbourg.



Basic idea: readout grown directly onto expitaxial layer of VLSI sensor; charge collected via diffusion through epilayer

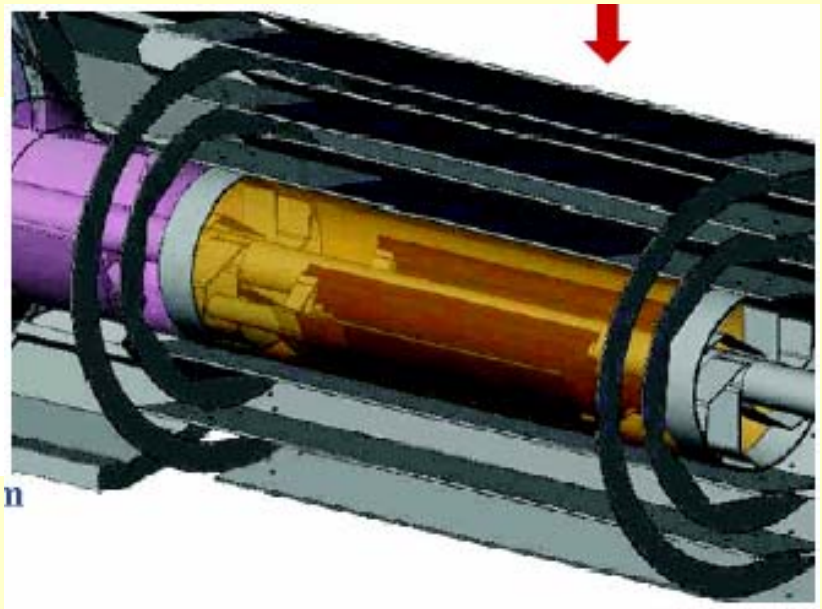
MIMOSA V: Proof of Principle



RESULTS:

Noise mean ENC:	20.74 e⁻
Single pixel S/N mean:	22.73
detection efficiency e:	99.3%
spatial resolution s:	1.7 µm
pixel-pixel gain nonuiformity	~3%
macro-scale gain nonuniformity:	~0.2%

Now under development: 'MIMOSA STAR' for use in STAR vertexing layers



Similar to CCD's, must go to faster, parallelized readout for Linear Collider ➔ increased on-pixel functionality

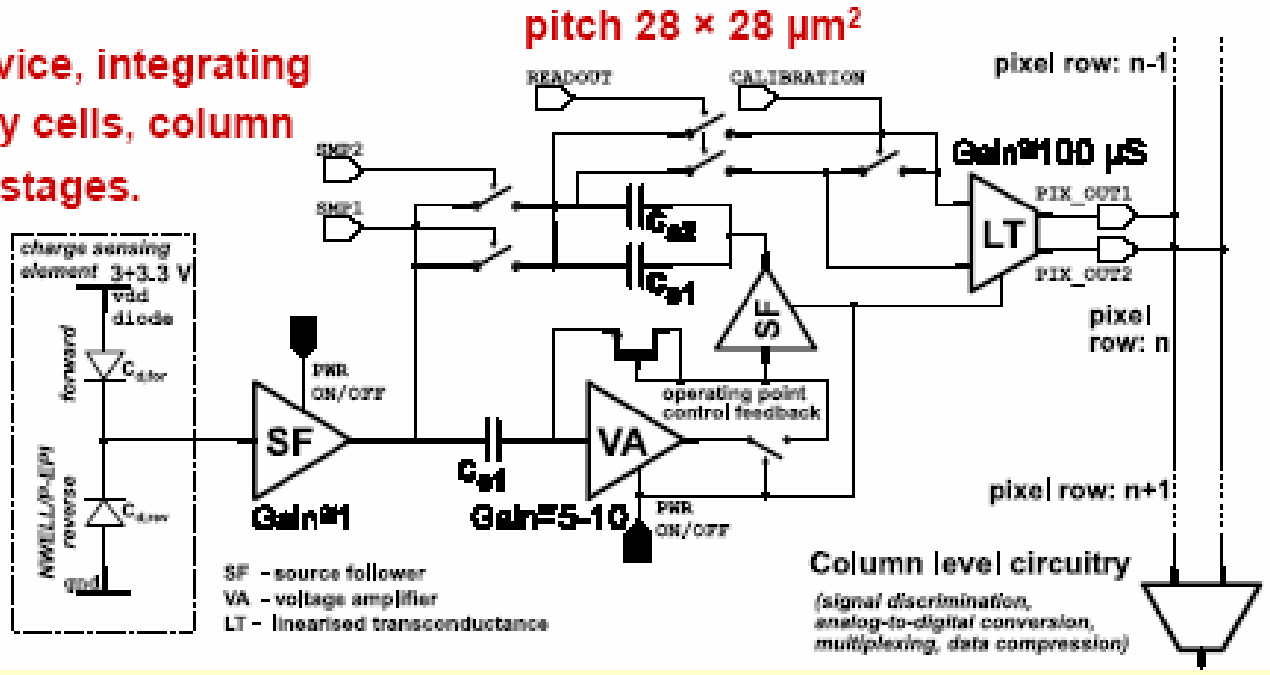
- Sample-and-hold (switched capacitors)
- Zero suppression
- Addressable for column-parallel readout

MIMOSA VI

MIMOSA VI - first tested device, integrating on-pixel voltage mode memory cells, column || readout, and discrimination stages.

main features:

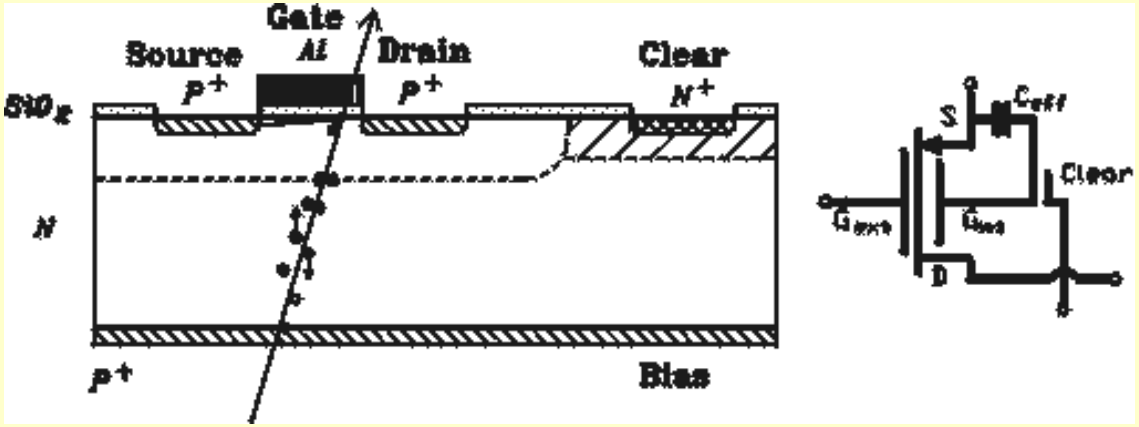
- mixed 0.35 µm process with 4 µm epitaxial layer,
- array of 128 rows × 30 columns read in || with CDS +signal discrimination (total 25 µs)
- AC coupled on-pixel voltage amplifier + CDS,



But deep submicron processes still promise attractive pitch, and active portion of device is intrinsically thin.

DEPFET principle and properties

DEPFET structure and device symbol



Function principle

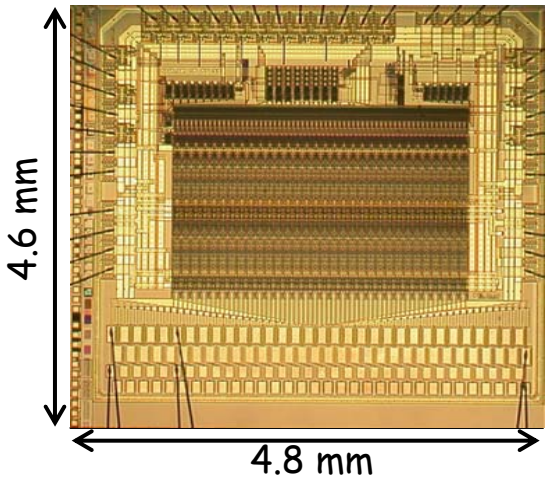
- Field effect transistor on top of fully depleted bulk
- All charge generated in fully depleted bulk; assembles underneath the transistor channel; steers the transistor current
- Clearing by positive pulse on clear electrode
- Combined function of sensor and amplifier

Participants: MPI Munich, MPI Halle, Mannheim, gGmbH Munich, Bonn; material presented here due to Gerhard Lutz, MPI Munich

DEPFET Matrix Read Out: ASICs

Development at the Universities Bonn and Mannheim

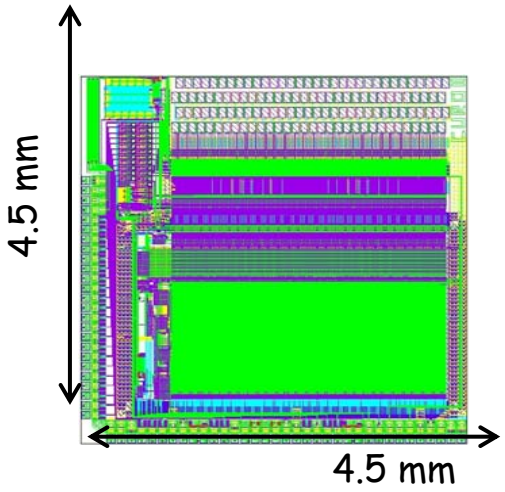
Switcher II:



Readout row selection chip

- AMS 0.8µm HV
- high speed
- high voltage range (20V)
- 64 rows=2x64 channels
- daisy chainable

CURO II:

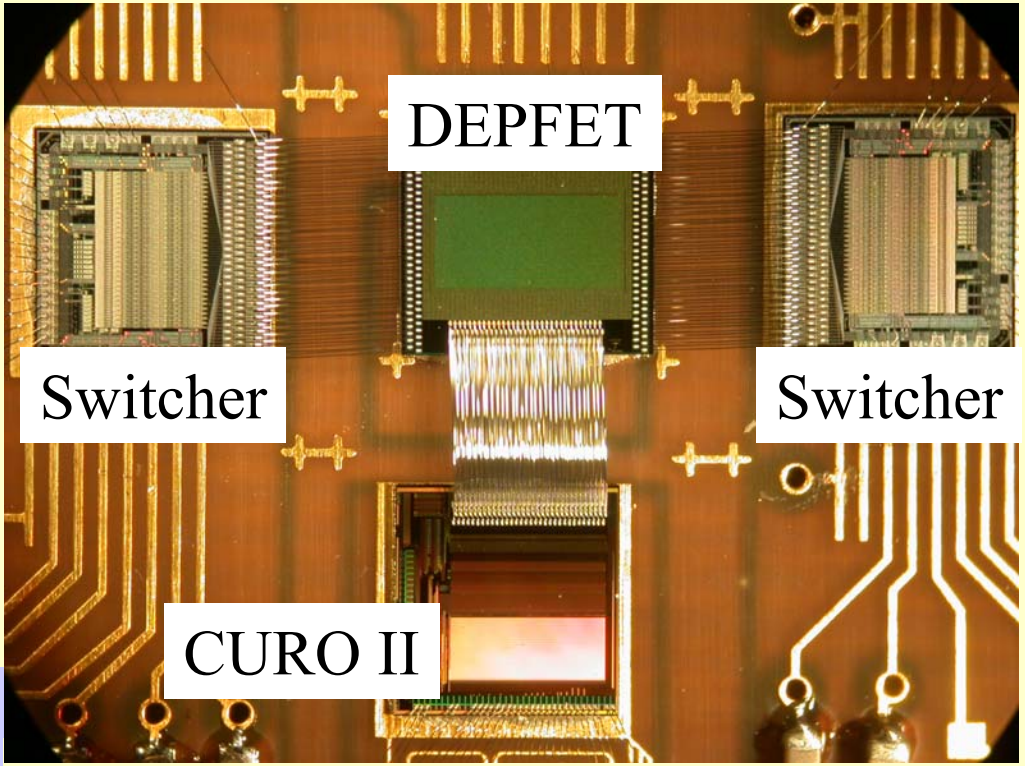


Fast RO chip for DEPFETs

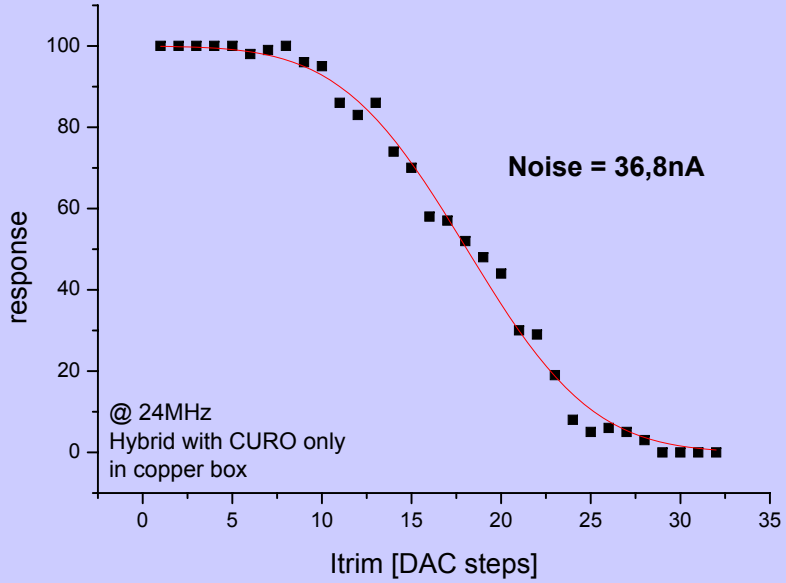
- TSMC 0.25µm, 5 metal
- 128 channels „CUrrent ReadOut“
- fast current based memory cells
- hit identification + zero suppression
- Correlated double sampling within 40ns

DEPFET STATUS

Basic versions in use in XRAY astrophysics, medical imaging.



noise perfomance via threshold scan:

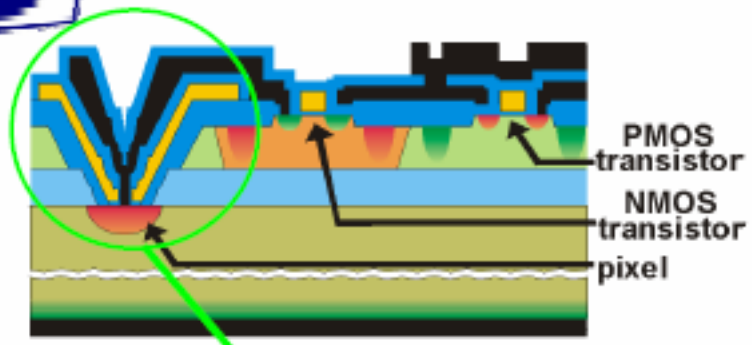


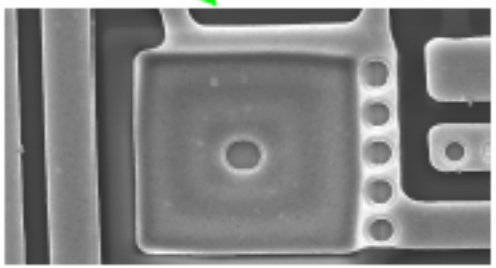
For LC: time structure, precision demand faster frame rate, power cycling; prototype is really just proof-of-principle at this point.

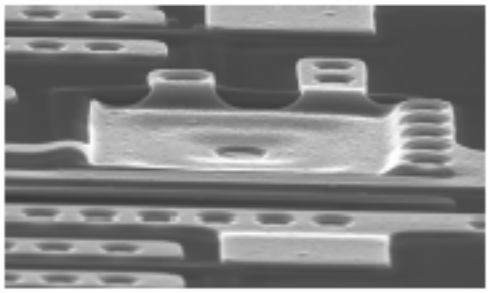
Silicon on Insulator (SOI) Detector Concept

AGH Krakow, IET Warsaw,U. of Insubria (Como)

Principle of SOI monolithic detector







The idea:

Integration of the pixel detector and readout electronics in the wafer-bonded SOI substrate

Detector → handle wafer

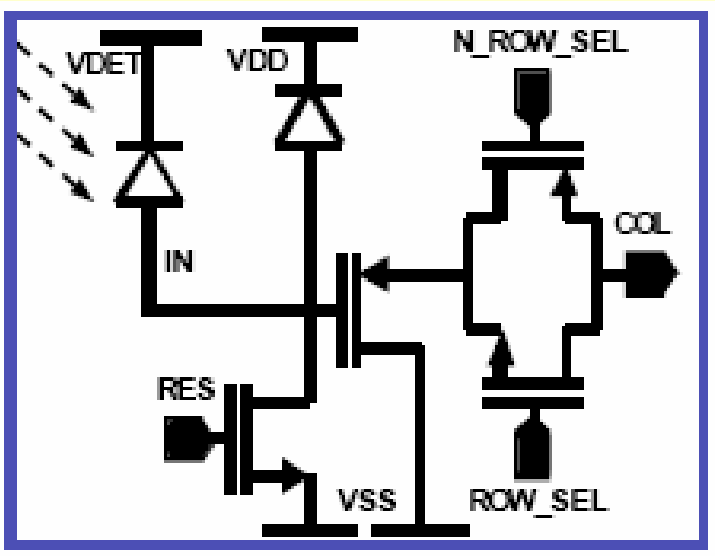
- High resistive (> 4 kΩcm,FZ)
- 300 μm thick
- Conventional p^+-n
- DC-coupled

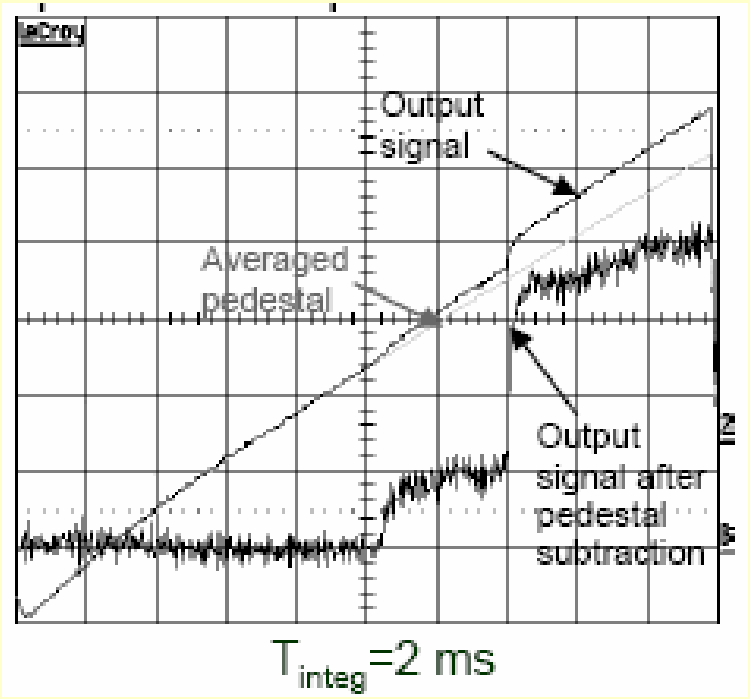
Electronics → active layer

- Low resistive (9-13 Ωcm, CZ)
- 1.5 μm thick
- Standard CMOS technology

Approach promises large signals since substrate is depleted; can use both NMOS and PMOS

Group has observed signals (^{90}Sr β source) with correlated sampling





But pixel size is large (150 x 150 μm^2) and integration time long

➔ Substantial R&D needed if technology is to be attractive for LC detector

Summary

LC detector development leading to many interesting R&D threads (with some interdisciplinary applications)

Most initiatives unique to LC (precision, bunch structure, power cycling)

Boundaries between detector and front-end electronics becoming obscured in some cases

Timeline for baseline (500 GeV) LC is surprisingly short: we are in the midst of the R&D phase

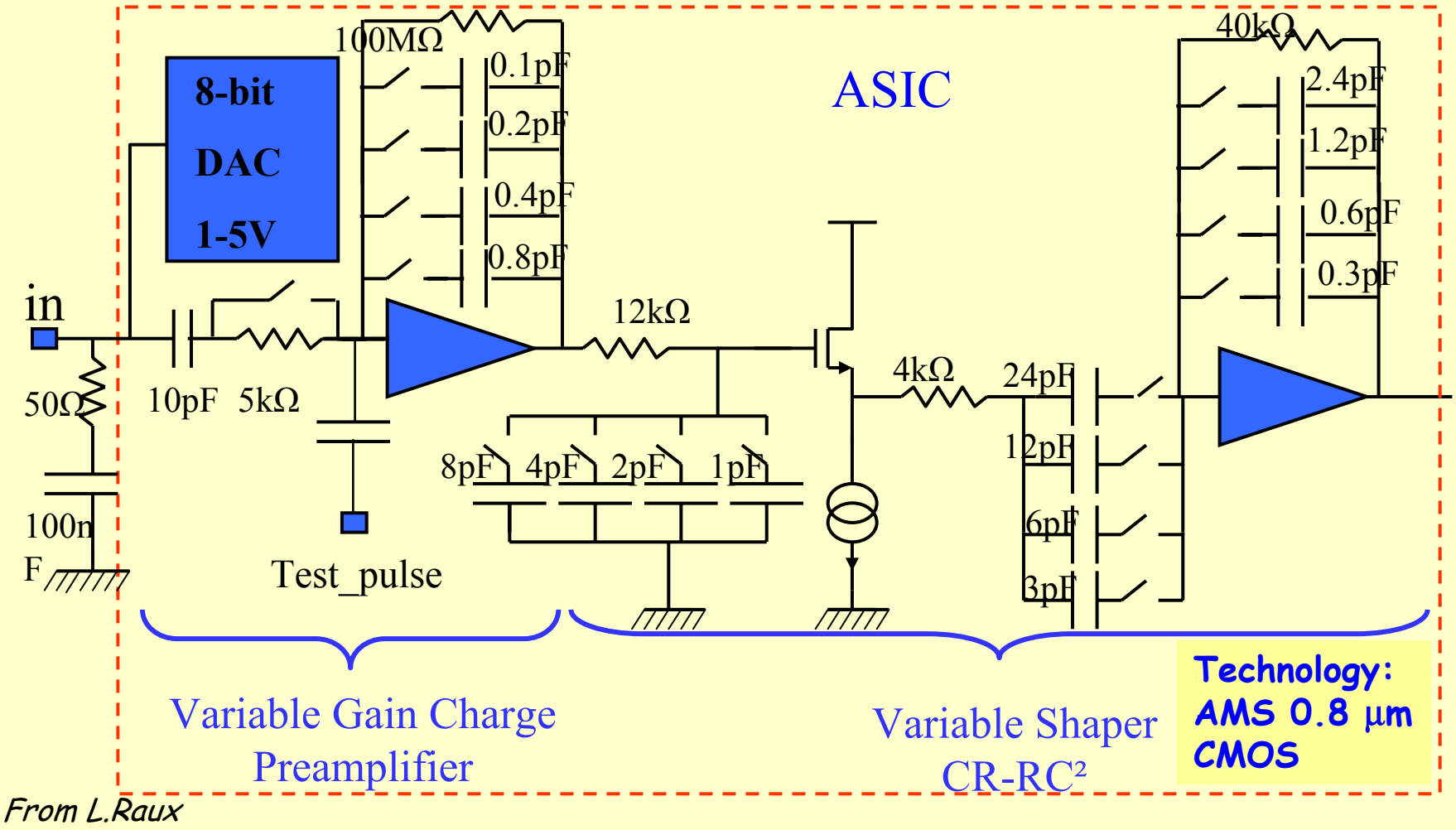
Next LC (machine) step: formation of International Design Group (IDG). Although far from certain, the LC is moving forward.

EXTRA SLIDES

Mimosa prototypes

CHIP	YEAR	PROCESS	EPITAXIAL	PITCH	METAL	PECULIAR
			µm	µm		
M1	1999	AMS 0.6 µm	14	20	3M	thick epitaxy
M2	2000	MIETEC 0.35 µm	4,2	20	5M	thin epitaxy
M3	2001	IBM 0.25 µm	2	8	3M	deep sub-µm
M4	2001	AMS 0.35 µm	0 !	20	3M	low dop. Substrate
SUC 2	2003	AMS 0.35 µm	none	40	3M	low dop. Substrate (SUCIMA project)
M5 & M5B	2001/2003	AMS 0.6 µm	14	17	3M	real scale 1M pixels
M6	2002	MIETEC 0.35 µm	4,2	28	5M	col. // r.o. and integrated spars.
M7	2003	AMS 0.35 µm	none	25	4M	col. // r.o. and integ. spars. (photoFET)
M8	2003	TSMC 0.25 µm	8	25	5M	col. // r.o. and integrated spars.
M9	2004	AMS 0.35 m	20	20/30/40	4M	opto. tests diodes/pitch/leakage current.
SUC 1						irradiation tests

Variable Shaping-Time / Variable Gain ASIC



From L.Raux