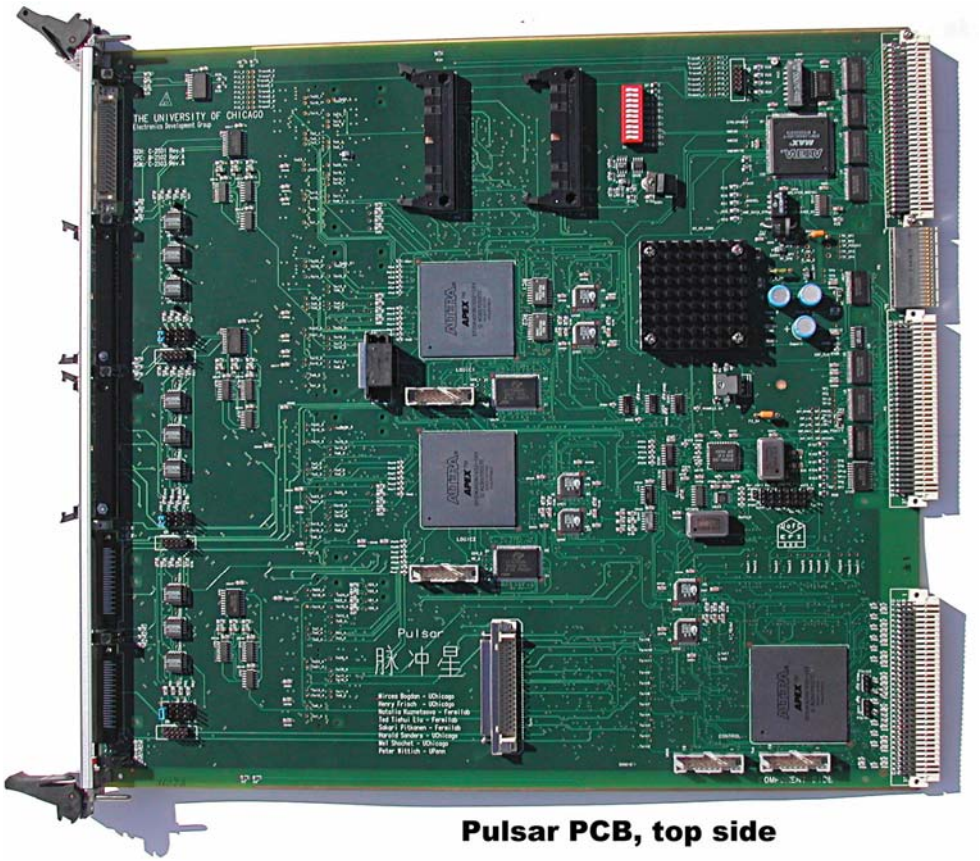
CDF Level 2 Trigger Upgrade: The *Pulsar* Project



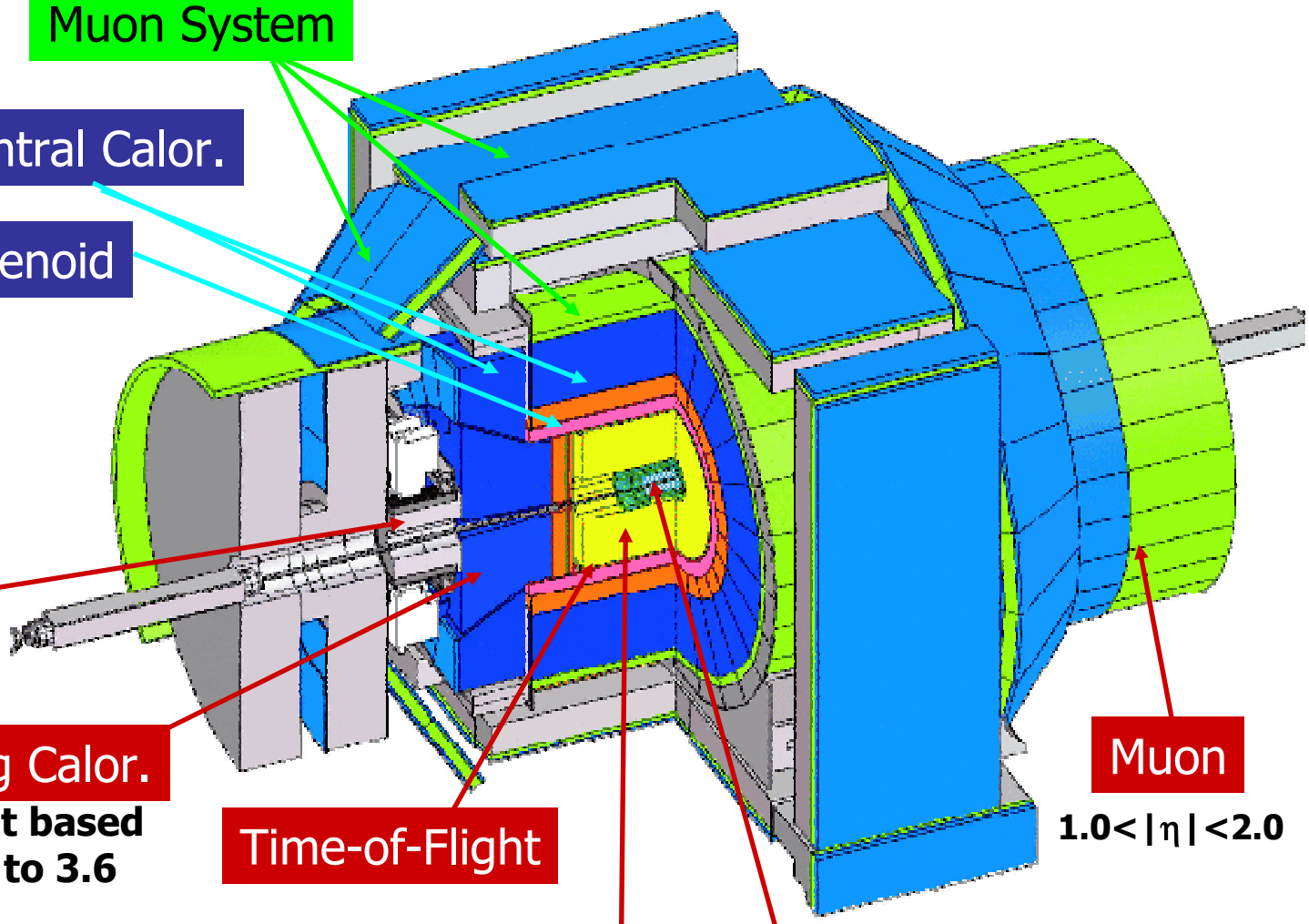
Pulsar PCB, top side

Burkard Reisert (FNAL)
(for the CDF Pulsar group)

10th Workshop on Electronics for LHC and Future Experiments

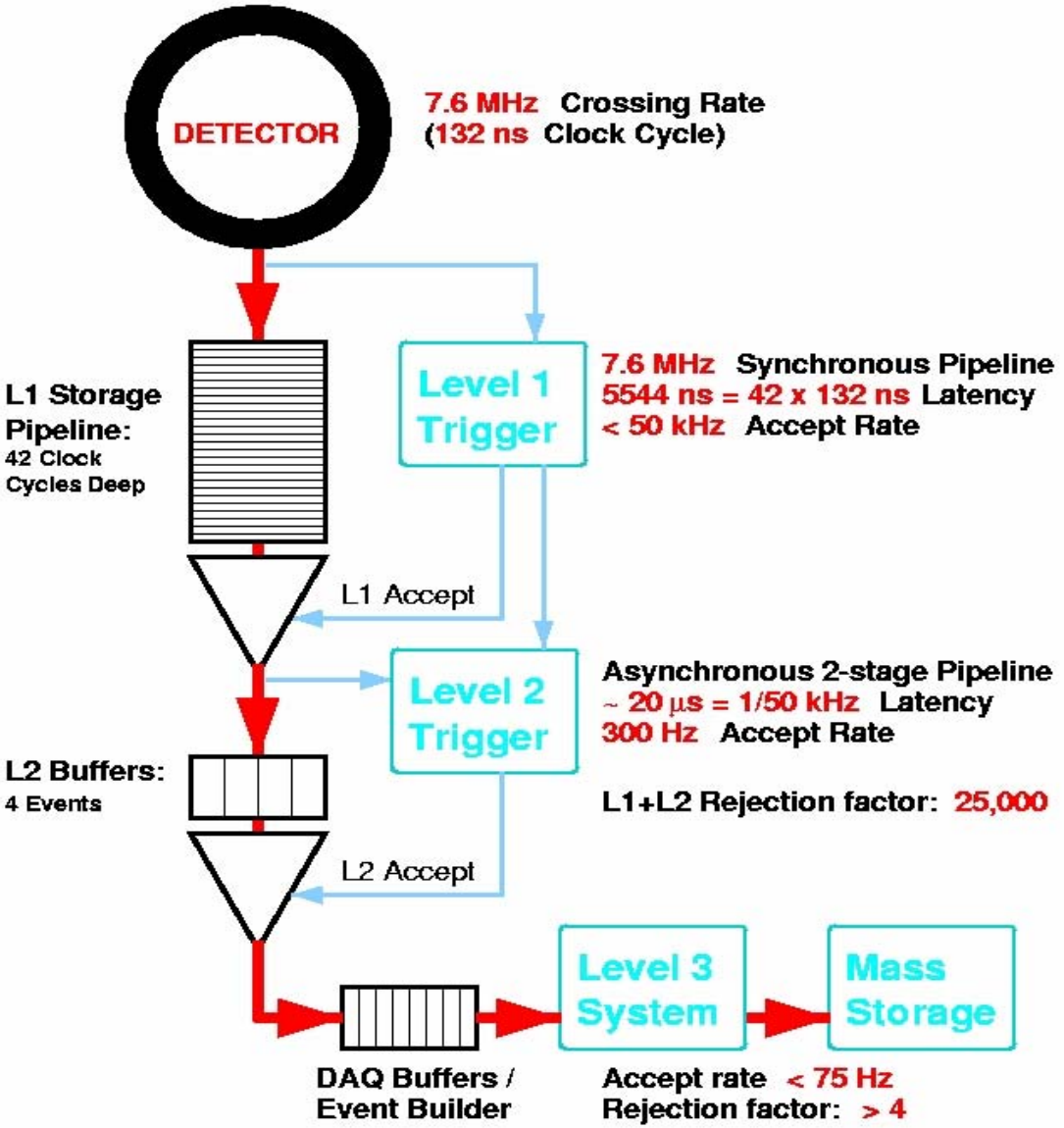
Pulsar web page:
http://hep.uchicago.edu/~thliu/projects/Pulsar/

CDF Detector



CDF Data Acquisition System

- **Level 1 trigger**
  - pipelined and "dead timeless"
  - fully synchronous
  - designed for 132ns operation
  - on L1A, write data to 1 of 4 local L2 buffers
- **Level 2 trigger**
  - asynchronous
  - L1 + supplemental info
- **Level 3 trigger**
  - full detector readout
  - PC farm runs reconstruction
  - output to mass storage



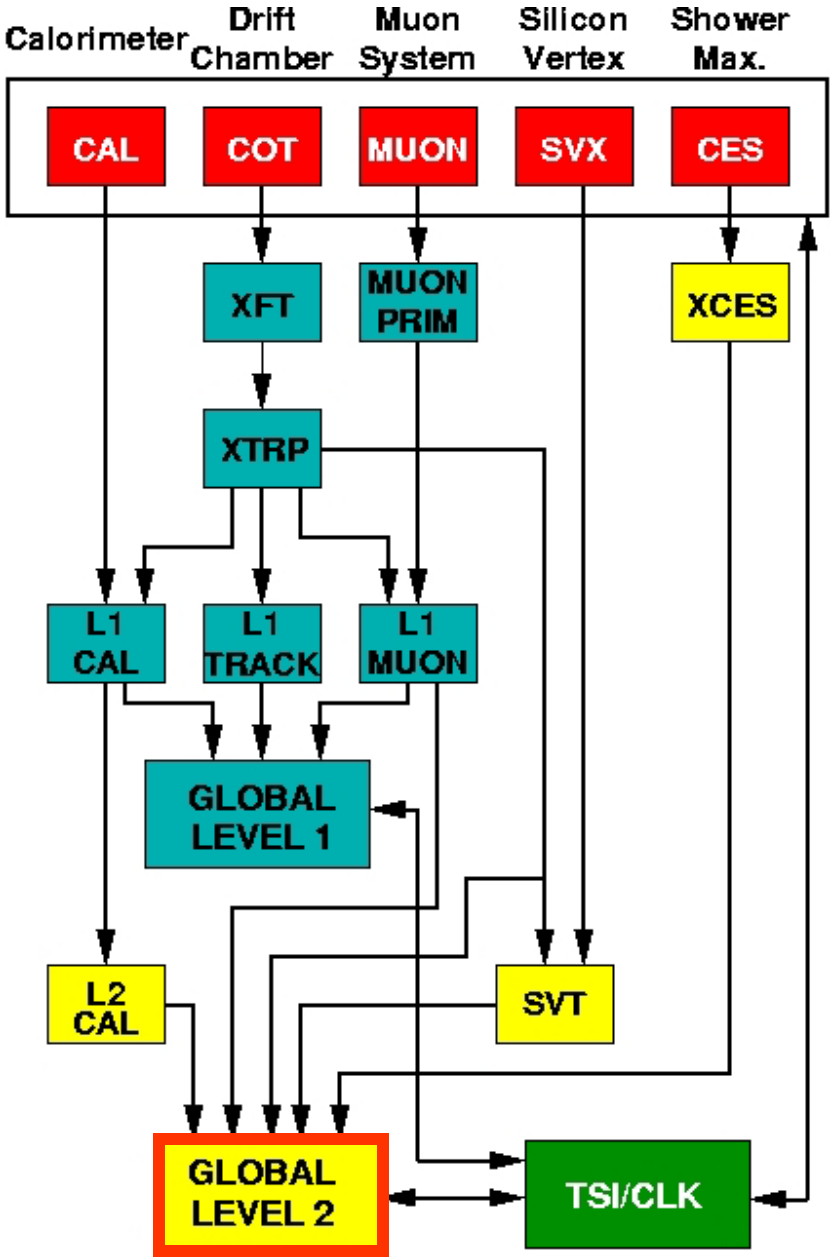
CDF L2 Legacy Decision Crate

Technical requirement: need a FAST way to collect/process many inputs…

→With the technology available back then (1990s), had to design custom (alpha) processor & backplane (magicbus) …

→had to deal with the fact that each data input was implemented in a different way …

→9U VME crate with 6 different types of custom interface boards + custom processor & custom backplane …



Each L2 input data path has been implemented differently:

	Silicon Vertex Trigger	Fast Track Trigger	Level1 Decision	Calorimeter Cluster & Isolated Cluster Trigger		Muon Systems	Shower Max
	SVT	XTRP	L1	CList	ISO	Muon	Reces
Interface hardware	LVDS cable (svt type)	LVDS cable (svt type)	LVDS cable (L1 type)	optical fiber (hotlink)	optical fiber (Taxi)	optical fibers (hotlink)	Optical fibers (Taxi)
Input data clock	30 MHz	7.6 MHz	7.6 MHz	20 MHz	12 MHz	32 MHz	7.6 MHz
Data size range	117 bits/trk	21 bits/trk	96 bits/evt	46 bits/clu	145 bits/clu	11k bits/evt	1.5k bits/evt
Data length	Variable n svt-trks	Variable n tracks	fixed	Variable n cluster	Variable n isoclu	fixed	fixed

(this table just lists a few examples to give the flavor)

Requirements for a new L2 System

Base line performance of legacy L2 System (CDF RunIIa):

input rate to L2: 20 kHz, output rate to L3 300 Hz

Baseline for upgrade (RunIIb):

inst. Luminosity increase by factor ~3 → increased occupancy

input rate to L2: 30 kHz, output rate to L3 300Hz to 1kHz

Goals for new Level2 system:

reduce execution time on L2

increase flexibility, reliability and testability

guarantee long term maintainability (end of CDF)

need to be compatible with all legacy input systems

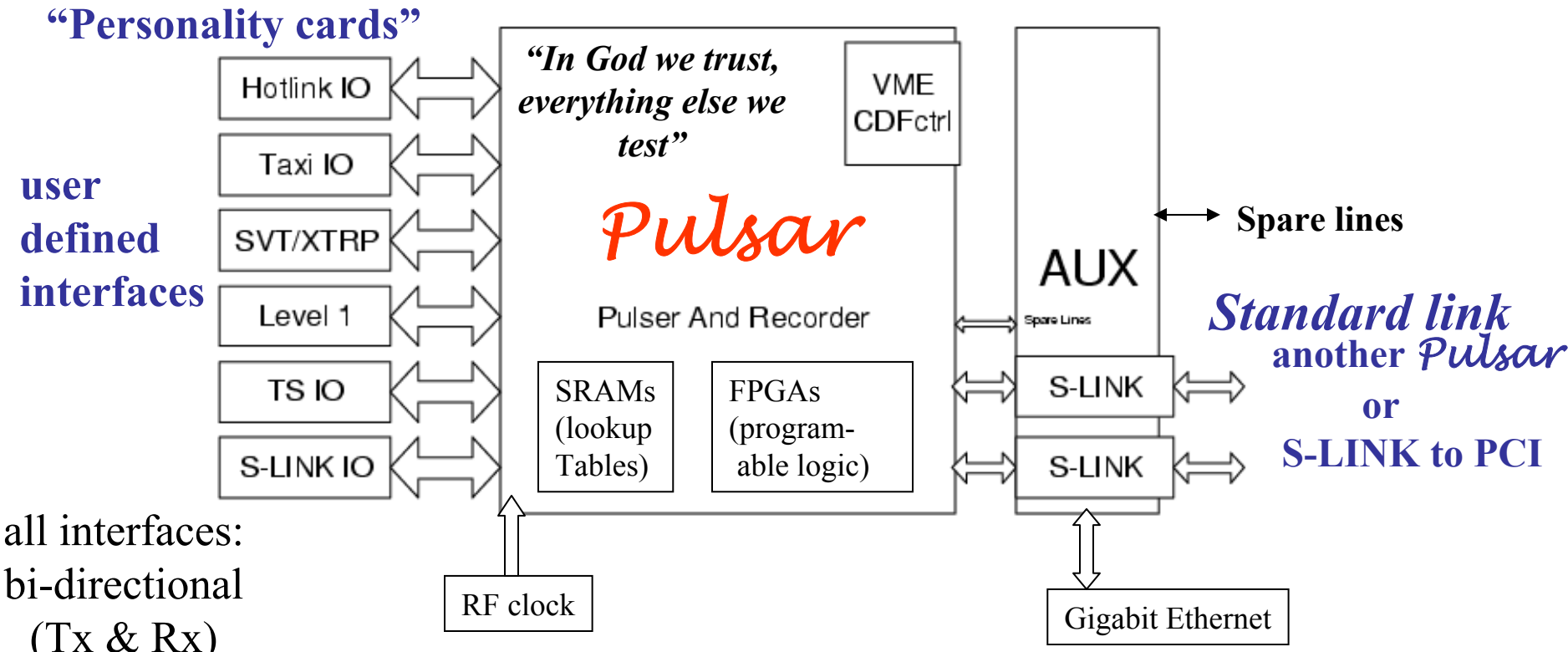
Pulsar Approach:

- Built one universal interface board
- send all data to a commercial available CPU via a standardized link

Pulsar is designed to be:

Modular, universal & flexible, fully self-testable (board &system level)

Each board has ALL interfaces L2 decision crate has



Pulsar Design Methodology

A major fraction of the effort was dedicated to extensive design optimization & verification:

Firmware:

- Leonardo Spectrum: VHDL synthesis
- Altera Quartus II: place and route, FPGA level simulation

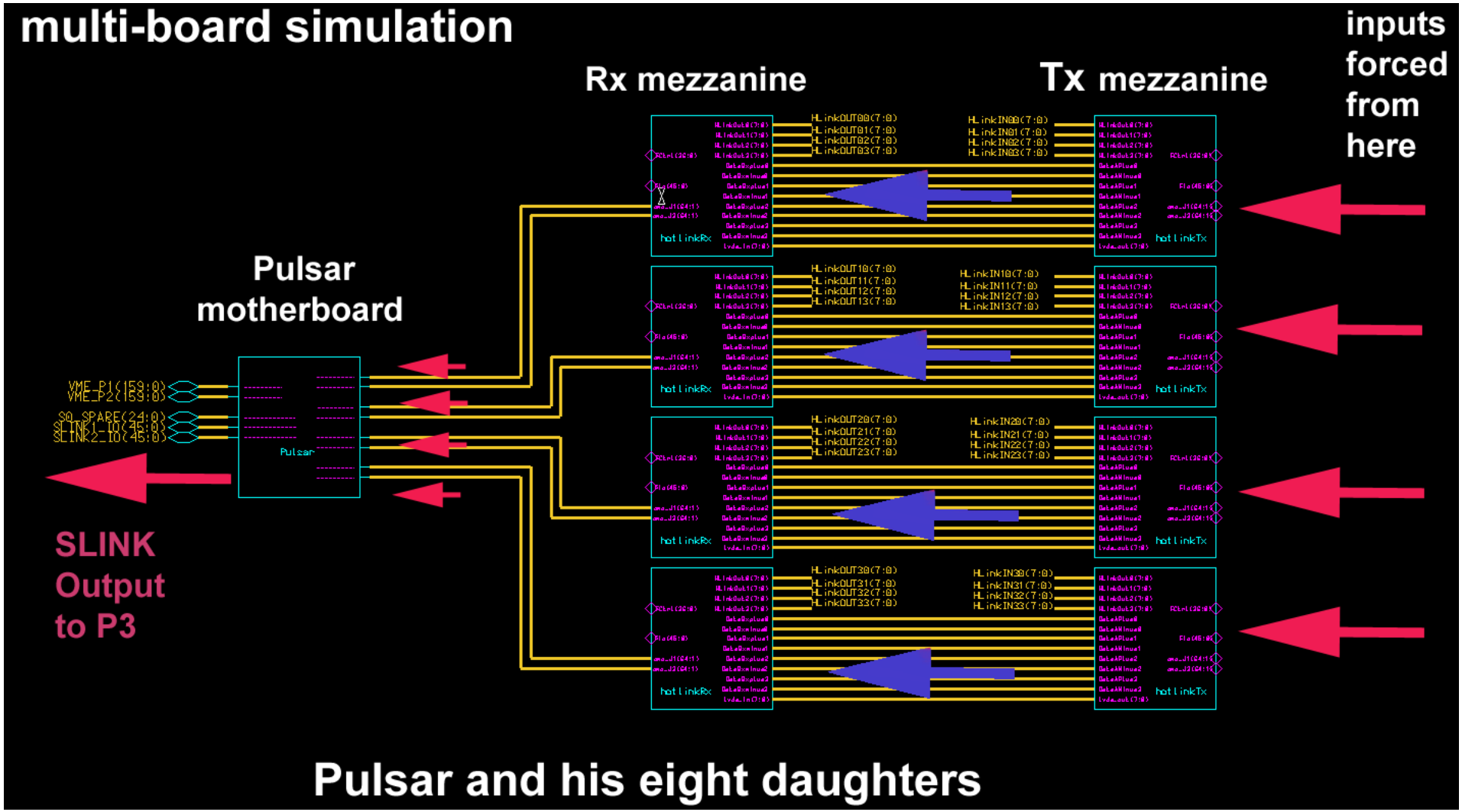
Printed circuit board (PCB) design:

- Mentor Graphics QuickSim: (multi)-board level simulation
- Interconnect Synthesis tool: trace & cross talk analysis
- IS_MultiBoard tool: signal integrity between motherboard & mezz cards

Design work done mostly by Fermilab Physicist/student & Univ. of Chicago engineer

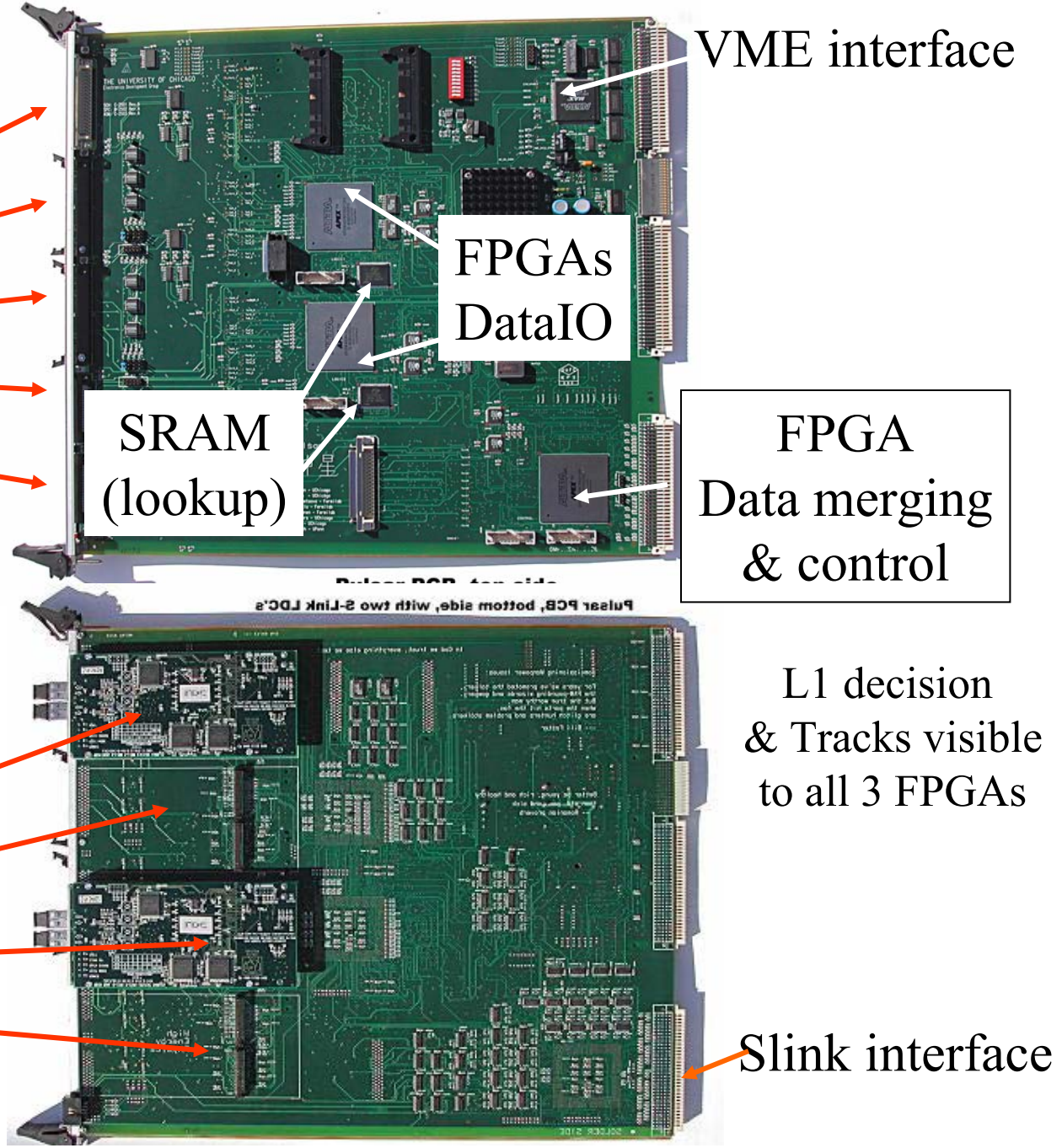
Example: Multi-board (9 boards) simulation

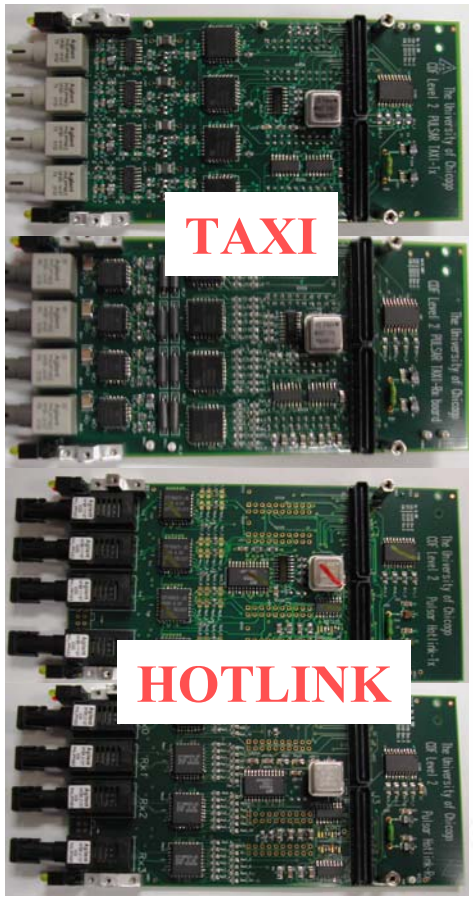
(from input *connector pins* to output *connector pins*)

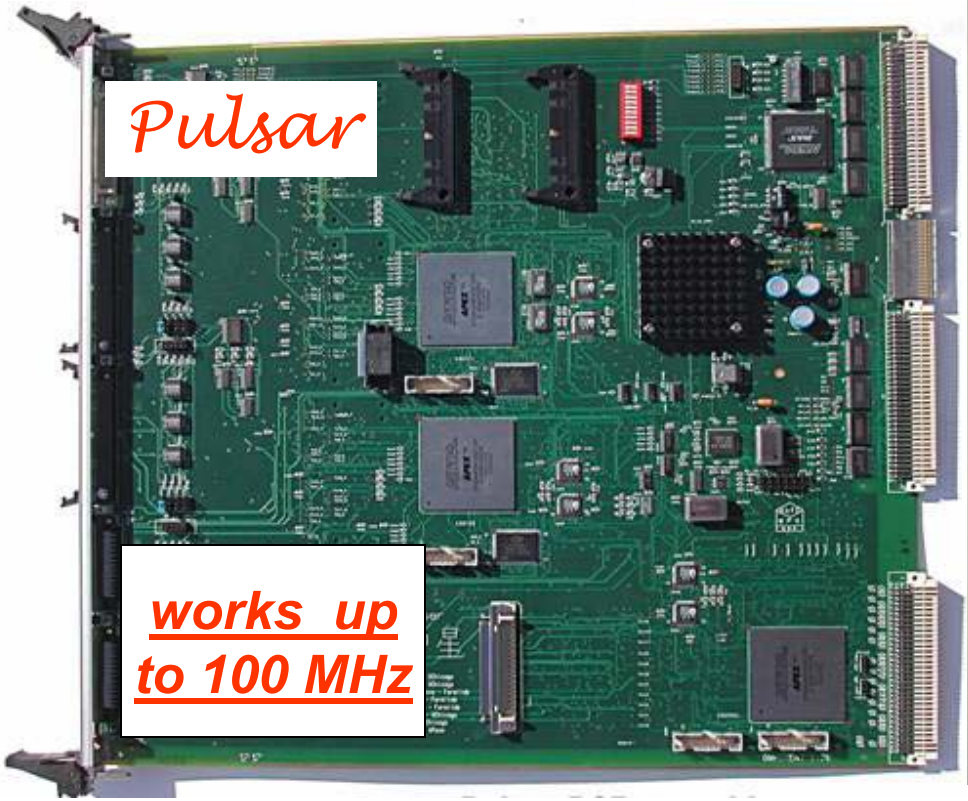


It took 1.5 GB memory on a 2GHz/2GB modern PC to simulate 9 boards together at the same time

Pulsar Board







4 types of custom mezzanine cards (Tx/Rx)

Design& Verifications: ~ 3 people in ~ 9 months

Initial checkout ALL interfaces: ~ 2 people in ~ 1 month

Benefits of Pulsar design methodology:

No blue wire on all prototypes

All prototypes became production boards

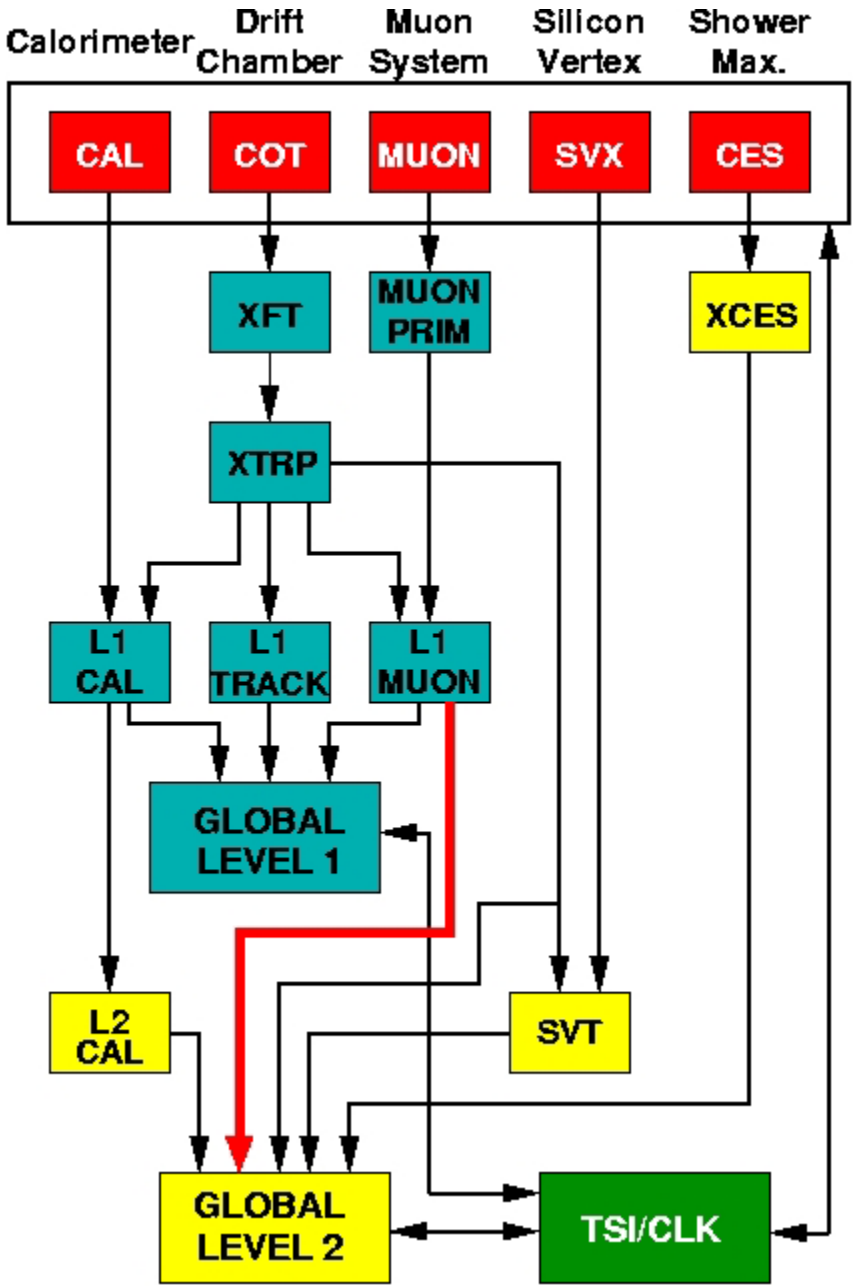
1st Application

L2 Muon Interface Board for CDF IIa

The Challenge:

- The CDF management requested to evaluate the application of a Pulsar board as an muon interface board for the current (RunIIa) system

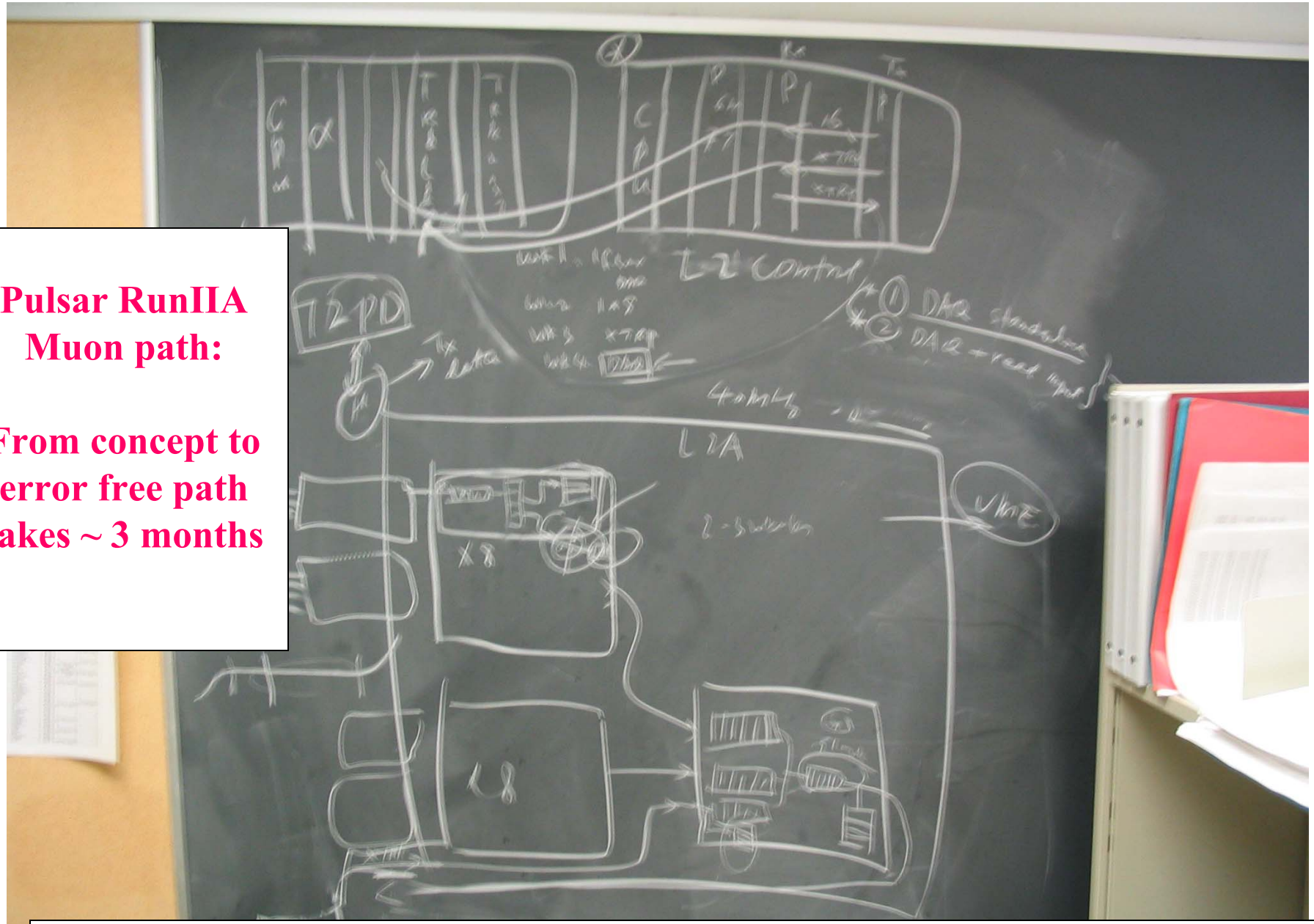
- Due to Pulsar's flexibility, this was possible …
- Pulsar is self-testable, it was possible to do it fast



June 2003: CDF Ops ordered us to "jump", we asked "how high?"

Pulsar RunIIA Muon path:

From concept to error free path takes ~ 3 months



CDF Ops office: discussion in June 03 about L2 Pulsar muon Path for RunIIA

RunIIa L2 Muon path commissioning: Pulsar methodology at work

upstream

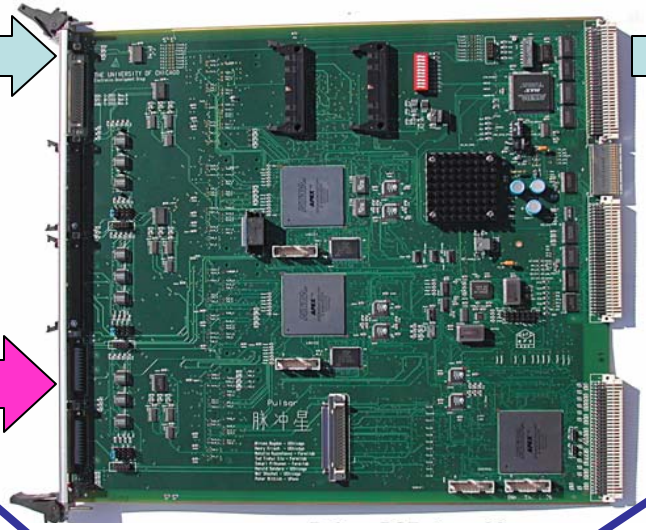
downstream

L1 Muon
(16 hotlink fibers)
and
Track data

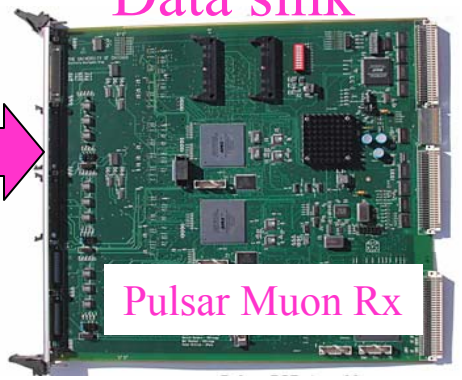
Pulsar Muon Board

Legacy
L2 decision
Crate
Track interface

Data source



Data sink



- **Fully self-tested before put in the running exp.**
  up to 1 Billions events in self-test mode.
- **The FULL chain test with beam worked on the first try (error free)**

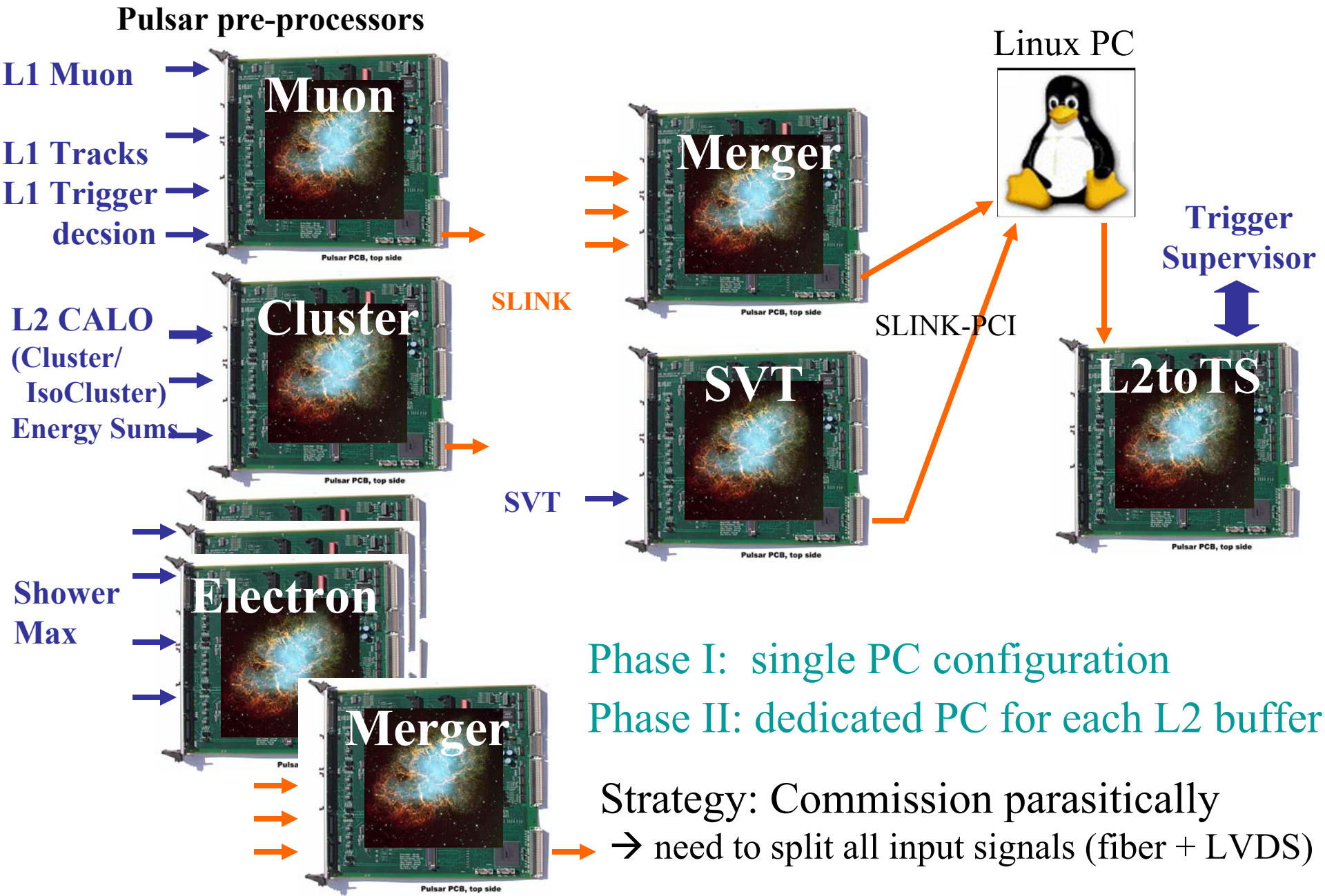
We didn't waste one second of beam time !

Successful application prototype & pre-production boards

Primary Application

CDF Level2 Trigger Upgrade

Level 2 Upgrade System configuration



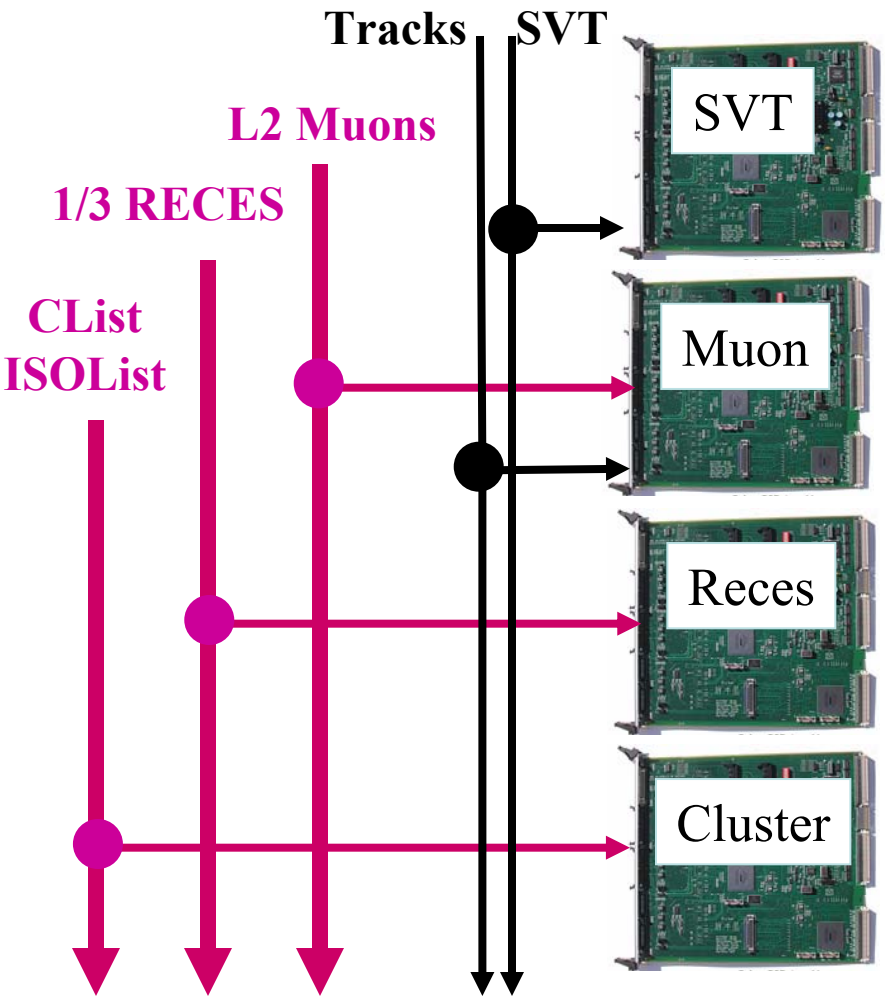
Phase I: single PC configuration

Phase II: dedicated PC for each L2 buffer

Strategy: Commission parasitically

→ need to split all input signals (fiber + LVDS)

A Parallel Universe for the Pulsar

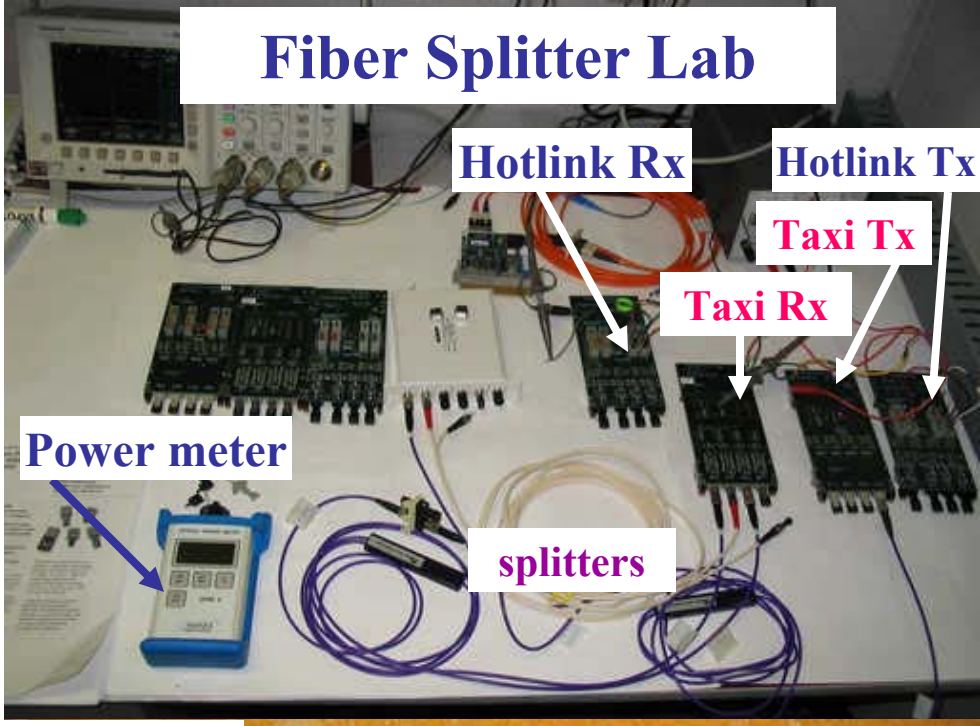


Legacy
Level 2 Decision Crate
α - Processor

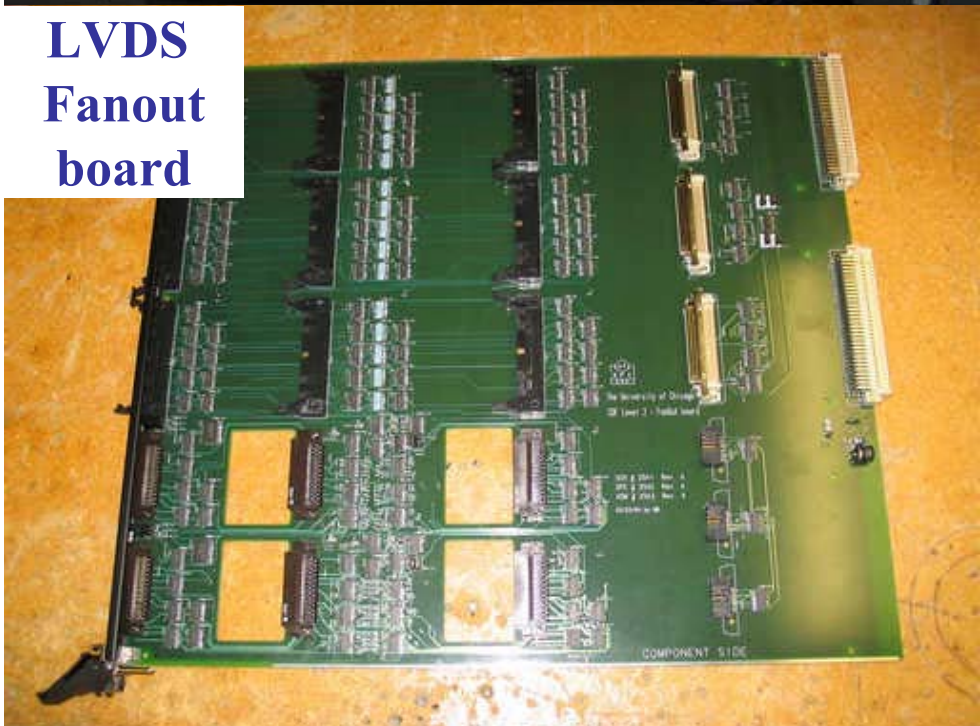
- Optical
- **LVDS**

Splitters

Fiber Splitter Lab

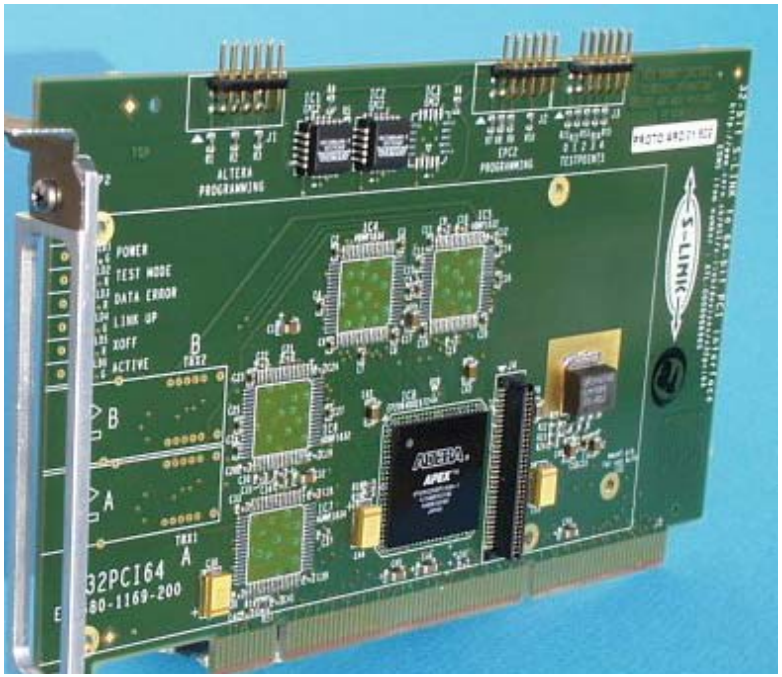


LVDS Fanout board



New 32-bit SLINK to 64 bit PCI interface card: S32PCI64 → developed at CERN

- highly autonomous data reception
- 32-bit SLINK, 64-bit PCI bus
- 33MHz and 66 MHz PCI clock speed
- up to 520MByte/s raw bandwidth



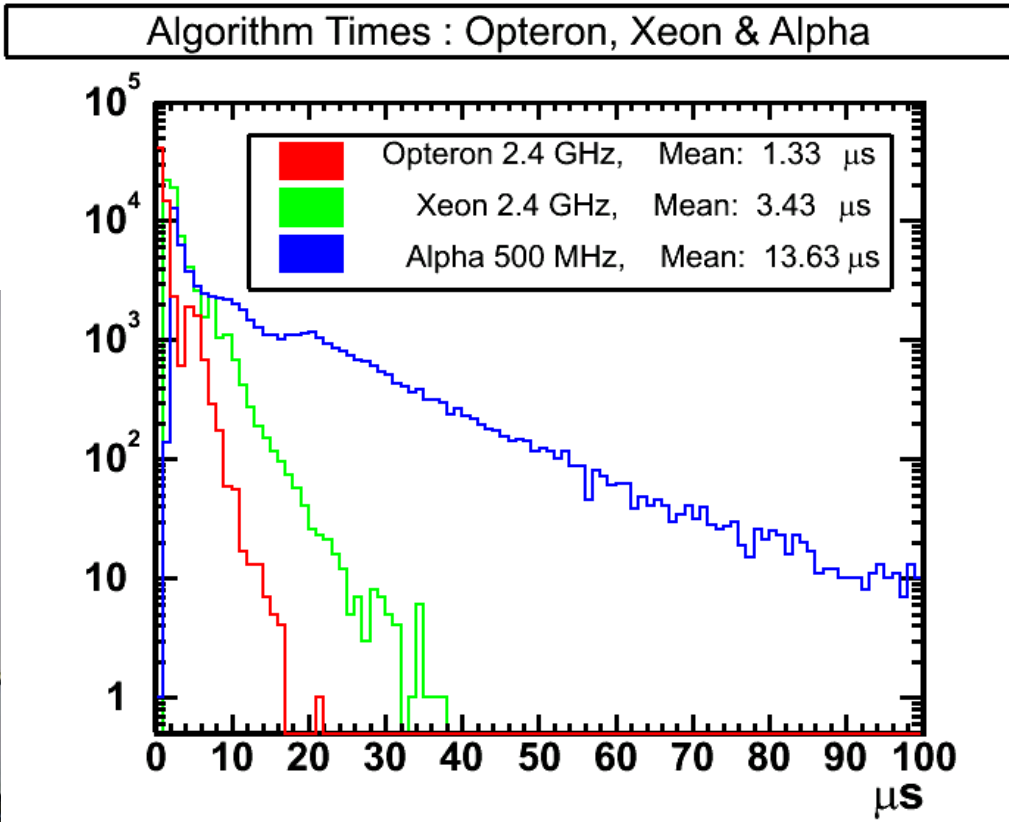
ATLAS SLINK data format

Beginning of Block control word
Start of Header Marker
Header Size
Format Version No.
Source Identifier
Level 1 ID
Bunch Crossing ID
Level 1 Trigger Type
Detector Event Type
Data or Status elements
Status or Data elements
Number of status elements
Number of data elements
Data/Status First Flag
End of Block control word

http://hsi.web.cern.ch/HSI/s-link/devices/s32pci64/

L2 Decision Processing Time Measurements

PC with 2.4GHz AMD Opteron (64bit) Processor fed by SLINK from Pulsar system



Level 2 Trigger algorithms run on real data in Run IIa system compared to Run IIb PC

Complete time including loading over S-Link/PCI and returning result <10μs

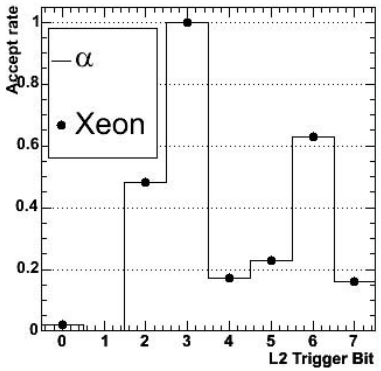
Beam Tests August 2004

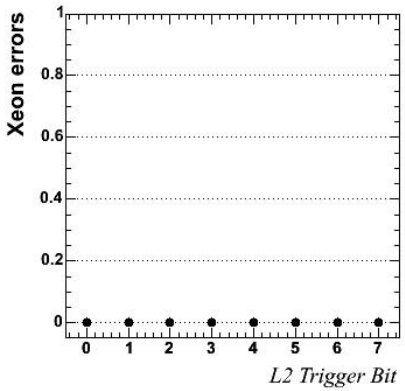
Test data taking with a subset of Triggers
(using Muon, Track and displaced Vertex)

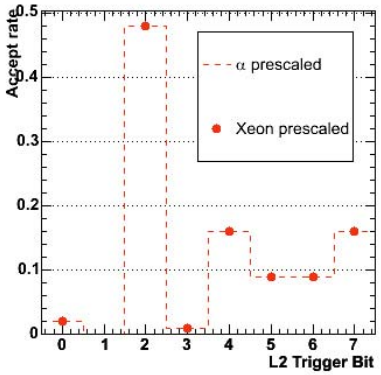
1) Legacy L2 making the decision
   Pulsar system running parasitically

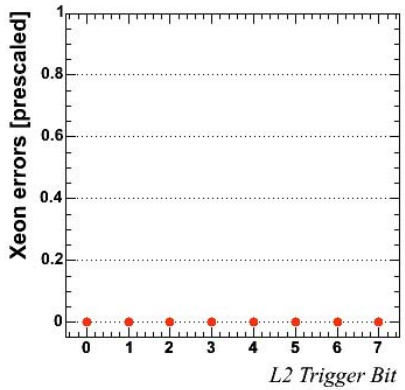
2) Pulsar making the decision

Perfect match of trigger decisions
Of both systems before and after
prescales

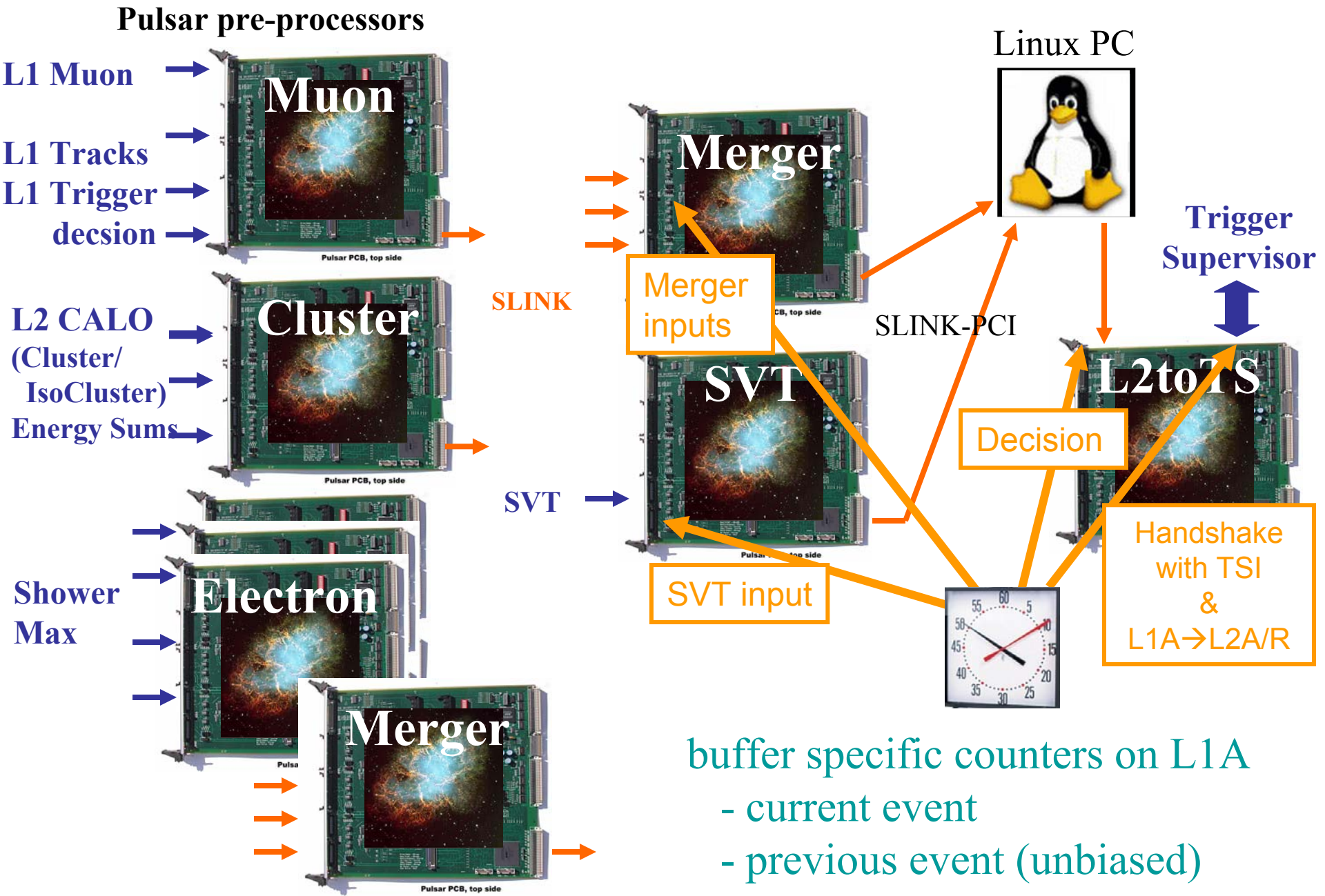






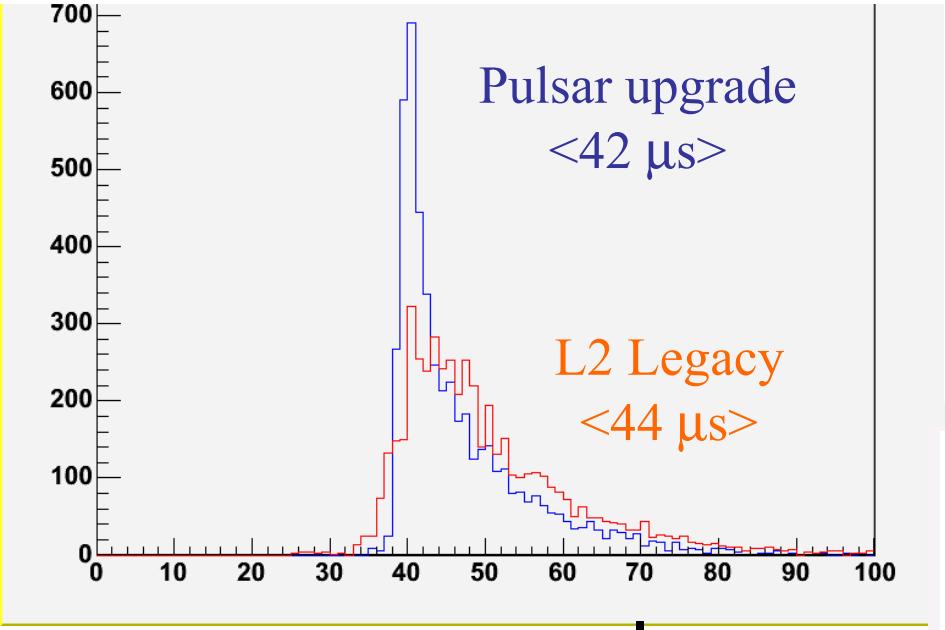


PULSAR System Timing Measurements



System timing measurements

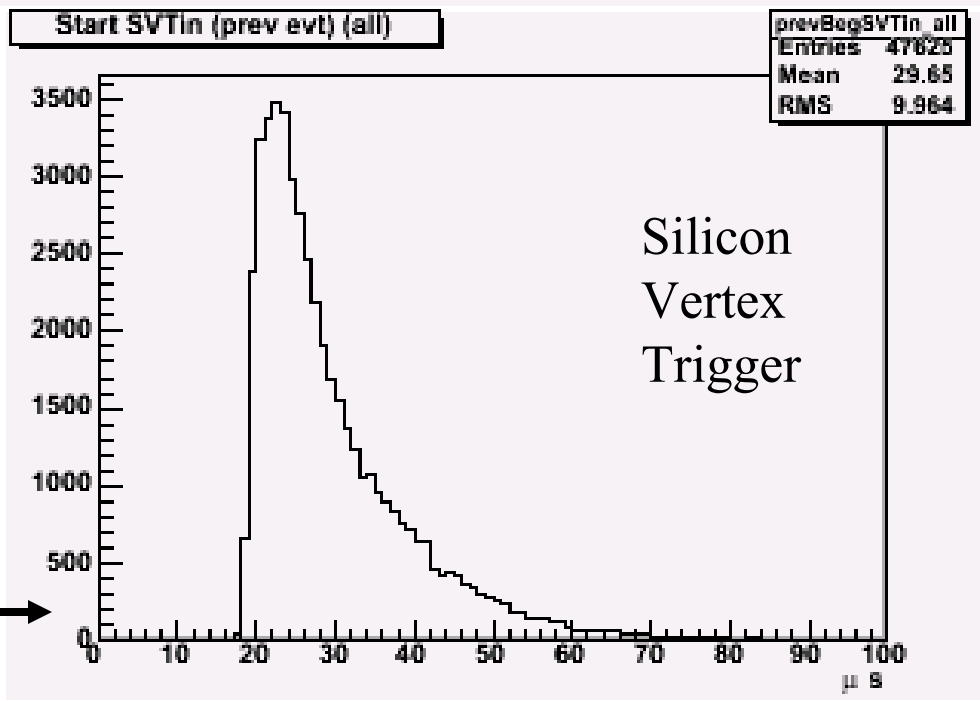
Overall L1A to L2 Decision latency



New system (not optimized)
already as fast as CDF Legacy Level2

More detailed timing measurements
Provide guideline for optimization.

Tail due to
Silicon Vertex Trigger
processing time

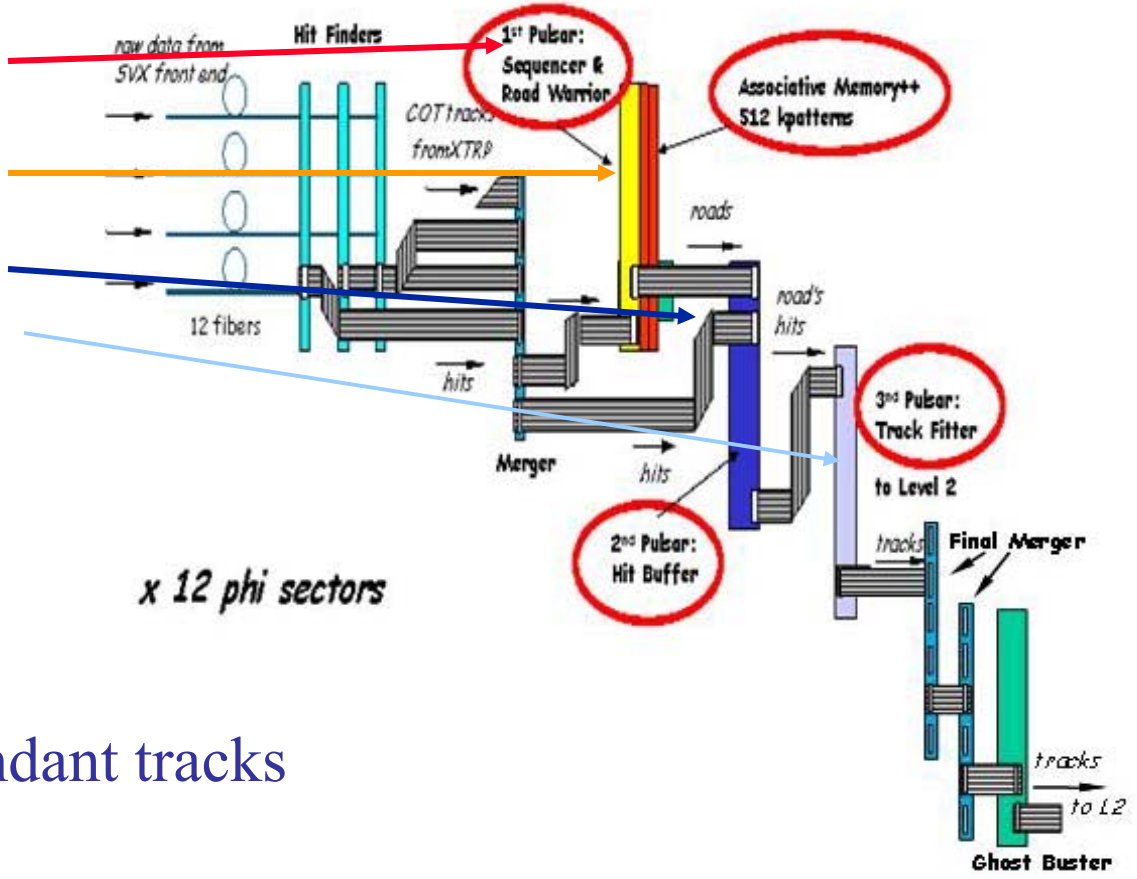


Silicon Vertex Trigger Upgrade

Goal: reduce SVT processing time

- reduce number of tracks to fit → narrow roads
- reduce time spent on track fitting

- new road pattern memory boards
- replace 3 custom boards by Pulsar boards with memory mezzanine cards



Aim: complete upgrade by end of next year

First part, eliminating redundant tracks already implemented

Summary: CDF Level 2 Trigger Upgrade The Pulsar Project

- ***Uniform & modular & flexible***

  Lego-style, general purpose design, backward & forward compatible.
  Many applications within & outside CDF:
  Plan to replace/upgrade > 10 different types of CDF trigger board
  Compatible with S-LINK standard → commodity processors …

- ***Design & verification methodology***

  simulation & simulation: single/multi-board/trace & cross talk analysis …
  → no single design or layout error (blue wire) on all prototypes

- ***Testability & commissioning strategy***

  Board & system level self-testability fully integrated in the design,
  Suitable to develop and tune an upgrade system in stand-alone mode
  Minimize impact on running experiment during commissioning phase

- ***Application of S-LINK at Hadron Collider***

  experience gained transferable to *and from* LHC community…

For more information see:
http://hep.uchicago.edu/~thliu/projects/Pulsar/