

# ALICE Trigger System

Features Overall layout Central Trigger Processor Local Trigger Unit Software Current status

On behalf of ALICE collaboration: D. Evans, S. Fedor, G.T. Jones, P. Jovanovic,

- A. Jusko, I. Kralik, R. Lietava, L. Sandor, J. Urban,
- O. Villalobos-Baillie

Anton Jusko, University of Birmingham

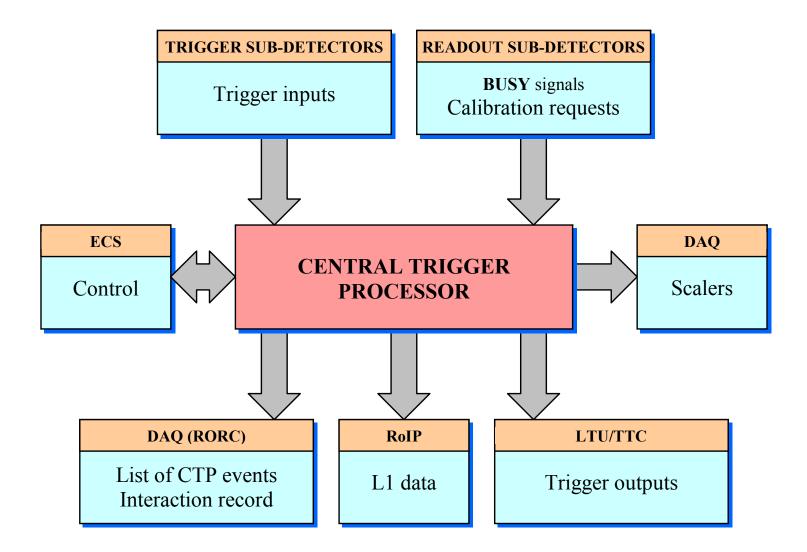
LECC 2004, Boston



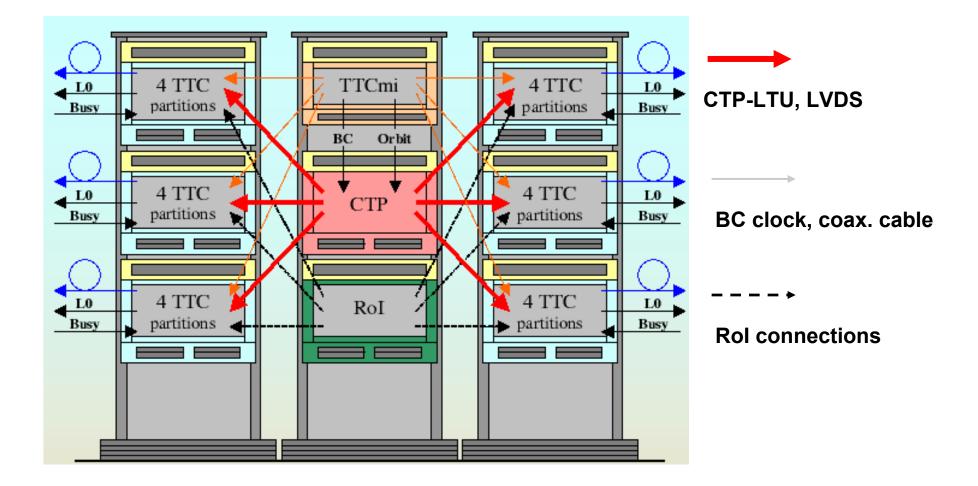
### Features

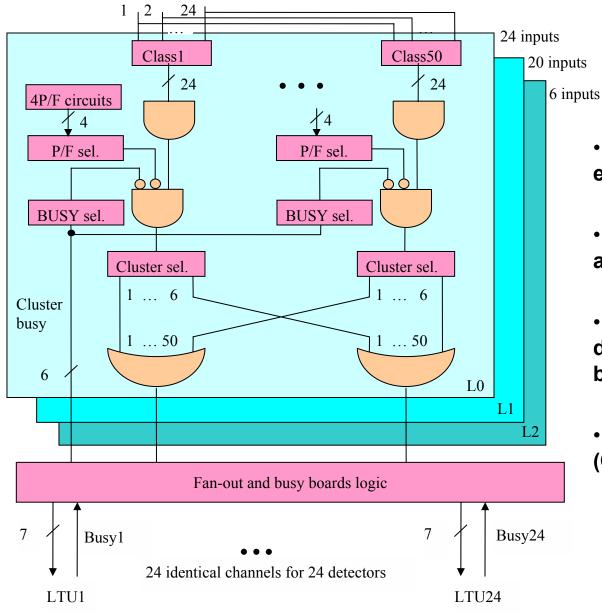
- 3 decision levels:  $L0: 1.2 \ \mu s$ ,  $L1: 6.5 \ \mu s$ ,  $L2: 88 \ \mu s$
- **Parallel decisions** at each level –different groups of detectors (clusters) are reading out different events at the same time
- All the readout detectors (max. 24) are partitioned in up to 6 dynamically partitioned independent detector clusters
- **4 past/future** protection circuits for each decision level shared among all detectors, which protects the system against pile-up
- **50 trigger classes** (combination of input signals and trigger vetos) for each level
- 24 L0 trigger inputs
- 20 L1 trigger inputs
- 6 L2 trigger inputs

## Overall layout



#### Connections





# CTP logic

- 50 programmable trigger classes for each level (AND of trigger inputs)
- past/future protection circuits shared among all classes
- BUSY veto replaced by delayed decision from previous level on L1, L2 boards
- On the output, classes are combined (OR) to detector clusters

# CTP partitioning

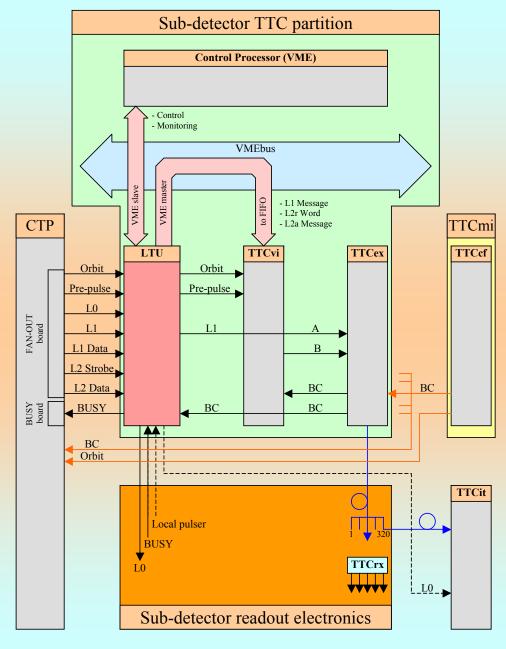
- 11 6U VME boards connected by special backplane
- 6 passive fan-in boards of
   6U VME size (not shown on the picture) for:
  - L0 inputs (2)
  - L1 inputs (2)
  - BUSY inputs (2)

BUSY	LO	L1	L2	FO	FO	FO	FO	FO	FO	INT
Cluster BUSY VME 0 0 0 0 0 0 0 1 0 0 0 0 0 1 0 0 0 1 0 0 0 1 0 0	Cluster L0 1 2 Cluster L0 4 5 6 C T T	Cluster L1 1 2 3 4 5 6 0 T T	Cluster L2a C Cluster L2a C 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	CTP outputs						
O BC Orbit	PPP	nputs		CTP outputs	Rol interface ScopeProbe					
ts BUSY inputs	puts L0 trigger inputs	puts L.1 trigger inputs	-inputs 	CTP outputs	DDL Rol					
BUSY inputs	Lo trigger inputs	L1 trigger inputs	P C I 12 trigger inputs	CTP outputs	11					

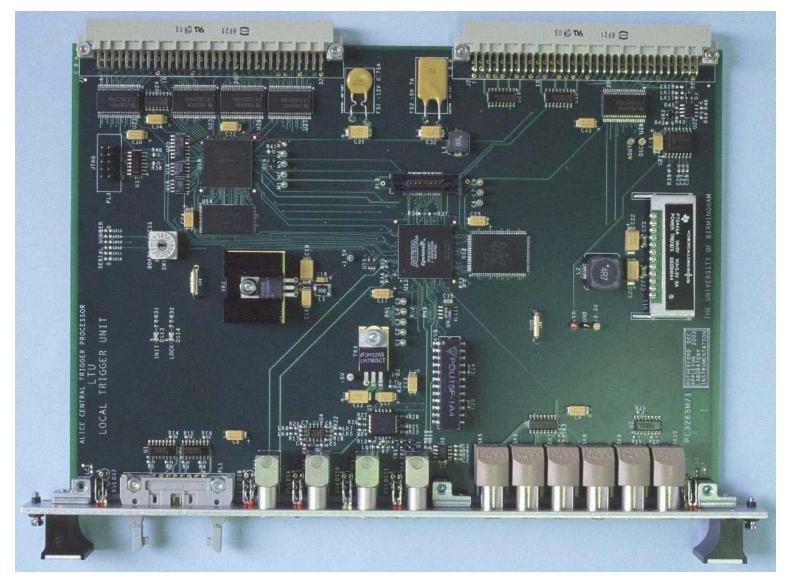
# Context diagram of LTU

- Up to 4 TTC partitions configured by 1 SBC in 1 crate
- TTC partition controlled by LTU through its VME master interface and I/O connections
- •GLOBAL (DAQ) mode: LTU is controlled by CTP
- •STANDALONE mode: LTU is controlled by on-board CTP emulator

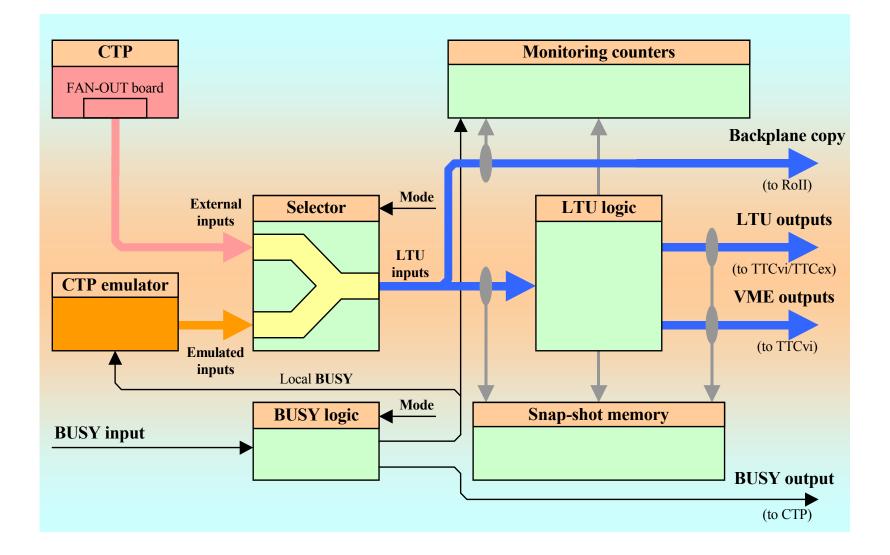
•The same front-end interface in both modes (L0, BUSY, FO)



### LTU board



## LTU block diagram

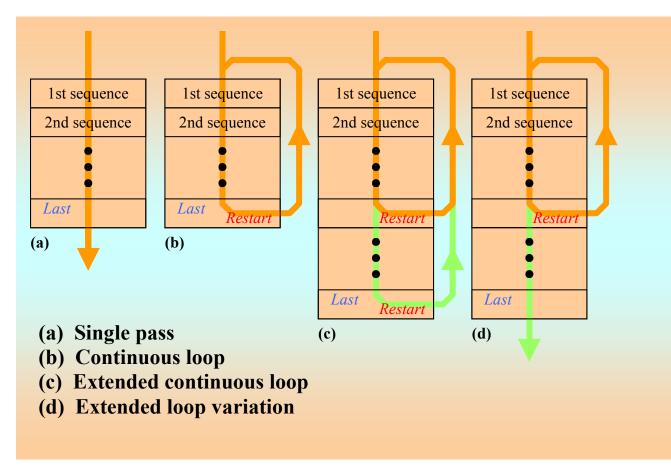


## **CTP** emulation

• Together with selector, it allows **STANDALONE** mode operation, presenting the same FE interface as in **GLOBAL** mode

- 7 legal sequences
- Programs of max. 32 sequences are prepared in emulator memory. L1 and L2 data are fully programmable
- Sequence execution triggered by **Start signal** derived from BC scaled down, random generator, external pulser or software request
- Error prone flag enables programmable random or 'on demand' errors with chosen sequences in order to allow the FE electronics testing for error recovery

## LTU sequences



```
Possible sequences:

L0

L0 - L1 - L2a (DAQ)

L0 - L1 - L2r

PP

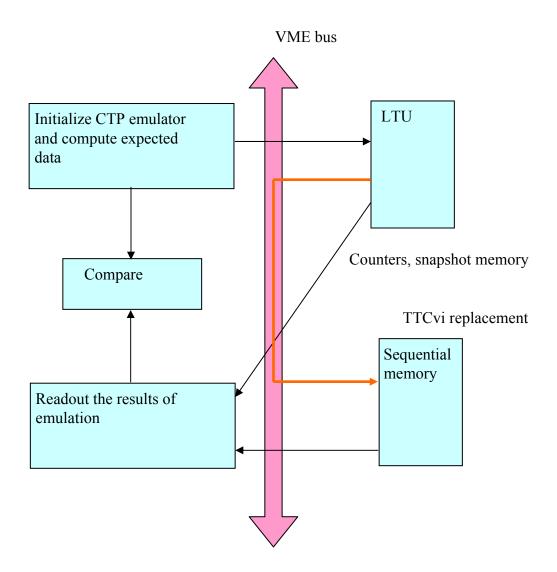
PP - L0

PP - L0 - L1 - L2a

PP - L0 - L1 - L2a
```

Errorneous sequences: L0 -  $\bowtie$  - L2a PP - L0 -  $\bowtie$  - L2r

## LTU testing, just completed



•<u>I/O tests</u> –front panel conectors, backplane connector - I2C bus and Roll connections

•<u>Functional tests</u> with CTP emulator, the TTCvi was replaced by VME board with large sequential memory where data sent to B-channel of TTC were caught

## LTU software

The control software for the LTU is ready. It is a subset of the software prepared during LTU development and testing. It is written in **Python/Tkinter** and **Tcl/Tk** (**GUI**) and **C** (**VME interface**).

Platforms:

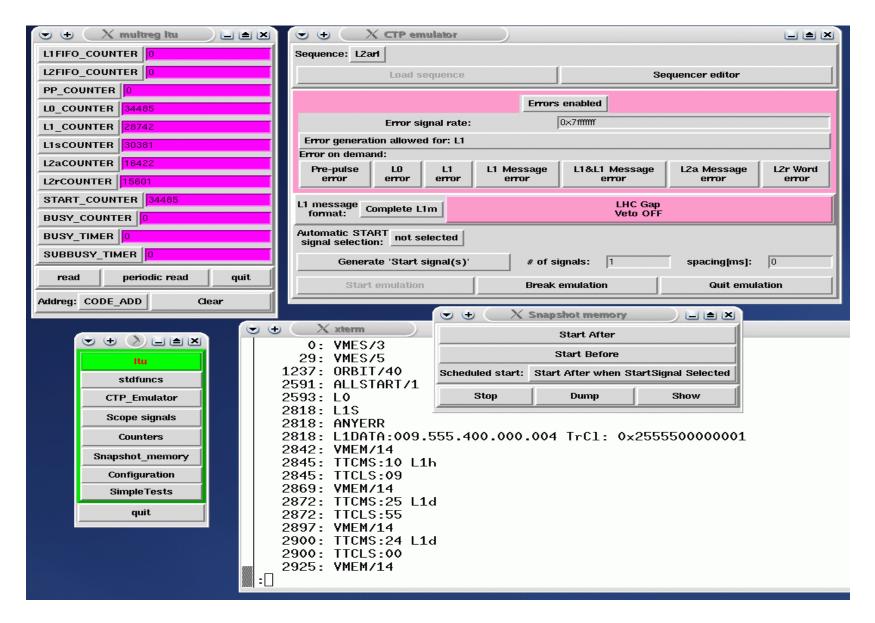
- VME SBC CCTVP110, Linux/VMERCC or CCT driver
- VME SBC Motorola, AIX

-PC + NI VME MXI cards with Windows/VISA possible

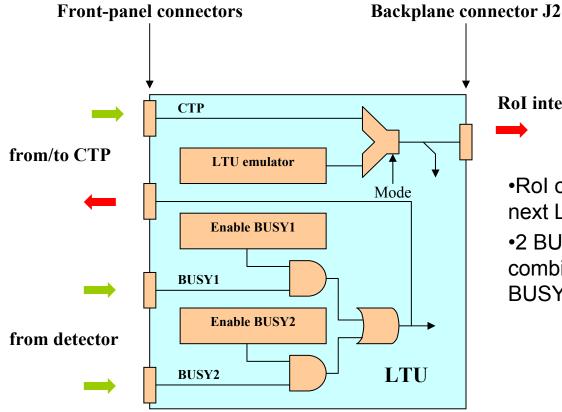
In addition to LTU control, SW supplies GUI for limited TTCvi control.

The same SW framework will be used with CTP boards

#### LTU software -example



# Testbeam setup Simplified block-diagram of LTU



**RoI** interface

•Rol output signals are used for feeding of the next LTU

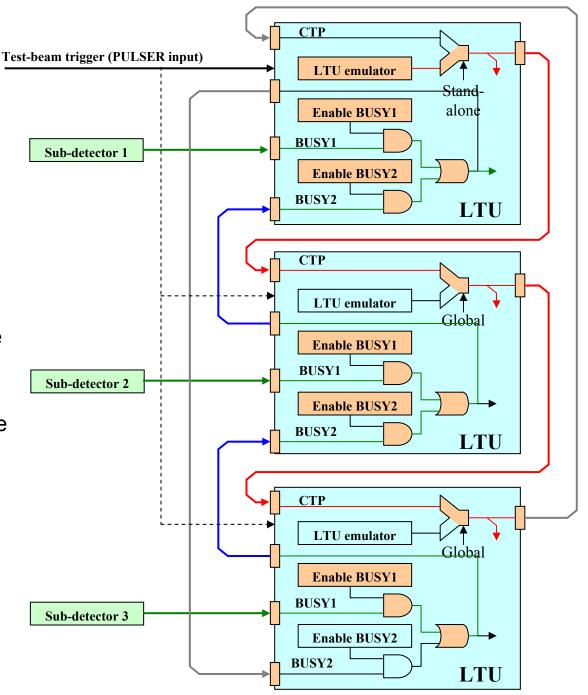
•2 BUSY inputs of 1 LTU can be used to combine BUSY from 2 detectors (common BUSY)

## Testbeam setup

• Thanks to programmability of busy logic and LTU Mode, any LTU can become Master (CTP emulator) by simple reprogramming of LTUs

• If trigger is connected to all the LTUs, the exclusion of any detector is possible without recabling

• Advantage: all the three LTUs operate together, without aditional hardware.



#### Current status

• 53 LTUs manufactured and tested, prepared to be used for tests with front-end electronics

- 3 LTUs are going to be used together in October combined Inner Tracking Subsystem test
- The ALICE CTP is being developed, first set of boards expected at the beginning of next year