A flexible stand-alone testbench for facilitating system tests of the CMS Preshower

<u>Paschalis Vichoudis^{1,2}</u>, Serge Reynaud¹, David Barney¹, Wojciech Bialas¹, Apollo Go³, Georgios Sidiropoulos², Yves Beaumont¹, Jacques Domeniconi¹

¹CERN, 1211 Geneva 23, Switzerland; ² University of Ioannina, Ioannina, Greece; ³National Central University, Chung-Li, Taiwan; Paschalis.Vichoudis@cern.ch

Abstract

A flexible test system for evaluating the CMS Preshower [1] on-detector electronics (analogue and digital) has been built using off-the-shelf components. The system utilizes an FPGA and a microcontroller, and is controlled via a standard USB link by a PC running LabVIEW. The testbench emulates the full functionality of the CMS Timing, Trigger and Control (TTC) system [2], as well as the CMS Tracker front-end control system (FEC) [3] and provides an electrical and/or optical data acquisition system, without the need for VME electronics. The testbench will be the principle evaluation and production testing system for all Preshower on-detector electronic components/systems, and can be easily adapted for other CMS (and non-CMS) systems.

I. CMS PRESHOWER ON-DETECTOR ELECTRONICS

CMS Preshower front-end electronics are organized as an analogue pipeline, where events are stored on front-end chips, followed by an on-detector analogue to digital conversion stage and a non-zero-suppressed data transmission system to the counting room. The general architecture is shown in Fig.1.

The Preshower on-detector system is composed of:

- Analogue front-end ASICs, called PACE, that provide 32channel pre-amplification and shaping, DC-coupled to 32strip silicon sensors, as well as analogue pipelines for the detector signals. A sensor and associated electronics (plus support structure) forms a "micromodule" (Fig.2). There are ~4300 of these micromodules in the CMS Preshower.
- Digital front-end ASICs, called K-chips, that collect the digitized (by ADCs) data from a group of up to four PACE chips, and format the information in a way suitable for serial transmission via gigabit optical hybrids (GOH) to the counting room.
- Front-end control ASICs (CCU, PLL etc) used for distributing fast timing control signals to the front-end readout ASICs as well as for providing system monitoring and control capabilities.
- 4. 40MHz bi-directional digital optical hybrids (DOH) used to deliver the fast timing signals (clock, trigger, reset, etc) to the embedded electronics and also to relay control and status information between the embedded electronics and the electronics in the counting room [4].

The Preshower on-detector system board contains the electronics necessary (items 2&3) to digitize and transmit the

signals from a number (7, 8 or 10) of micromodules. The first prototype of the system board is shown in Figure 3.







Figure 2: Photograph of a prototype micromodule



Figure 3: Photograph of the first prototype of the CMS Preshower on-detector system board with two PACE hybrids attached.

II. TESTBENCH

A. Motivation

The motivation for the development of this testbench was the need for a stand-alone evaluation system for all the Preshower on-detector electronic components/systems able to generate timing, trigger and control signals, as well as to readout data. Since multiple copies of the testbench are to be produced (for different laboratories, beam tests etc.), no "crate" electronics should be designed but only a selfcontained compact system requiring simply a PC for user interaction via a single link. A very important consideration for the system is the capability of optical interconnection with the components/ systems under test.

The testbench must include the functionality of simulating the LHC running conditions, in a similar way as in a previous test system developed for the design verification of the PACE chipset [5]. Therefore, the testbench must be capable of simulating the LHC running conditions (i.e. the 40.08 MHz clock and fast control signals). It must be able to send programmable bursts of triggers in order to test different functionalities and also to examine the response of Preshower front-end chips to various trigger rates – including pseudorandom triggers generated with an LHC-like Poisson distribution. In addition to the fast timing/trigger and control signals, slow control (setting the parameters of the front-end chips) must be incorporated and the system should also incorporate its own real-time DAQ system, with subsequent data output to a PC via a simple interface.

Finally, this testbench must be the principal production testing system for the evaluation of \sim 500 CMS Preshower ondetector system boards as well as \sim 4300 PACE hybrids.



Figure 4: Preshower's evaluation setup by using the testbench

B. Implementation

The testbench [7] is based around two principle components: an FPGA (Altera's Stratix GX EP1SGX10C [8]) and a microcontroller (Renesas's M16C [9]).

The principle characteristics of the FPGA are:

- 4 embedded gigabit deserializers
- 900K bits of RAM

- 10K logic elements
- 345 programmable I/O pins
- Multi-voltage I/O support (1.5V,1.8V,2.5V,3.3V)
- Differential I/O support (LVDS,LVPECL,CML)

The principle characteristics of the microcontroller are:

- 250K bytes FLASH RAM (for programs)
- 20K bytes RAM (for stack)
- 8 channels of 10-bit ADCs
- 2 channels of 8-bit DACs
- I²C interface
- 87 programmable I/O pins

The FPGA and the microcontroller are mounted on a custom-built PCB together with some auxiliary components. These include a 12-channel digital optical receiver (NGK's POR10M12SFP), a 4-channel digital optical transceiver (NGK's POX25B04SEJC), an additional single-channel optical transceiver (Agilent's HFCT-5911), an S-Link64 transmitter mezzanine card and a USB interface. Figure 5 shows a photograph of the testbench.



Figure 5: Photograph of the testbench

C. Features

The testbench emulates the full functionality of the CMS TTC system, including the generation of fully programmable bursts of up to 1000 triggers. The FPGA can be programmed to generate bursts of triggers by specifying the time between consecutive triggers expressed as a number of LHC-clock cycles (up to 65535), respecting the LHC triggering rules and trigger coding schemes (T1). Each of these so-called "triggers" is in fact a sequence of two commands¹:

- Calibration Pulse telling the PACE chipset to generate an internal electronic injection signal, sent to a selection of channels specified by the user
- LV1A sent <latency> clocks after Calibration pulse to tell PACE chipset to block a sequence of 3 columns in memory where the signal is being held.

¹ it is possible to mask one of the two commands, if necessary

The trigger bursts may appear in different ways depending on the internal triggering mode settings. They may occur either at a specified time after a ReSynch command, or "on demand" by the user. Indeed the ReSynch command may also be either single-shot or repeated, with a user-defined period. In addition, pseudo-random triggers can be generated with an LHC-like Poisson distribution.

The fast trigger and timing signals can be transmitted either electrically and/or optically. For optical transmission over a single fibre the fast trigger and timing signals are encoded by a 160.32 MBaud bi-phase mark encoder with time-division which multiplexes 2 channels using a balanced DC-free code. The system can also accept trigger and timing signals provided from external sources.

Another feature of the system is that it includes the functionality of the CMS Tracker FEC system for providing front-end control signals optically and/or electrically². In this way, the testbench is capable of controlling fully the Preshower on-detector electronics system without any additional hardware.

Four gigabit optical inputs are included for receiving data from optical transmitters (i.e. GOH), providing in this way a mini data acquisition system. The POR10M12SFP optical receiver that it is used for this purpose has been specified as the component that will also be used for the CMS ECAL data acquisition boards. Data from the board are either buffered and transmitted to a PC via a standard USB interface, or transmitted in real-time via an on-board S-Link [10] interface³.

From the programmer's point of view, a large part of the flexibility of the system comes from the rather low-level tasks⁴ programmed into the M16C. By using these tasks, the user is able to set all the desired parameters of the testbench. Essentially, the user sends a command to the M16C from the PC (via USB) in the form of a text string. The format of the text string is:

z<task ID><number of bytes><other parameters>⁵

These text commands can either be sent by using a graphical user interface or even directly from a terminal window⁶.

III. USER INTERFACE

The testbench comes with a LabVIEW user's interface developed specially for the Preshower on-detector components/systems needs. This application implements a number of Preshower-related procedures and is currently used for the design verification of the Preshower on-detector system board first prototype.



Figure 6: Front panel used to evaluate the CMS Preshower ondetector system board

For a more general purpose use of the testbench, an additional LabVIEW application is also available, giving the opportunity of using some of the testbench's features in a more general approach. It includes among others, a graphical display of the fast timing signals generated, in case that the internal triggering mode is selected. This LabVIEW application example can be easily adapted for other CMS (and non-CMS) systems, depending on the user needs.

It is worth mentioning that the LabVIEW applications developed for controlling the testbench are compatible with both Windows and Linux operating systems.



Figure 7: General purpose front panel used to control the testbench. The user can change the basic timing signals, mode of operation etc.

² FEC firmware/software was kindly provided by its authors in order to be included in the testbench.

³ in the case of S-Link transmission, an S-Link receiver board is necessary in the PC

⁴ This task-based protocol was firstly developed for the PACE test system

⁵ the parameters following the character "z" are expressed in hexadecimal format by using two ASCII characters each

⁶ The testbench under Windows operating system can be treated like a common RS232 device because of its USB interface device drivers that appear to the system as an extra serial port [11].

IV. PRESHOWER ELECTRONICS SYSTEM TESTING

The purpose of the first system tests was the design verification of the Preshower on-detector system, focused mainly on the basic in-system digital functionality and performance, as well as the tracing of possible interfacing or synchronization problems between the front-end chips, since all of the front-end chips have been already tested.

The verification of the on-detector system was done in two stages. In the first stage only the control chain, which consists of the previously mentioned front-end control ASICs, was involved. The testing procedure verified that the system was able to be reset, could receive/decode the multiplexed Clock+T1 signals and provide slow control signals on a full chain of 13 boards. For the second stage the data chain⁷ was added, comprising up to four PACE hybrids, followed by two bi-channel ADCs, a K-chip and a GOH. The verification procedure was done by sending calibration pulses to a number of PACE channels, reading out the digitized data formatted by the K-chip and reproducing the pulse shape generated by the PACE chipset using the three time samples taken (Fig. 8). The readout was done by de-serializing the serialized data that were transmitted optically by the GOH.



Figure 8: Reproduction of the pulse shape generated by the PACE chipset. The amplitude is expressed in ADC counts (~0.5mV) and the time in steps of 3.25ns.

In addition to design verification the testbench is currently used for measuring the noise performance and studying the grounding and shielding schemes of the Preshower ondetector system. Figure 9 shows a plot from noise measurements from PACE hybrids (no silicon sensor attached).

Another important test still to be done is the behaviour of the on-detector system under an LHC-like Poisson distributed high trigger rate (100kHz), where in this case the real-time data readout via the on-board S-Link64 transmitter mezzanine card is necessary.



Figure 9: Noise measurements. The horizontal axis indicates the multiplexed output of 32 channels x 3 time samples. The amplitude is expressed in ADC counts.

V. PRODUCTION TESTING OF SYSTEM BOARDS

On the basis of the measurements necessary for the design verification, a suitable for non-expert users systematic testing procedure, based on LabVIEW, is currently under development. For each Preshower on-detector system board, a bar code will be assigned, that will be used to create a directory on the PC and subsequent data files, in a similar way as in the PACE chipset test system [5]. The user is then taken through a series of tests, each of which produces a file in spreadsheet format and an indication as to whether the test was successful or not. Clearly during production testing if the result of any functionality test is bad, the remaining tests are skipped. Some of the tests performed systematically are:

- Verify that all the registers of the on-board chips (Kchip, DCU) are accessible
- Verify that there are no connectivity problems on the hybrid sockets⁸.
- Attach the PACE hybrids and verify that all the registers of each chip are accessible
- Verify that the fast commands are received properly
- Perform a number of calibration events, readout and reconstruct the pulse shape.

In the above mentioned tests, few of the tests performed for the PACE chipset production testing procedure [5] can be included, in order to verify that the PACE continues to function properly onto the PACE hybrids.

All the above tests will be done by using the testbench's electrical interfaces because the optical fibres are fragile and they are not recommended for the production environment.

A software interface is provided to the main construction database (CRISTAL2 [12]).

This production testing procedure based exclusively on the testbench will characterize ~500 CMS Preshower system boards as well as ~4300 PACE hybrids in Taiwan, Greece and CERN.

⁷ The first prototype of the CMS Preshower on-detector system board comprises two data chains

⁸ by using additional mezzanine cards plugged on the special general purpose sockets of the testbench

VI. OTHER USES OF THE TESTBENCH

In addition to the system and production testing procedures, the testbench will be used as the control and DAQ system during a beam test of a Preshower system board prototype in September 2004.

The DAQ component of the testbench is very similar, in both hardware and software, to that required for a CMS Preshower "Data Concentrator Card" (i.e. VME-based DAQ board). It would thus be expanded and used as the real CMS Preshower Data Concentrator Card, in the event that the development of such a board will be proven necessary.

It is important to mention that the flexibility of this system means that it could, in principle, be adapted in order to characterize/evaluate other CMS (and non-CMS) systems since it has the ability of providing all the necessary LHC-like trigger, timing and fast/slow control signals as well as to readout data, in a variety of interfaces (both optical and electrical). It would simply require some program adaptation and possibly a change in some connectors.

VII. SUMMARY

A flexible system using off-the-shelf components has been built for evaluating the CMS Preshower on-detector electronics. The motivation for the development of this testbench was the need for a stand-alone PC controlled evaluation system for all Preshower on-detector electronic components/systems that can generate timing, trigger and control signals, as well as to readout data. The board interfaces with the components/systems under test both optically and electrically.

The testbench will also be the principle production testing system for all Preshower on-detector electronic components/ systems. It will be used together with a systematic testing procedure software application based upon LabVIEW in order to characterize approximately ~500 CMS Preshower system boards as well as ~4300 PACE hybrids in Taiwan, Greece and CERN.

It is envisaged that the variety of controllable interfaces on the board (both optical and electrical), coupled with its flexible firmware, will be useful for evaluating or production testing of other detector electronics systems, for LHC and beyond.

VIII. REFERENCES

[1] P.Wertelaers *et al*, "*ECAL Preshower Engineering Design Review*", CMS ECAL EDR-4

https://edms.cern.ch/document/115565/1

[2] B.G.Taylor, *"Timing distribution at the LHC"* presented at the 8th Workshop on electronics for LHC, 2002. http://www.cern.ch/TTC/LECC02.pdf

[3] C.Ljuslin-C.Paillard, "FEC-Front End Control unit for embedded slow control draft 0.83"

[4] K.Kloukinas, "CMS Preshower front-end readout & control system, Version 0.2 draft"

http://cmsdoc.cern.ch/cms/ECAL/preshower/Documents/pres hower/Readout/CMS_Preshower_Readout_and_Control_Syst em_V0.2.pdf

[5] D.Barney et al, "A flexible stand-alone testbench for characterizing the front-end electronics for the CMS Preshower detector under LHC-like timing conditions" presented at the 8th Workshop on electronics for LHC, 2002. <u>http://lhc-electronicsworkshop.web.cern.ch/LHC-electronics-</u> workshop/2002/links/A64.pdf

[6] P.Aspell, "*The Design and Development of the Front-end Electronics for the CMS Preshower Detector*", PhD thesis <u>http://cmsdoc.cern.ch/cms/ECAL/preshower/Documents/preshower/PACEIIthesis.pdf</u>

[7] The schematics for the testbench may be found on https://edms.cern.ch/cedar/plsql/navigation.tree?top=1107553 635&only_doc=Y

[8] For details concerning the EP1SGX10C FPGA see <u>http://www.altera.com/products/devices/stratixgx/overview/sg</u> <u>x-overview.html</u>

[9] For details concerning the M16C microcontroller see http://www.renesas.com/fmwk.jsp?cnt=m16c_family_landing_isp&fp=/products/mpumcu/m16c_family/

[10] O.Boyle, R.McLaren & E.van der Bij, "The S-Link interface specification"

http://cmsdoc.cern.ch/cms/TRIDAS/horizontal/docs/s-link.pdf

[11] Future Technology Devices Intl. Ltd, "FTDI's VCP drivers for Windows" <u>http://www.ftdichip.com/FTWinDriver.htm</u>

[12] J-M. Le Goff et al, "Detector Construction Management and Quality Control: Establishing and Using a CRISTAL System", CMS Note-1998/033