The Muon Sorter in the CMS Drift Tubes Regional Trigger

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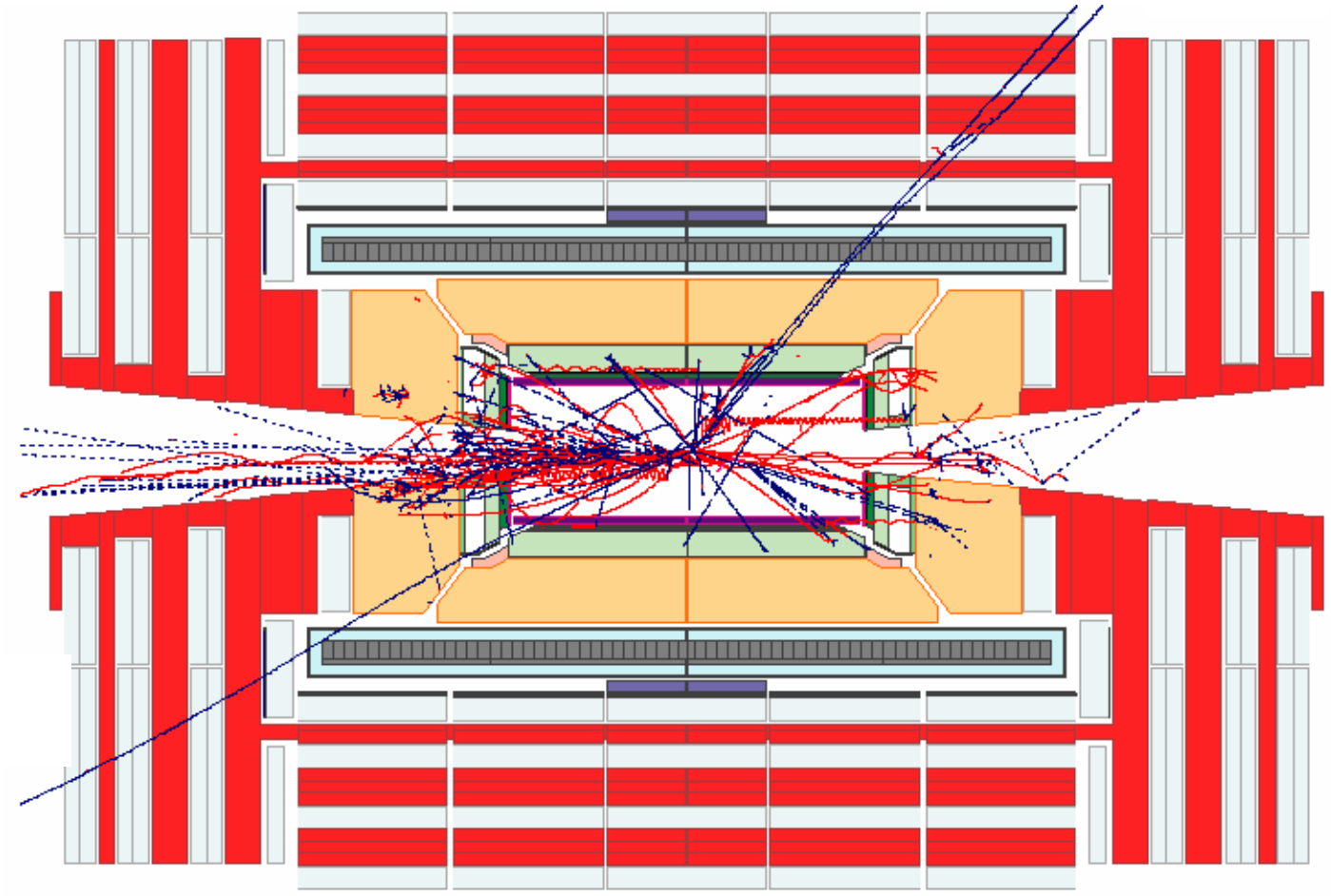
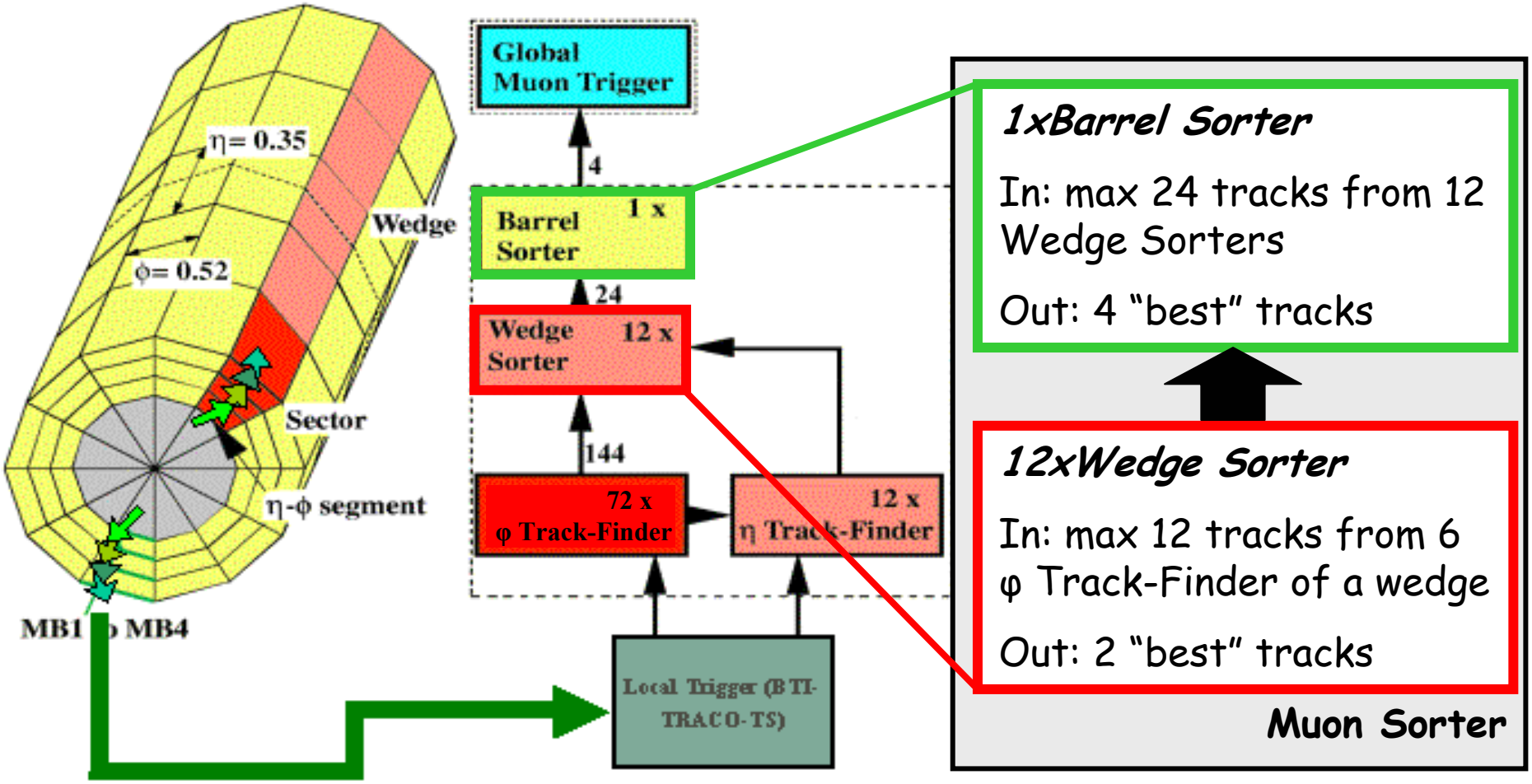
CMS Drift Tubes Detectors



DT Regional Trigger

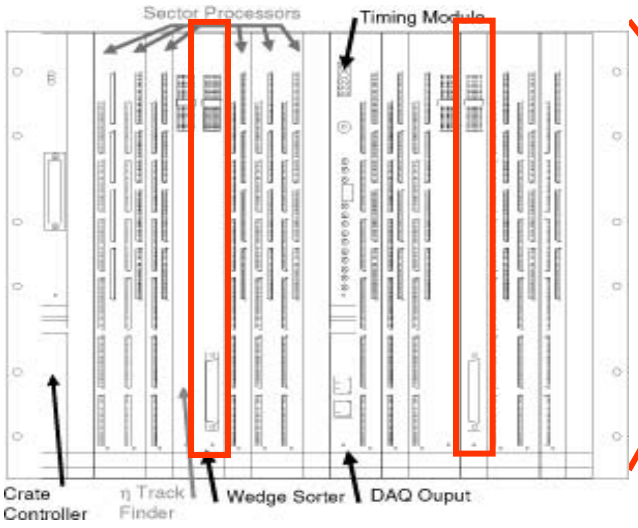


Hardware - location

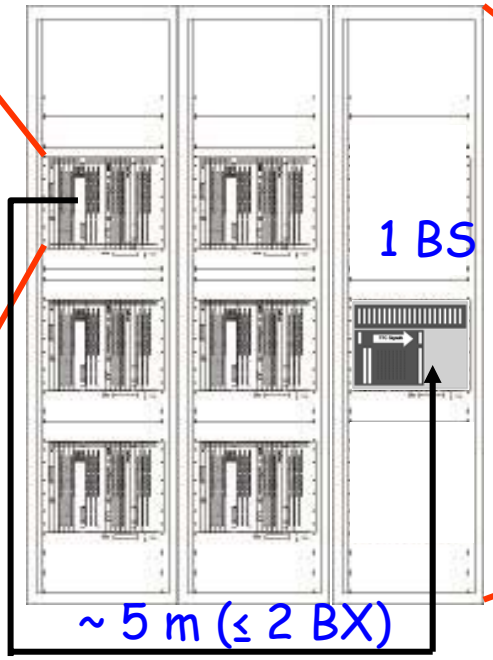
- DT Regional trigger racks in underground counting room USC55
- No radiation environment, easy maintenance access

  → Use of programmable devices
- 3 racks, with 6 crates for TF and WS, 1 crate for BS

  → All boards are VME-9U J1 + custom backplane, 400 mm depth

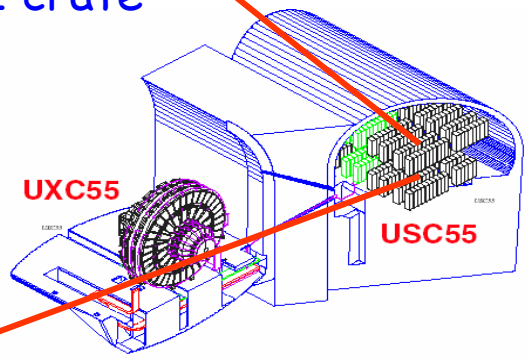


(2 WS / crate) x 6 crates



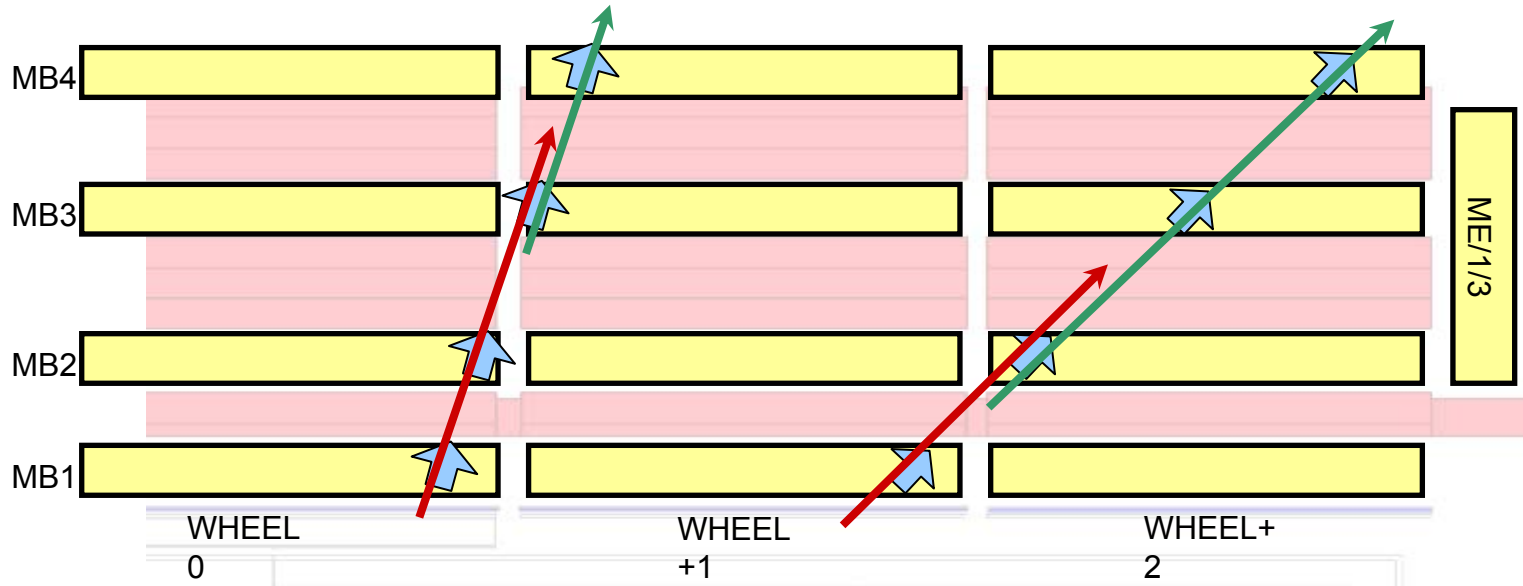
1 BS / 1 crate

~ 5 m (≤ 2 BX)



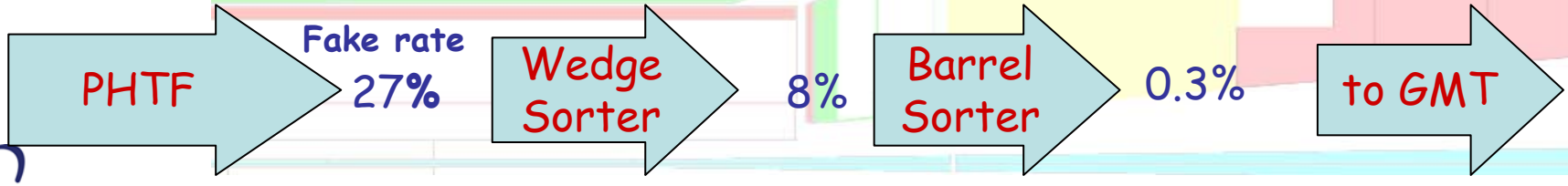
WS requirements: ghost busting

- Adiacent PHTFs can build the same muon track:



→ Single muon events can appear as dimuon events

- Goal: keep this fake rate below 1 % at Muon Sorter end
- WS compares the locations of track segments used by different PHTF, and the fake tracks found are cleared

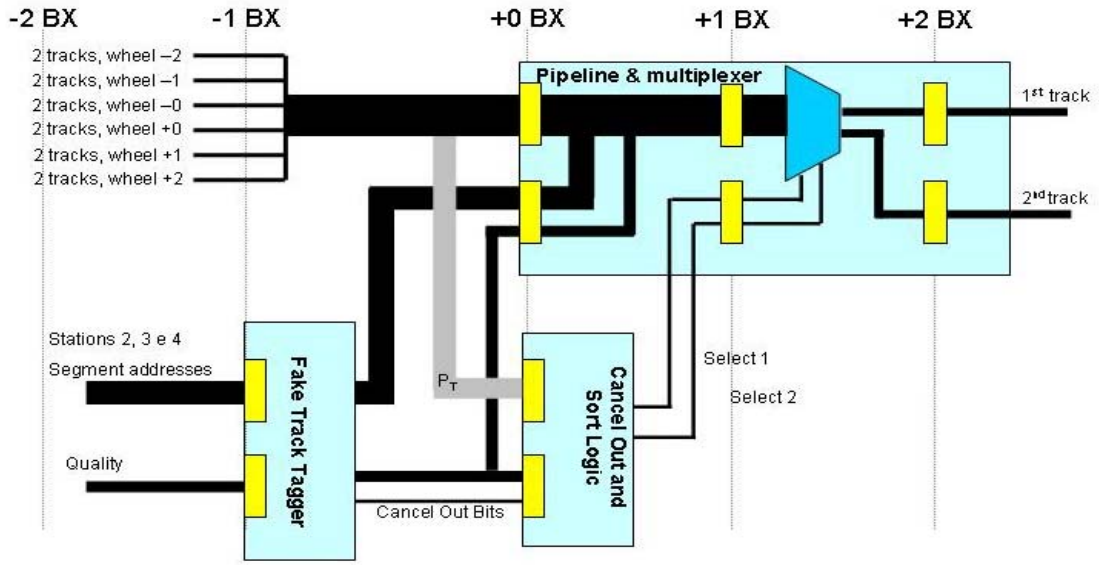


WS requirements: sorting

- Keep high efficiency on dimuon events:
  - Sort **2 out of 12** candidates from the wedge, in 2 BX
  - Sorting based on track quality (3 bits) and P_T (5 bits)

    → Rank based on **8 bits/track** → HEAVY TASK
- Full track information is 31 bits (qual, P_T, φ, η, q, address)

    → Algorithm uses about **450 I/Os** → LARGE DEVICE

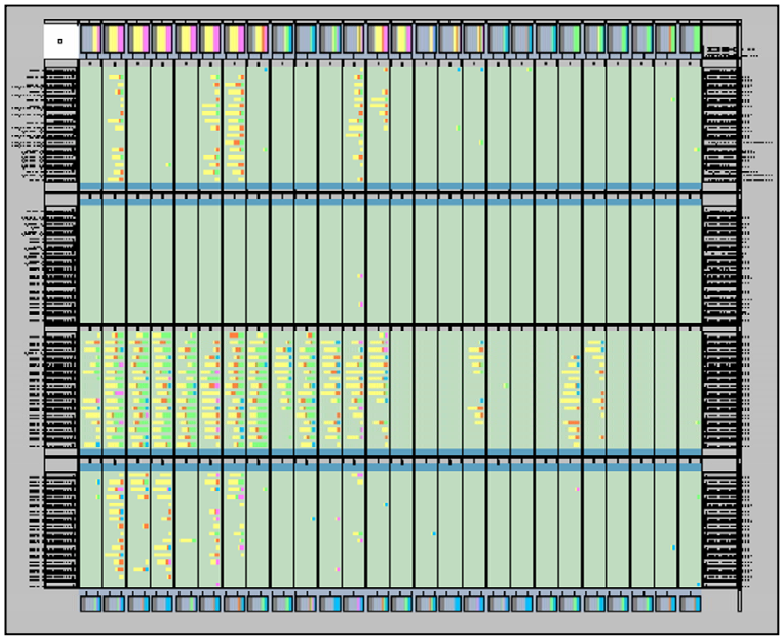


Wedge Sorter latency: 2 BX

WS main FPGA design

- Design is developed in VHDL
- Vendor dependent libraries usage is minimized, VHDL is synthetized on different vendors FPGAs
- Fit all logic on a single device if possible

After simulations → ALTERA APEX



-Design fits one APEX20K400 from Altera, 672 pins FineLineBGA

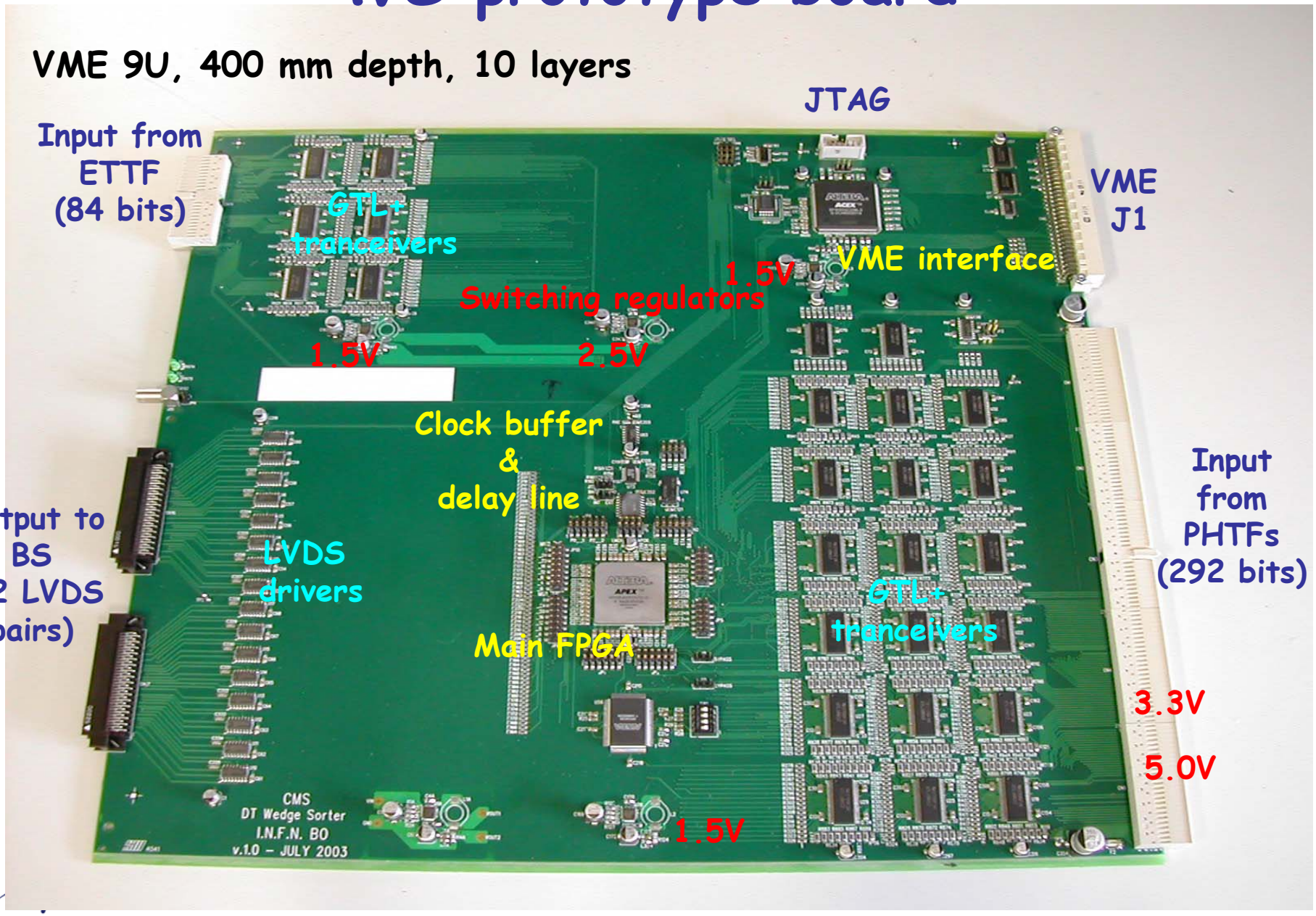
-The sorter core latency is about 21 ns

-The max operating frequency is about 48 MHz

-25 % of resources is used, about 100k equivalent logic gates

WS prototype board

VME 9U, 400 mm depth, 10 layers

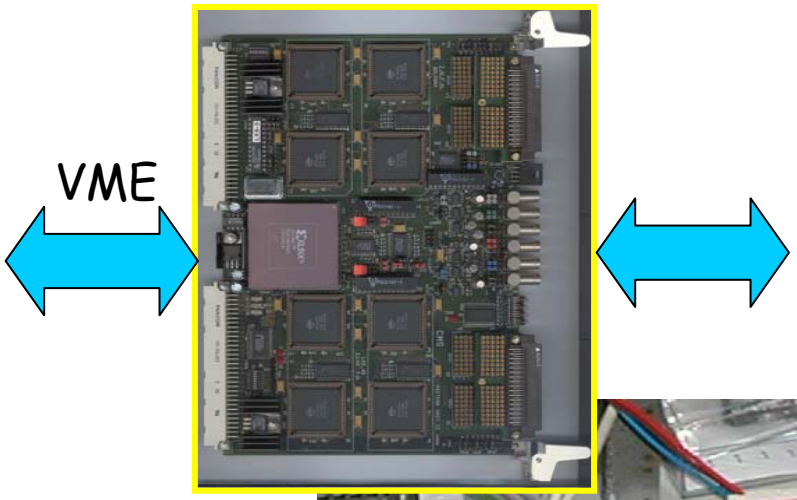


WS board features

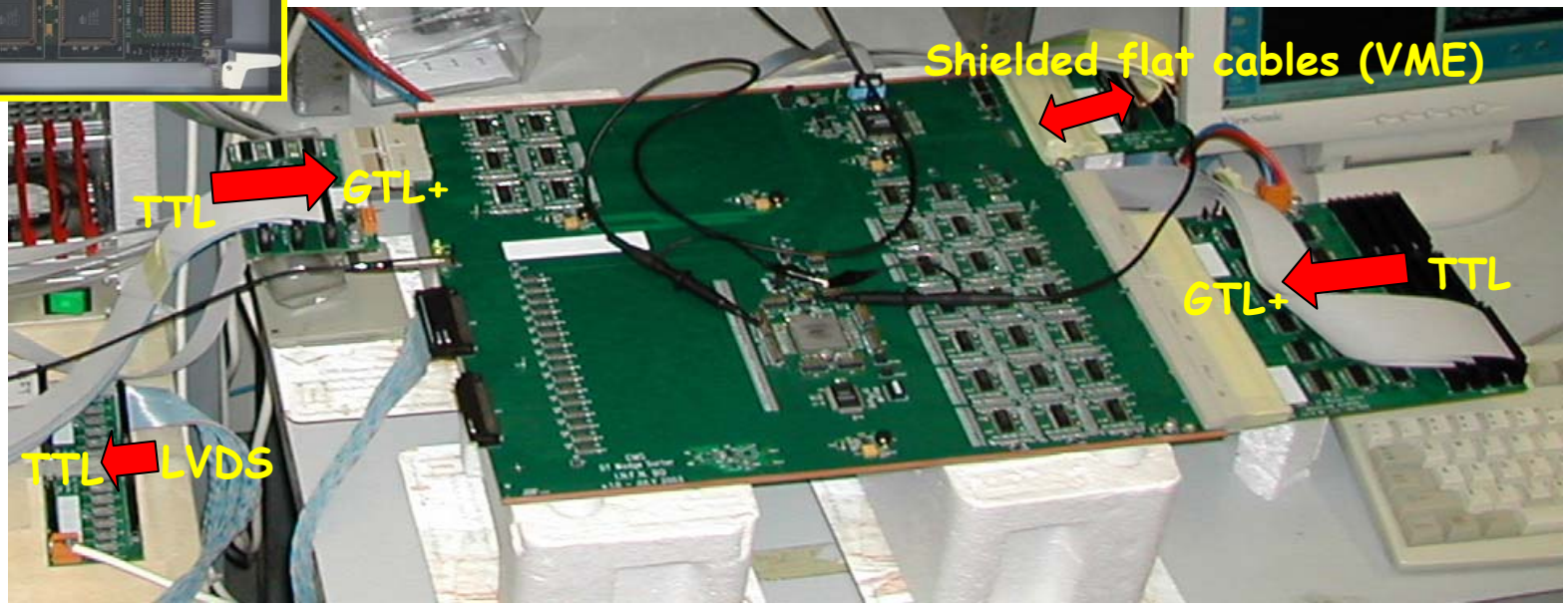
- Routing out of Apex20K in FineLineBGA675 package is optimized fixing pinout before synthesis of VHDL into device logic
- 3 clock sources (backplane, front panel, internal); phase adjust through VME
- JTAG chain through FPGAs and configuration device, for configuration and debugging; access through on-board connector or VME interface
- Private parallel and JTAG interfaces between main FPGA and VME chip
  - VME access to configuration, test and snap registers
- Series termination on all I/O and clock lines

WS test adapter boards

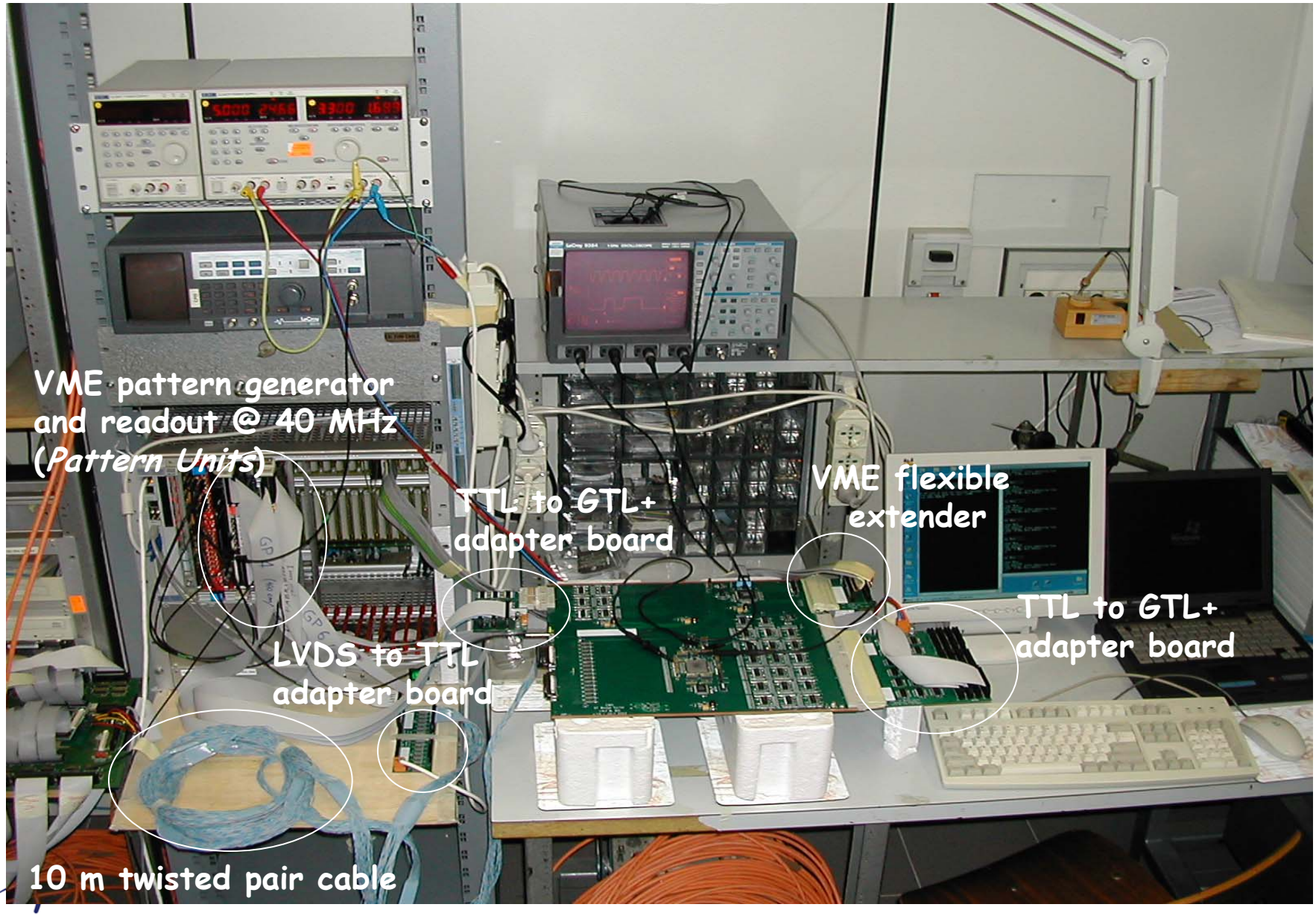
Adapter boards were designed to provide WS GTL+ input signals and and to read back LVDS outputs using general purpose I/O boards (**Pattern Units**)



TTL
128 I/O
up to 100 MHz

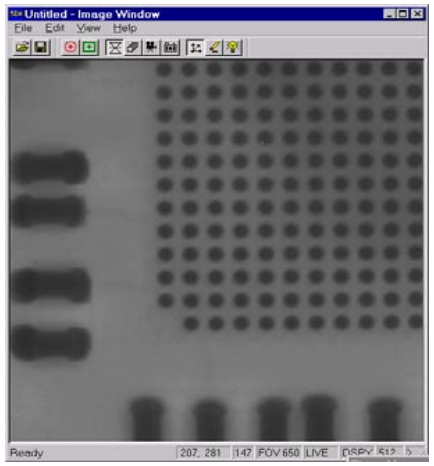


WS test setup

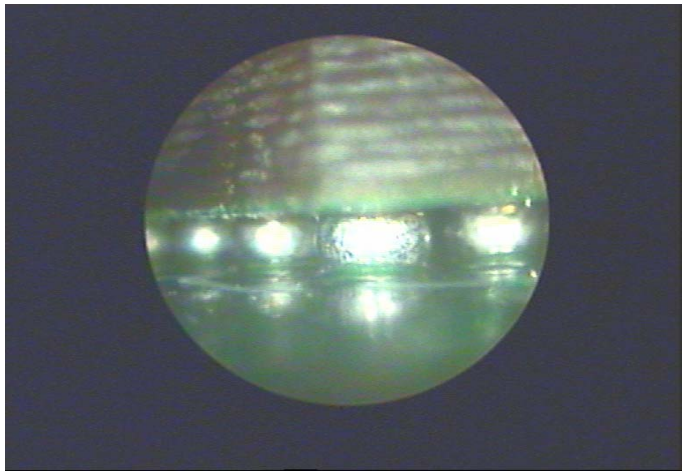


WS standalone static tests

- Switching voltage regulators are tuned, no noise on voltage levels
- JTAG programming of VME interface and main FPGA as a cycling multiplexer
- Access to VME chip with R/W operations
- Check of BGA chip soldering:
  - Set static patterns on WS inputs, read outputs and check
  - Cross check with JTAG sampling
    - × 15 unconnected pins on first prototype!

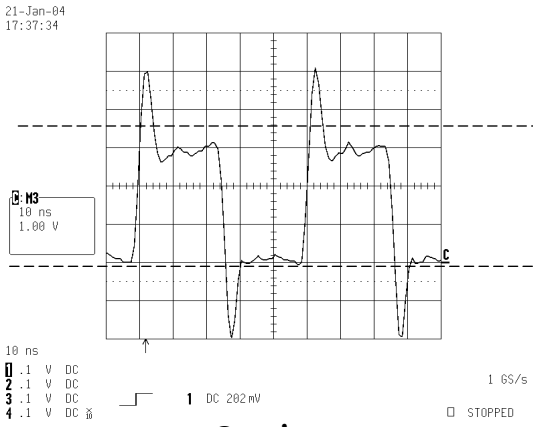


RX & microscope pictures to check FLBGA soldering

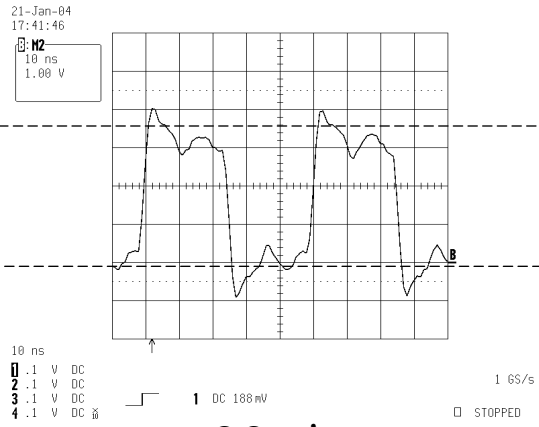


WS standalone dynamic tests

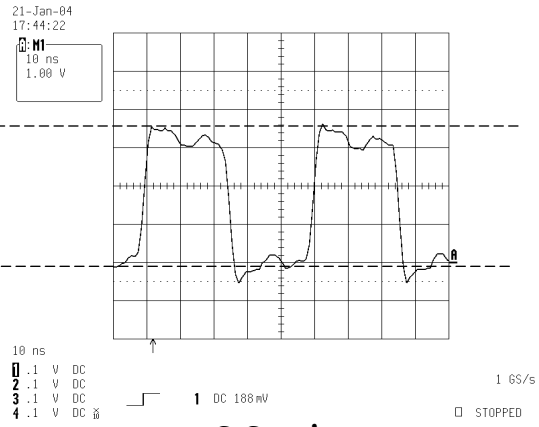
- Tune series resistors sampling signals waveforms at traces end:



0 ohm



22 ohm



33 ohm

- Measure timings and set clock phases windows
- Inject 40 MHz signals and read back after 10 m of LVDS cable transmission:
  checked to BER < 10^{-12}
- Check cross-talk among lines on board with several switching patterns: OK

✓ **Board validated, production with no modifications (tender phase)**

Barrel Sorter requirements and approach

TASKS: BS algorithm is similar to WS one BUT

- 24 input tracks → much bigger I/O (~ 870)
  → complex ghost busting
  → sorting 4 out of 24 (heavy task)

Design approach similar to WS

- All functionalities on one big FPGA
  - (Altera Stratix EP1S60/EP2S130, 1508 fBGA)
- 9U, 400 mm VME board
- Latency: 3 BX for ghost-busting + sorting&multiplexing

with some main different features

- Inputs from cable (LVDS) through connectors on board top
- Main FPGA on mezzanine board

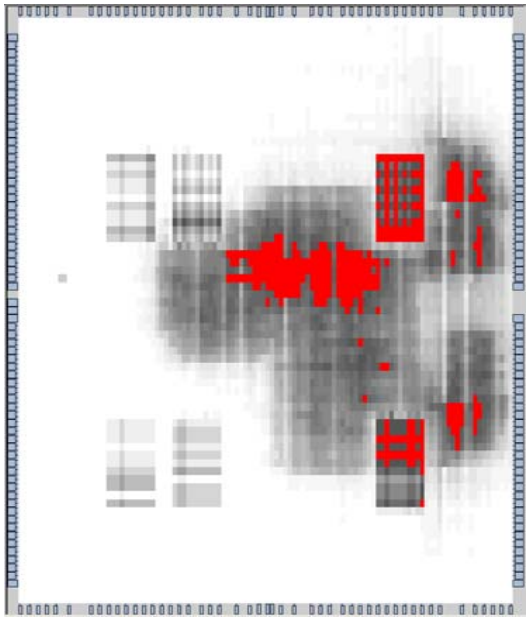
BS board layout

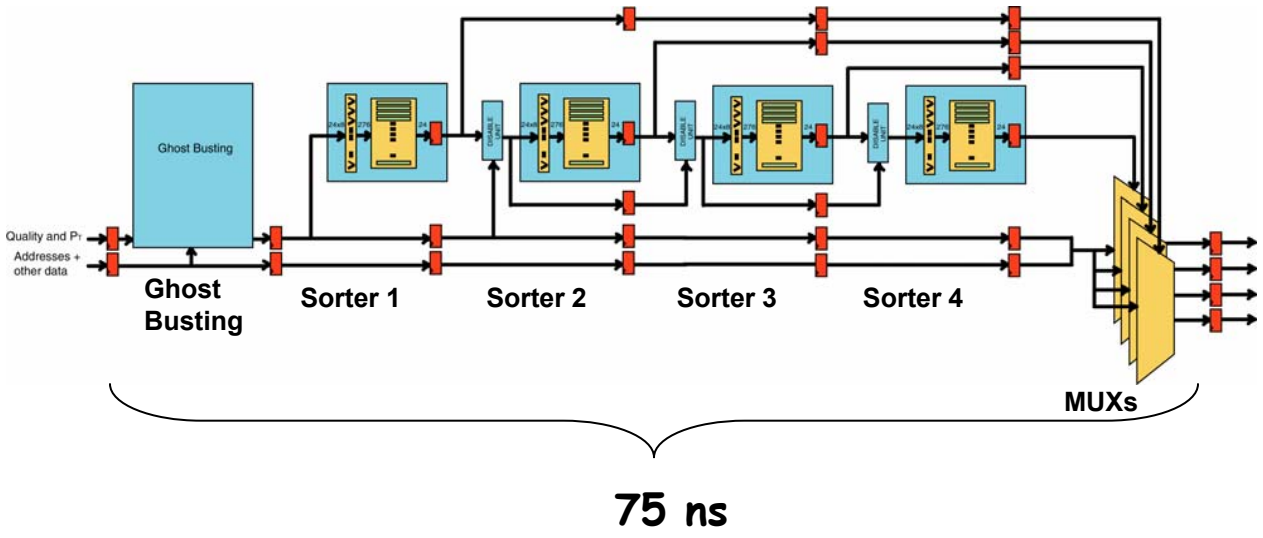
Barrel Sorter board layout (1:2) v7 - A.Montanari, 25-Aug-04

BS main chip design

- Notice that (sorting 4 out of 24) >> 2 x (sorting 2 out of 12) !!!
  - In the fully-parallel sorting algorithm used in WS, logic usage and routing congestion increase as very steep functions of the number of input words
- New FPGAs work better with fine segmented pipelines

✓BS uses sequentially 4 x 1-out-of-24 sorters in pipeline





Summary

- The Muon Sorter in Drift Tubes Regional Trigger selects and forwards to the Global Muon Trigger up to 4 muon per event

- Two boards, WS and BS, have to fulfil the requirements
  - Ghost suppression down to satisfactory low rate
  - Sorting of tracks within limited latency

- WS board prototype was designed, built and tested in 2003-2004
  - Design goals achieved with single big FPGA
  - The prototype worked well: exaustive stand-alone test & integrated test OK
    - ✓ Production in tender phase; boards delivery: exp. end of october
  - It will be used in the next test beam to acquire φ-TF data

- BS is being designed, relying in new FPGA tech. and new chip design strategy