# The Muon Sorter in the CMS Drift Tubes Regional Trigger

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### Abstract

Drift Tubes chambers were designed to be used in CMS trigger to allow muon tagging in the barrel of the detector [1]. Local Trigger logic reconstructs chamber-level track segments that are assembled into full tracks by the DT Track Finder in parallel over smaller sections of the barrel. In the final stage of the regional trigger the Muon Sorter has to select the best four candidates in the barrel and to filter fake muons generated by system redundancy. The hardware implementation of Muon Sorter satisfies large I/O and fast timing requirements using latest FPGA technology. The hardware was tested with custom facilities. Constraints, design implementation and test setup will be reported.

## I. DRIFT TUBES REGIONAL TRIGGER

## A. Regional Trigger partitioning

The arrangement of muon detectors determines the partition of trigger logic [2]. CMS Drift Tubes detectors [3] are arranged in *stations*. Each station is provided with Local Trigger logic that reconstructs track segments [4]. Dimensions and positioning of the stations are such that four stations along the radial direction form a *sector* that covers  $30^{\circ}$  in the r- $\phi$  projection. Thus, 12 sectors at the same  $\eta$  cover the full  $\phi$  angle making a *wheel*, while 5 sectors at the same  $\phi$  make a *wedge*.

The DT Regional Trigger structure is shown in Figure 1.  $\varphi$ Track Finder boards [5,6,7] perform local trigger segments correlation in the r- $\varphi$  projection. In parallel,  $\eta$  Track Finder boards use a pattern recognition algorithm on r-z projection hits to assign  $\eta$  values to found tracks [8]. Up to two tracks are built from data from one sector. Thus, up to 144 muon tracks can be built in the barrel region. The Muon Sorter selects up to 4 muon tracks to be forwarded to the Global Muon Trigger in two stages: 12 *Wedge Sorter* (WS) boards select up to 2 muons out of the 12 tracks collected from a wedge of the barrel; 1 single *Barrel Sorter* (BS) board performs the final selection of 4 tracks out of 24 tracks collected from the WS boards.

## B. Location of Regional Trigger hardware

Regional Trigger electronics is located in the underground counting room of the experiment (USC55). No radiation issues have to be considered. Thus, the trigger logic is designed using programmable logic (FPGA). Modules are VME 9U boards, with a depth of 40 cm. The crates host a single J1 VME backplane and a custom backplane that provides power supply (3.3 V and 5 V) and GTL+ busses to exchange data between the boards. The system is shown in Figure 2: two racks host six crates for the Track Finder system and Wedge Sorter boards. One more rack with one crate hosts the Barrel Sorter board. The WS to BS connection is built with twisted pairs cables for LVDS transmission.



Figure 1: Block view of the DT Regional Trigger system. Inside blocks the number of boards is shown, while numbers close to data flow arrows show the maximum number of muon tracks delivered by each stage.



Figure 2: DT Regional Trigger hardware layout.



Figure 3: Partial longitudinal cross section of the muon detectors, showing two examples of muons crossing wheel boundaries. Each track is reconstructed twice, by two consecutive  $\varphi$  Track Finders.

#### II. WEDGE SORTER BOARD

### A. Requirements

As it is shown in Figure 3, if a muon track crosses the boundaries between wheels, the two consecutive  $\phi$  Track Finders can build the same track, since they operate independently over their own sectors. Thus, a single muon can be reconstructed twice and two muons could be forwarded to the following stages of the trigger. The aim is to suppress this background below the real dimuon event rate that is about 1% of the single muon rate. Wedge Sorter board receives encoded information about the position of Local Trigger segments used by the  $\varphi$  Track Finder to build the tracks. Moreover, each track has attached a reconstruction quality. If two muons from consecutive sectors are found to be built with common segments, the Wedge Sorter module cancels the worst reconstruction quality member of the pair [9]. Simulation of the algorithm performed over single muon events shows that with this procedure the fake track rate can be reduced down to 0.3% at the end of the Muon Sorter, as shown in Table 1.

Table 1: Fake tracks rate at different stages of Muon Sorter logic.

|      | φ TF Output | WS Output | BS Output |
|------|-------------|-----------|-----------|
| Rate | 27 %        | 8 %       | 0.3 %     |

After fake tracks suppression, the Wedge Sorter has to sort the two "best" tracks of the received sample. This is done according to 8-bits ranking words, made of reconstruction quality and transverse momentum values, 3-bits and 5-bits values respectively. A fully parallel algorithm is used, more details can be found in the last paragraph for comparison with the Barrel Sorter algorithm. The two selected tracks are sent to the Barrel Sorter module. Full track data is made of 31 bits, as shown in Table 2. The full algorithm I/O count is about 450. Latency for sorting and multiplexing operations is limited to two BX, or 50 ns.

Table 2: Muon track information format

| Value     | Quality | P <sub>t</sub> | q  | Φ    | η   | Address |
|-----------|---------|----------------|----|------|-----|---------|
| Bits pos. | 3028    | 2723           | 22 | 2114 | 137 | 60      |

### B. Hardware implementation

The Wedge Sorter prototype board is shown in Figure 4. The algorithm has been designed in VHDL and it is fitted in a single FPGA chip, Apex20K400 from Altera, in 672 pins 1 mm-pitch BGA package. A VME interface, also written in VHDL, has been fitted into an Acex1k from Altera. The main features of the board are:

- The board is 10 layers with controlled impedance lines (100 ohm differential for LVDS, 50 ohm single ended for LVTTL).

- All LVTTL lines on the board are equipped with series terminations.

- Switching voltage regulators are used to generate 2.5 V for FPGAs powering and 1.5 V for GTL+ terminations.

- A JTAG chain connects the two FPGAs and the two configuration devices, allowing configuration and boundary scan testing of the devices. This chain can also be controlled by the VME FPGA, allowing remote reconfiguration of the main FPGA and boundary scan access through VME accesses.



Figure 4: Wedge Sorter board.

- A parallel and a serial (JTAG) interface connect VME chip and main FPGA. They are used to access registers used in main FPGA to store configuration parameters of the algorithms, or snap registers to monitor the chip during operation.

- The board can be clocked with three different sources: the default LVDS clock received from crate backplane, a TTL clock fed through a LEMO connector on front panel, useful in the debugging phase, and an on-board 40 MHz oscillator, that is used to ensure operation of the VME interface also when no external clocks are received. The clock used to feed the main FPGA chip is phase adjusted by a delay line that can be set through the VME interface.

## C. Stand alone board test

In order to avoid or reduce debug problems in integrated tests, an exhaustive stand alone test has been developed for

the Wedge Sorter board. The test setup is shown in Figure 5. We set up the test jig by using general purpose VME I/O boards, Pattern Units [10] (Figure 6), already developed by our group.



Figure 5: Wedge Sorter test setup.

Each Pattern Unit board can provide up to 128 I/Os in LVTTL, running up to 100 MHz frequency, and more boards can be set to work synchronously. Thus, adapter boards (shown in Figure 7) were designed to interface the Pattern Units to the Wedge Sorter (LVTTL to GTL+ for inputs, LVDS to LVTTL for outputs).



Figure 6: Pattern Unit board.

A VME bus extender over shielded flat cables has been built in order to put the setup on table top. This setup allowed us to emulate the Wedge Sorter I/O within the Regional Trigger system.



Figure 7: Adapter boards plugged into Wedge Sorter, signal conversion is shown.

The test procedure has undergone the following steps:

- Tuning of passive components used by switching voltage regulators to get very clean voltage levels with no switching noise.

- JTAG chain access with FPGAs configuration and boundary scan operations.

- Check of VME interface operation.

- Series resistors values were tuned by sampling signals at the end of long traces on the board, in order to match traces impedance. Overshoot and undershoot at switching edges are corrected with the right termination value (Figure 8).



Figure 8: LVTTL signals behaviour at traces end. From left to right: using 0, 22 and 33 ohm series resistors.

- Check of the BGA chip soldering, by injecting static patterns in inputs, reading outputs from the board and cross checking with boundary scan chain "sample" operations. The BGA chip soldering procedure has been analyzed also using X-ray pictures of the ball array, and chip side microscope pictures to check balls shapes (Figure 9).

- Timings of data and clock lines have been measured in order to understand board delays, clock-data phases, and skews.

- LVDS output transmission over 10 m twisted pair cable has been checked down to a bit error rate less than  $10^{-12}$ .

- On board cross talk has been checked by injecting several switching patterns and no effects were found.



Figure 9: Left: X-ray picture of the ball array. Right: microscope picture of the array side.

With this exhaustive test we could validate the board design. The full set of Wedge Sorter boards is now in production with no modifications of the design. Moreover, the WS board prototype is being used with a module of the  $\phi$  Track Finder in a test beam of the Drift Tubes Chambers. Thus, a full slice of the trigger system is being tested with real data.

#### III. BARREL SORTER BOARD

#### A. Requirements

Requirements of Barrel Sorter and Wedge Sorter are similar: fake track cancellation and sorting according to quality and transverse momentum. The overall design strategy has been the same: a 9Ux400 mm board, the aim to fit all algorithm logic on a single FPGA, latency for all operations limited to 3 BX. The main difference comes from the higher I/O count, 24 input and 4 output tracks, corresponding to about 860 bits. This implies a more complex fake track cancellation scheme, and a computationally heavy sorter stage.

#### B. Board design

The board layout is shown in Figure 10. The 24 input connectors for LVDS cables will be placed on board top. The mechanical issues arising from the plug-unplug operations led to the development of a mezzanine board for the main FPGA. This also reduces the number of layers for the mother board, which can be very high on the mezzanine because of the large BGA chip used. Moreover, the mezzanine could be reused for future or different implementations with other mother boards. Outputs will be sent in LVDS to the Global Muon Trigger through SCSI connectors at board front panel [11].



Figure 10: Barrel Sorter board layout.

The FPGA will be an Altera Stratix (or StratixII) in 1508 pins, 1mm-pitch BGA package. VME control and interfaces to the main FPGA are similar to those developed for the Wedge Sorter board.

### C. Main FPGA design

The algorithm running on the main FPGA of Barrel Sorter board is in principle similar to the Wedge Sorter one, but the sorting of 4 out of 24 tracks, with 8-bits ranking and 32 bits for the full tracks information, is computationally much



Figure 11: block view of the WS core implementation.

heavier and it should run with the same latency. In the fully parallel algorithm used in Wedge Sorter (scheme in Figure 11) the results of comparators checking all possible track pairs are analyzed by a set of equations delivering directly selection vectors for both the first and the second track found. The complexity of such an approach grows very steeply with both the number of input tracks and the number of tracks to be selected. This can be seen from the following simple calculations: having N tracks in input and requiring k tracks to be selected there are

$$N_{COMP} = N(N-1)/2$$
$$N_{EQ} = N!/(N-k)!$$
$$N_{IN/EQ} = k(2N-k-1)/2$$

where the three quantities are: the comparators required to check each possible pair, the number of equations required to decode the results, and the number of inputs each equation uses, respectively.

The critical behaviour is the factorial dependence of the number of equations from N and k, and the  $N \cdot k$  increase of the number of input signals for each equation. These quantities are directly related to the routing density required in the device. Latest FPGAs are provided with very fast look up table elements, but routing delays become dominant in an algorithm with high routing densities. In fact, there are not enough local (i.e., short range) interconnections to route signals between blocks. In this case, long range interconnections the are used, increasing overall



Figure 12: Block view of the Barrel Sorter algorithm implementation.

propagation time. It was clear that the fully parallel architecture, with N=24 and k=4, would not run at the required speed on any existing device. Thus, the task has been serialized in Barrel Sorter design. A simpler sorter 1 out of 24 has been designed using the same parallel approach: parallel comparison and results decoding. This sorter is used 4 times in sequence, setting to zero the ranking words of the tracks already selected (Figure 12). This structure is run at a frequency higher than 40 MHz to keep the overall latency of 75 ns.

The Barrel Sorter is now in the design phase. The chip is being simulated to finalize the VHDL design and to choose a specific model and speed grade of the Stratix device. The mother and mezzanine board electrical schemes are in the final design phase. We expect to produce the prototype boards by the end of 2004.

#### IV. SUMMARY AND CONCLUSIONS

In the CMS muon trigger, subsystems are designed to be redundant, to ensure operation of the chain in case of failures and to achieve a high efficiency. In DT Track Finder this implies a high number of candidate tracks and partial overlap of track finding regions of the modules. The Muon Sorter solves both the drawbacks. Using a fake track tagging scheme, it cancels tracks found twice by the Track Finder. Then, a configurable sorting process selects the "best" (high reconstruction accuracy, high transverse momentum) tracks from each event. These operations are performed in two stages, with Wedge Sorters and Barrel Sorter. Algorithms are implemented in FPGAs from Altera. The boards are interfaced for control and configuration by VME bus. The Wedge Sorter board prototype has been exhaustively tested with a stand alone setup that emulated the large I/O of the system in which the board will operate. The test was developed using Pattern Unit boards, general purpose VME I/O modules designed by our group. Wedge Sorter production is now in progress with no modifications to the prototype design. The prototype is being used in a slice test of the trigger system with real data from DT chambers in a test beam. The Barrel Sorter board is being designed, using latest FPGA technologies available. Even if Wedge Sorter and Barrel Sorter have similar tasks, the very large I/O of the latter led us to different choices in VHDL modelling and in the layout of the board. We expect to produce Barrel Sorter board by the end of the year.

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