Pixel Multichip Module for the BTeV Experiment at Fermilab

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Abstract

At Fermilab, a pixel detector is being developed for the BTeV experiment. The pixel detector will be located close to the beam, and all collected data will be read out for use in the lowest level trigger for track and vertex reconstruction every beam crossing. The results of the characterization of pixel multichip module prototypes as well as the baseline design of the readout scheme are presented. These prototypes were characterized for threshold and noise dispersion. The bump-bonds of the pixel module were examined using an X-ray inspection system. Furthermore, the connectivity of the bump-bonds was tested using a radioactive source (Sr 90), while the absolute calibration of the modules was achieved using X-ray sources.

I. INTRODUCTION

At Fermilab, the BTeV experiment has been proposed for the C-Zero interaction region of the Tevatron [1]. One of the tracker detectors for this experiment will be a pixel detector composed of 60 pixel planes of approximately 100x100 mm^2 each, assembled perpendicular to the colliding beam and installed at 6 millimeters from the beam, as shown in Figure 1. The planes in the pixel detector are formed by sets of different lengths of pixel-hybrid modules, each composed of a single active-area sensor tile and of linear array of readout ICs. The modules on opposite faces of the same pixel station are assembled perpendicularly in relation to each other.
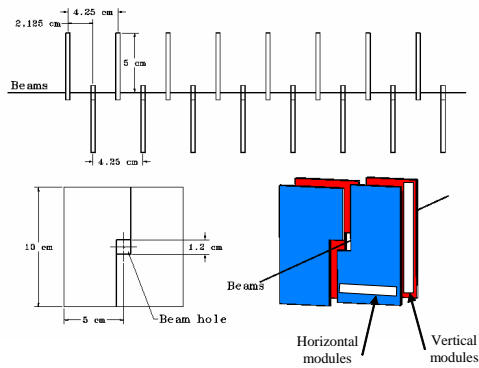

Figure 1: Pixel detector stations

The BTeV pixel detector module is based on a design relying on a hybrid approach [2]. With this approach, the readout chip and the sensor array are developed separately and the detector is constructed by flip-chip mating the two together. This approach offers flexibility in the development process, the choice of fabrication technologies, and the choice of sensor material.

The multichip modules must conform to special requirements dictated by BTeV: The pixel detector will be inside a strong magnetic field (1.6 Tesla in the central field), the HDI and the adhesives cannot be ferromagnetic, the pixel detector will also be placed inside a high vacuum environment, so the multichip module components cannot outgas, the particle fluence (around 3 Mrad per year at the edges of the detector closest to the colliding beams) and temperature (-5°C) also impose severe constraints on the pixel multichip module packaging design.

The pixel detector will be employed for on-line track and vertex finding for the lowest level trigger system. Therefore, the pixel readout ICs will output all detected hits. This requirement imposes severe constraints on the design of the readout IC, the hybridized module, and the data transmission rate to the data acquisition system.

Several factors impact the amount of data that each IC needs to transfer: readout array size, distance from the beam, number of bits of pulse-height analog to digital converter (ADC) data format, etc. Presently, the dimension of the pixel chip array is 128 rows by 22 columns and 3 bits of ADC information.

II. PIXEL MODULE READOUT

The pixel module readout must allow the pixel detector to be used in the lowest level experiment trigger. Our present assumptions are based on simulations that describe the data pattern inside the pixel detector. The parameters used for the simulations are: luminosity of 2×10^{32} cm^{-2}s^{-1} (corresponds to an average of 2 interactions per bunch crossing), pixel size of 400×50 μm^2, threshold of 2000 e$^-$ and a magnetic field of 1.6 Tesla. The pixel pitch in the 128 rows is 50μm, while the pixel pitch in the 22 columns is 400μm.

We've used simulations of the readout architecture with a clock rate of 35MHz. This frequency can support a readout efficiency of approximately 98% even when considering three times the nominal hit rate for the readout ICs closest to the

beam. Efficiency is lost either due to a pixel being hit more than once before the first hit can be read out, or due to bottlenecks in the core circuitry.

III.   PROPOSED READOUT ARCHITECTURE

The readout architecture is a direct consequence of the BTeV detector layout. The BTeV detector covers the forward direction, 10-300 mrad, with respect to both colliding beams. Hence, the volume outside this angular range is outside the active area and can be used to house heavy readout and control cables without interfering with the experiment. The architecture takes advantage of this consideration.

The data combiner board (DCB) is located approximately 10 meters from the detector and remotely controls the pixel modules. All the controls, clocks and data are transmitted between the pixel module and the DCB by differential signals employing a low-voltage differential signaling (LVDS) approach. Common clocks and control signals are sent to each module and then bussed to each readout IC. All data signals are point-to-point connected to the DCB. Figure 2 shows a sketch of the proposed readout architecture. For more details refer to [3][3]. The bias voltages for the pixel readout IC and the sensors are provided by separate cables.

This readout technique requires the design of just one rad-hard chip: the pixel readout IC. The point-to-point data links minimize the risk of an entire module failure due to a single chip failure. Simulations have shown that this readout scheme results in readout efficiencies that are sufficient for the BTeV experiment.
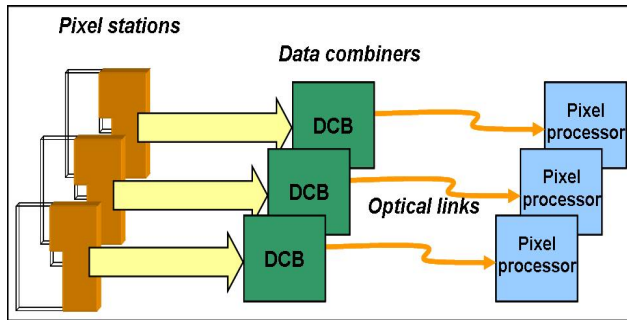

Figure 2: Pixel module point-to-point connection

A. Pixel Module Prototype

Figure 3 shows a sketch of the pixel module prototype. This design uses the third version of the Fermilab pixel readout IC, the FPIX2 IC. For more details on the FPIX2 IC refer to [4].
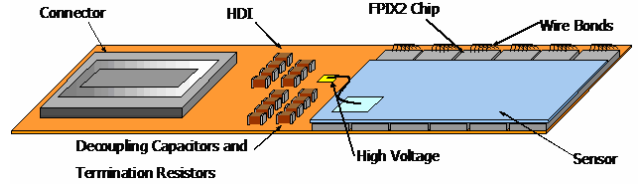

Figure 3: Sketch of the pixel multichip module

The pixel multichip module prototype is composed of three layers, as depicted in Figure 4. The high density interconnects (HDI) form the bottom layer. The back of the readout IC is in electrical and thermal contact with a ground plane on the top layer of the HDI, while the other side of the readout IC is flip-chip bonded to the silicon pixel sensor. The clock, control, and power pad interfaces of FPIX2 extend beyond the edge of the sensor and are wire bonded to the HDI. The HDI then extends to one end of the module where a set of wire bond pads interface the HDI to the data acquisition system. For the prototype module we've used low profile connectors to interface the module to the data acquisition system. The large number of signals in this design imposes space constraints and requires aggressive design rules, such as 50µm trace width, center-to-center pitch of 50µm, and via pads of 150µm.
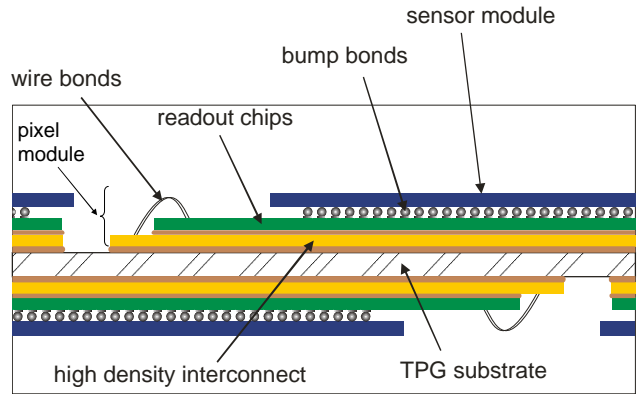

Figure 4: Sketch of the pixel multichip module "stack"

This packaging requires a HDI with four layers of copper traces. The data, control and clock signals use the two inner layers; power uses the bottom layer, while a single ground uses the top layer. The HDI has two power traces, one analog and one digital. These traces are wide enough to guarantee that the voltage drop from chip to chip is within the FPIX2 ±5% tolerance. The decoupling capacitors in the HDI are close to the pixel chips. The trace lengths and vias that connect the capacitors to the chips are minimized to reduce the interconnection inductance. A picture of the 6-chip module prototype is shown in Figure 5a. Figure 5b-d shows the small via pads and via holes of this HDI.
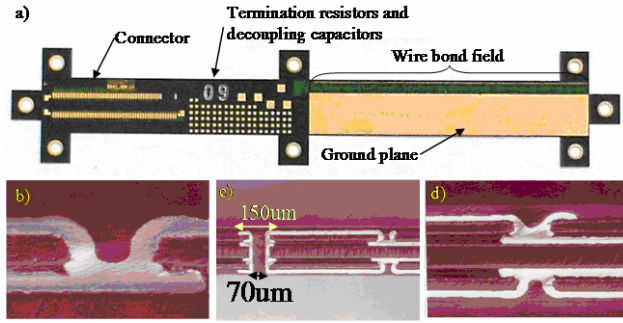
Figure 5: HDI picture

To minimize coupling between digital and analog elements, signals are grouped together into two different regions. The digital and analog traces are laid out on top of the digital and analog power supply traces, respectively. Furthermore, a ground trace runs between the analog set and the digital set of traces.

B. High Voltage Bias

The pixel sensor is biased through the HDI using up to 1000VDC. The coupling between the digital traces and the bias trace has to be minimized to improve the sensor noise performance. To achieve this, the high voltage trace runs in the second metal layer between ground traces in the first and third layers. The high voltage trace is connected to a pad on the top layer of the HDI, which is then wired to the sensor.

C. Assembly

The pixel module packaging is a 3 layer "stack". The bottom layer of this "stack" is the HDI, on top of which is assembled the pixel readout ICs. Conductive epoxy electrically and mechanically connects the back of the readout ICs to the ground plane on the top layer of the HDI. The HDI wire bond pads extend 1mm beyond the readout ICs. In order to provide mechanical support to the wire bond section of the HDI the whole module is assembled on an Aluminum support structure, as shown in Figure 6. The region of this structure right underneath the pixel module is filled with porous Aluminum, which is connected to a vacuum pump and used to hold down the HDI during wire bonding. Preliminary results with around 1200 wire bonds show that this technique provides wire bonds with pull strengths in the order of 10g. A picture of the support structure with a 6-chip module (bare dies, no sensor) is shown in Figure 7.
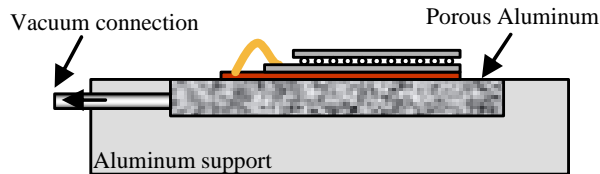

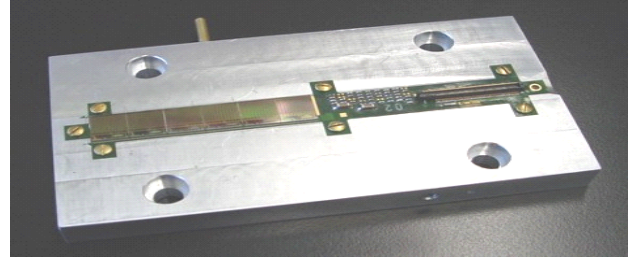Figure 6: Sketch of module support structure

Figure 7: Module support structure with 6-chip module (bare dies)

IV.   PIXEL MODULE EXPERIMENTAL RESULTS

In this section the characterization results of one 5-chip module are presented. The pixel module has been characterized for noise and threshold dispersion. These characteristics were measured by injecting charge in the analog front end of the readout IC with a pulse generator and reading out the hit data through a PCI based test stand developed at Fermilab. The results for different thresholds are summarized in Table 1.

Table 1: Performance of the pixel prototype module (in e^-)

		Chip 1	Chip 2	Chip 3	Chip 4	Chip 5
Threshold	μ	4000	4000	4000	4000	4000
	s	200	180	220	195	180
Noise	μ	77	80	90	87	90
	s	7	9	8	8	9

The comparison of these results with previous results (single bare die readout IC without the HDI) shows no noticeable degradation in the electrical performance of the pixel module. The results with these bare dies readout ICs show a noise of $70e^-$ and a threshold dispersion of $180e^-$ [4].

Figure 8 shows the hit map of the 5-chip pixel module using a radioactive source (Sr 90). This result was obtained by shining the radioactive source distant 4cm from the module, and centered on top of chip 3. Figure 9 shows the hit map as the radioactive source was moved and centered on top of each of the readout chips of the module. These results show that the bump-bond connectivity is excellent. There is only one not connected bump bond (chip 3) in the whole module. Figure 10 shows a picture of the 5-chip pixel module.
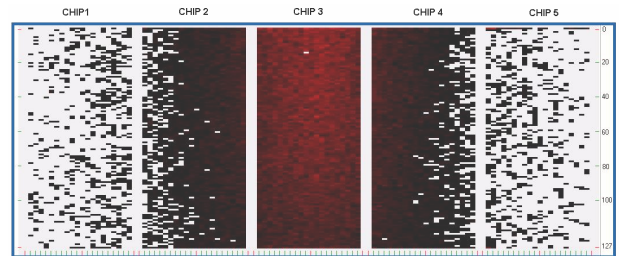

Figure 8: Pixel multichip module hit map when source is centered on top of chip 3
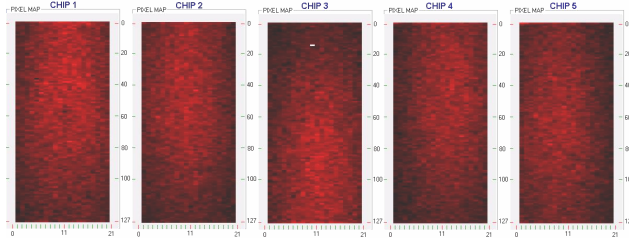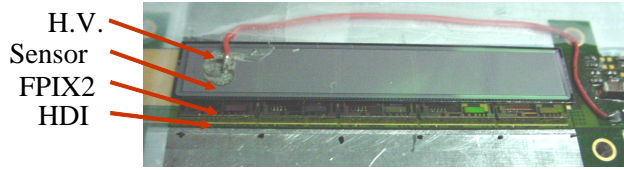
Figure 9: 5-chip pixel module hit map

Figure 10: Pixel module bump-bonded to 5 readout ICs

Table 2 shows the influence that the threshold variation has on the noise of the readout IC. The test has been performed in all chips, but just the results for chip 3 are presented. The 5 chips tested showed similar performance. These results show that the pixel module has a fairly flat noise as a function of the threshold.

Table 2: Performance of the pixel prototype module (in e⁻)

	Threshold		Noise	
	μ	σ	μ	σ
	4000	200	77	7
	3700	178	82	9
	3300	172	78	9
Chip 3	2700	165	80	9
	2300	152	79	8
	1800	144	78	10

V. HYBRIDIZATION RESULTS

Pixel detectors proposed for the new generation of hadron collider experiments will use bump-bonding technology based on either indium or Pb/Sn solder to connect the front-end readout chips to the silicon pixel sensors. We have previously reported large-scale tests of the yield using both indium and Pb/Sn solder bump [5]. We have also carried out studies of various effects (e.g. storage over long period, effect of heating and cooling, and radiation) on both types of bump bonds using daisy-chained parts on a small scale. We have also studied the bumps by visual inspection of bumps that bond silicon to glass sensors before and after thermal cycles and irradiation, with and without being attached to a thermal pyrolytic graphite (TPG) substrate having a different coefficient of thermal expansion (CTE). We concluded that the bump bonding technologies with indium and solder are both viable for pixel detectors. The indium bumps look somewhat more susceptible to temperature variations. We

visually observed the degeneration of these bumps at cold temperatures. The shift on some of the glass chips we observed can be attributed to the production errors (misalignment) rather than the temperature changes. The solder bumps, on the other hand, were not affected by temperature changes or by radiation. The visual changes we observed are superficial in origin and are not expected to cause any operational problems. The CTE mismatch between the TPG and the silicon of the sensors seems to have no effect on the structural integrity of the bump bonds of either kind.

We studied the effect of cryogenic temperatures on the bonds using daisy chained bump-bonds connecting silicon dummy hybrids. We built a cryo vessel that houses a printed circuit board (PCB) on which we installed a dummy hybrid. This hybrid contained 48 channels each with a daisy chain of 14-16 solder bumps. The channels were wire-bonded to the strips on the PCB and the strips were accessed from outside of the vessel by flat cable connectors. We then measured the electrical resistance of the channels. An open channel (infinite resistance) would indicate a break in either at the bumps or the wire-bond. We had 3 such channels. The hybrid was glued on a TPG, which was glued on a copper plate. The copper plate, and therefore the TPG and the hybrid, were cooled in the vessel by conduction. Figure 11 shows the PCB and the hybrid. We had two cycles of exposing this PCB-hybrid assembly to LN2 temperatures over an 8 hour period each, and all of 45 good channels and their wire-bonds survived with no damage.
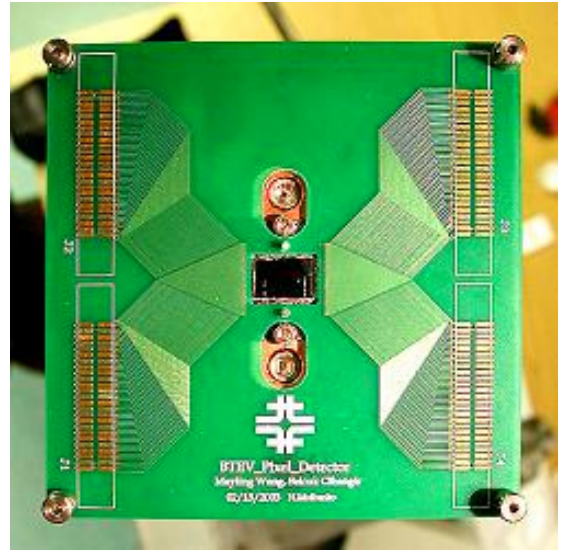

Figure 11: PCB-hybrid assembly for the cryo test

Furthermore, we also have modules that are hybrids of BTeV FPIX2 chips solder bump-bonded to silicon sensors. These hybrids are made up of 1, 4, 5, 6 or 8 readout ICs. In total we have visually inspected 160 hybridized readout ICs with an X-ray imaging system and observed no damage, bridge between bumps, or variation of size of the bumps. Figure 12a shows an image from the X-ray inspection system

of a good set of bump-bonds. For comparison, Figure 12b shows some bad bumps encountered in a previous sample of this device.
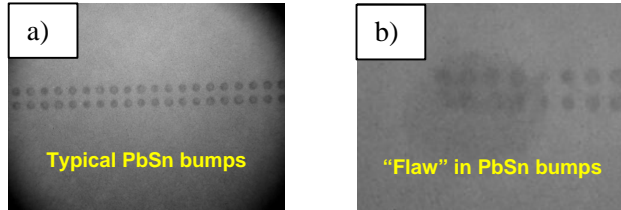

Figure 12: X-Tay picture of bumps on an assembly

VI. CONCLUSIONS

In this paper we have described the baseline pixel multichip module designed to handle the data rate required for the BTeV experiment at Fermilab. Furthermore, the assembly and characterization of a 5-chip pixel module prototype was successful. The tests detected no crosstalk problems between the digital and analog sections of the readout chip and the HDI. The characterization of the prototypes showed that there is no degradation in the electrical performance of the pixel module when compared with previous prototypes. Furthermore, the 5-chip module showed no significant increase in noise and threshold dispersion when compared with the single chip bare die prototypes.

VII. REFERENCES

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