MULTIPROCESSOR SYSTEM CONTROLLING POWER DISTRIBUTION FOR THE ATLAS SCT

On behalf of ATLAS SCT community

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&
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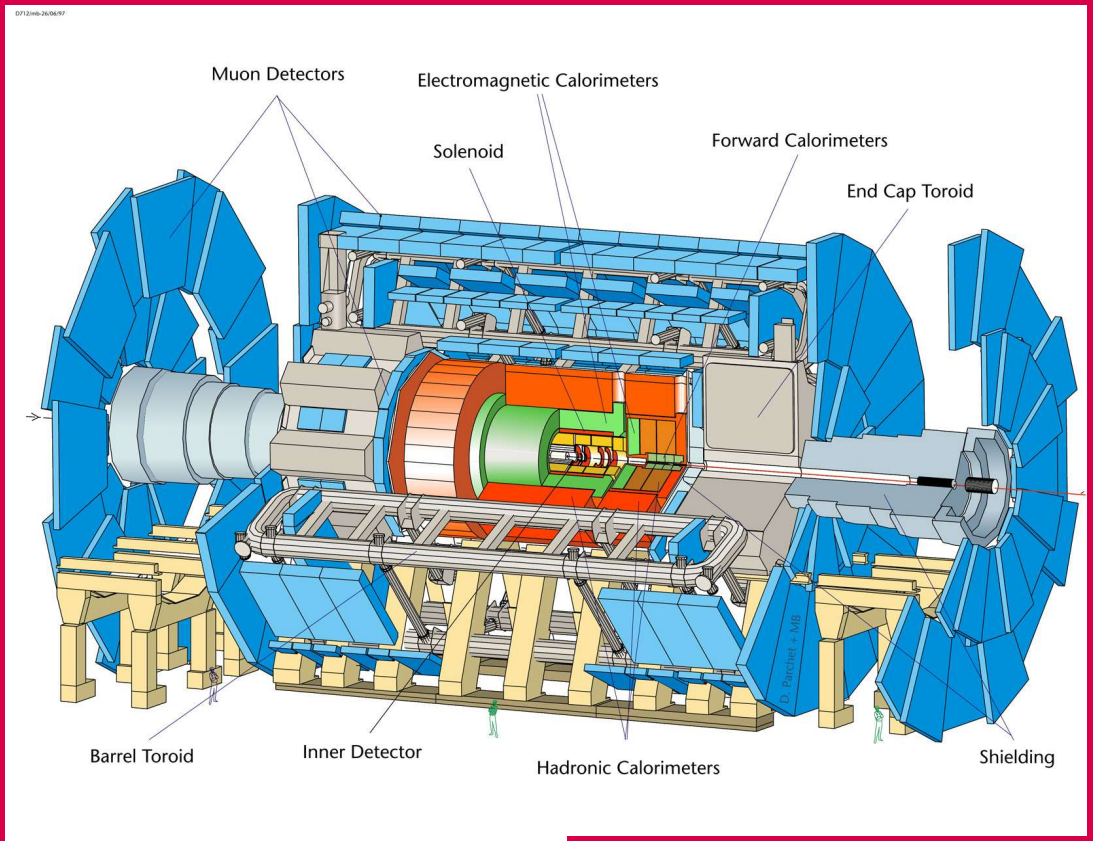
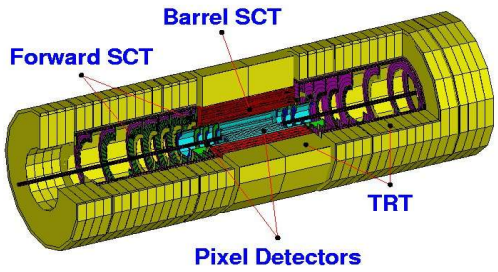
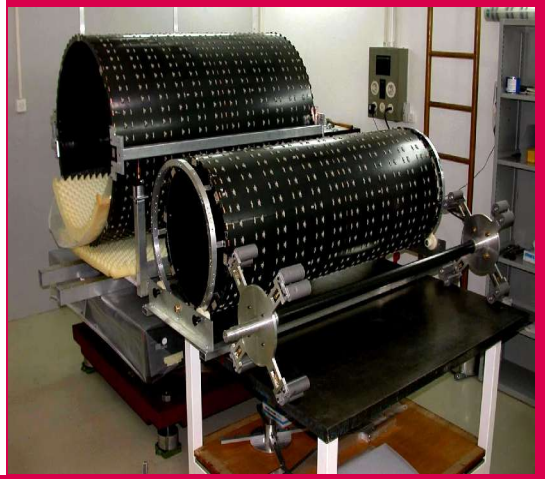
OUTLINE







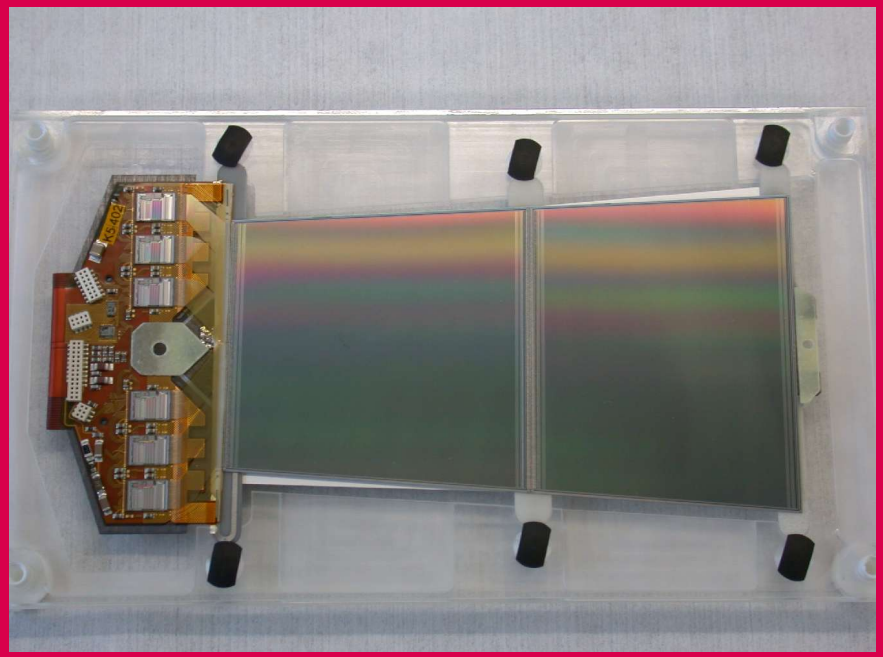
ATLAS SEMI-CONDUCTOR TRACKER

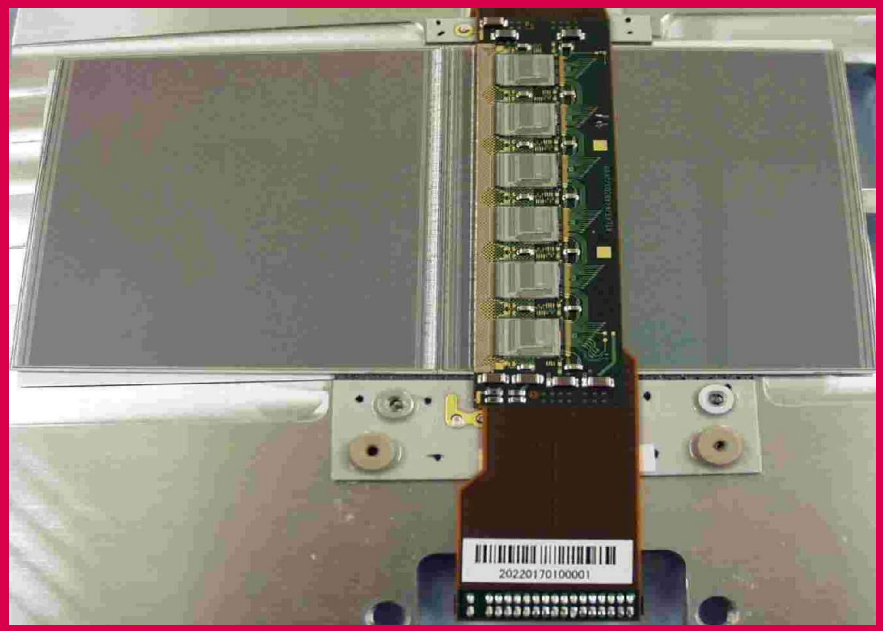
4088 MODULES
- 4 Barrel layers - 2112 modules
- End cap wheels - 1976 modules

MODULE:
- 2 single-side microstrip detectors
- 768 strips each
- read by twelve 128-channel chips
- *N.B. (also) Cracow FPNT UMM design*

- and equipped with opto-electronics (for two lines) assembled on “hybrids”

- End cap and barrel modules are identical wrt power supplies



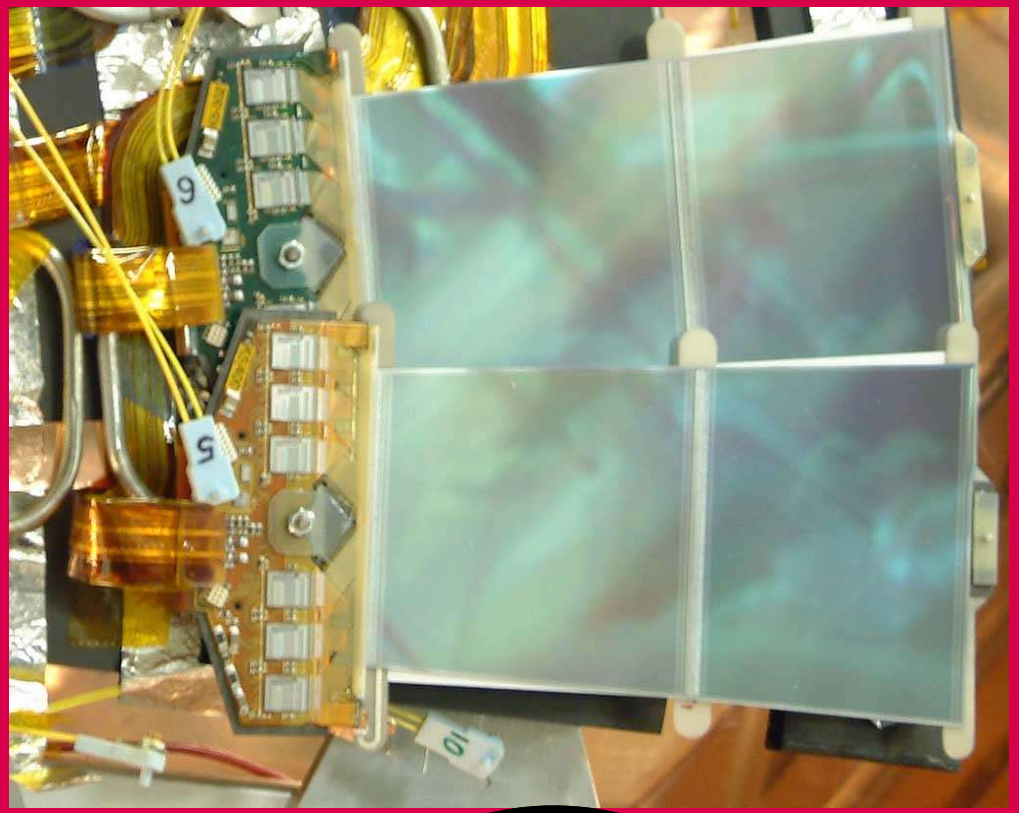


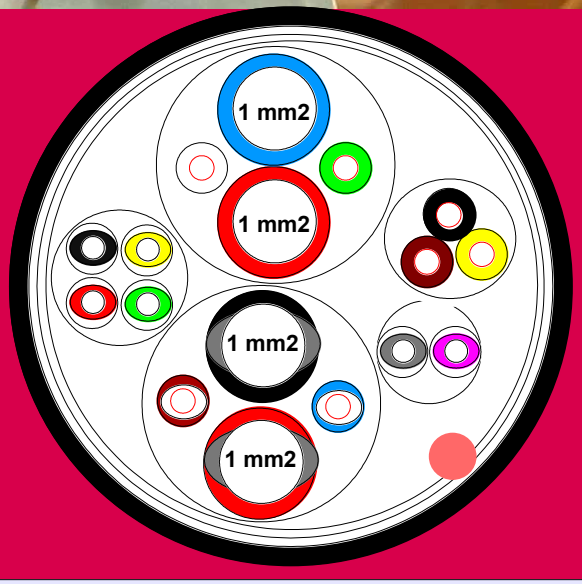
ATLAS SEMI-CONDUCTOR TRACKER POWER DISTRIBUTION

SCT modules are powered by DC isolated, “floating” low voltage (LV) and high voltage (HV) power supply modules via long, multi-wire lines.

LV and HV power supply modules are integrated in several ways.
All low voltages and control levels as well as HV for each detector module are transmitted from corresponding LV and HV module via dedicated multi-wire conductors of thickness varying from “thick, conventional” cable to low mass Kapton tapes.

Racks with SCT power supply modules will be distributed in USA15 and US15 caverns (11 + 11 racks).





ATLAS SEMI-CONDUCTOR TRACKER
LOW VOLTAGE POWER SUPPLIES

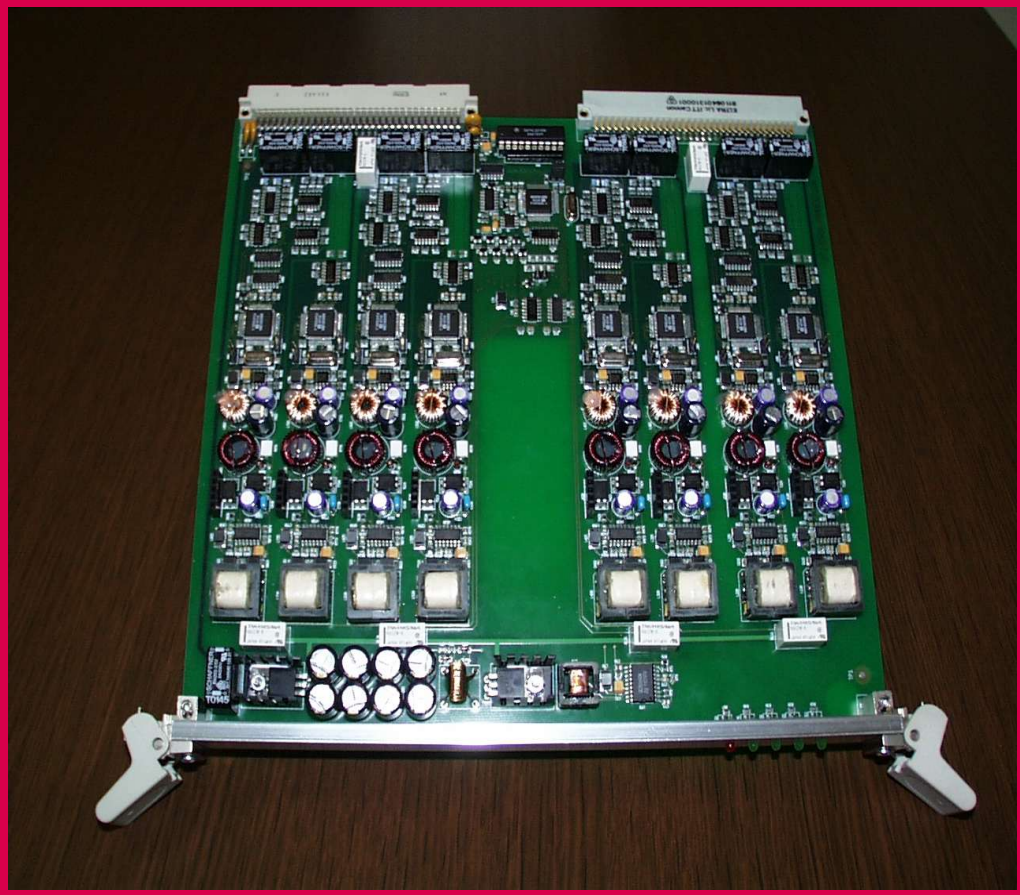
each LV module provides:

"Digital" voltage	4 V	0.5/1.3 A
"Analog" voltage	3.5 V	0.9/1.3 A
Vcsel ctrl. Voltage	1.6 : 6 V	4/6 mA
Photo-diode suppl.	10V	0.6/1 mA

2 NTC thermistor current sources
RESET/SELECT control levels

LOW VOLTAGE BOARD
CONTAINS 4 MODULES

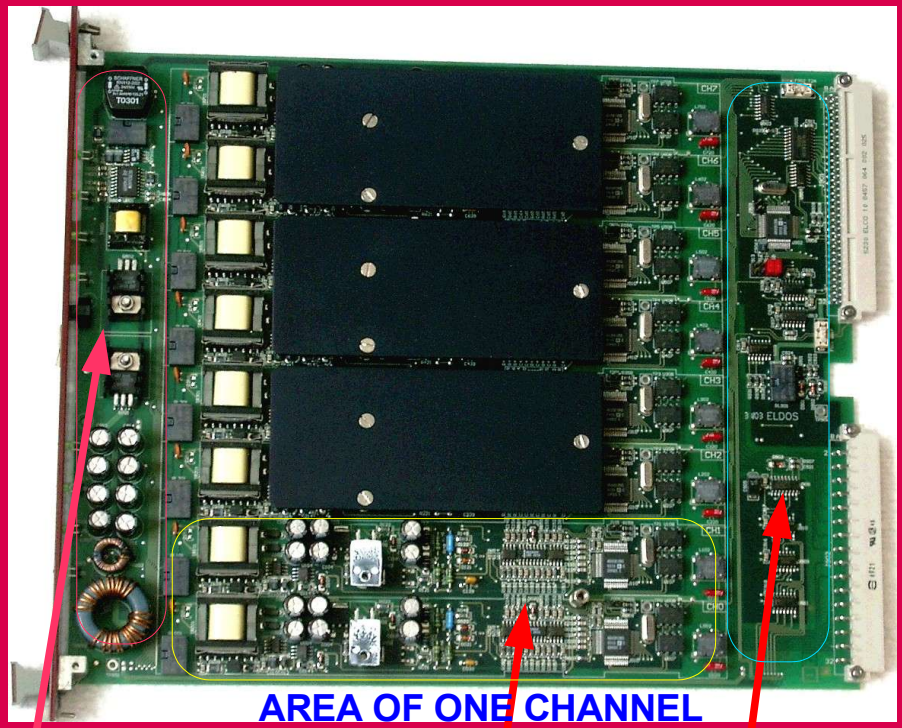
EACH LV MODULE IS DRIVEN BY
TWO µCONTROLLERS ADµC812
and
ANOTHER ADµC812 CONTROLS EACH CARD



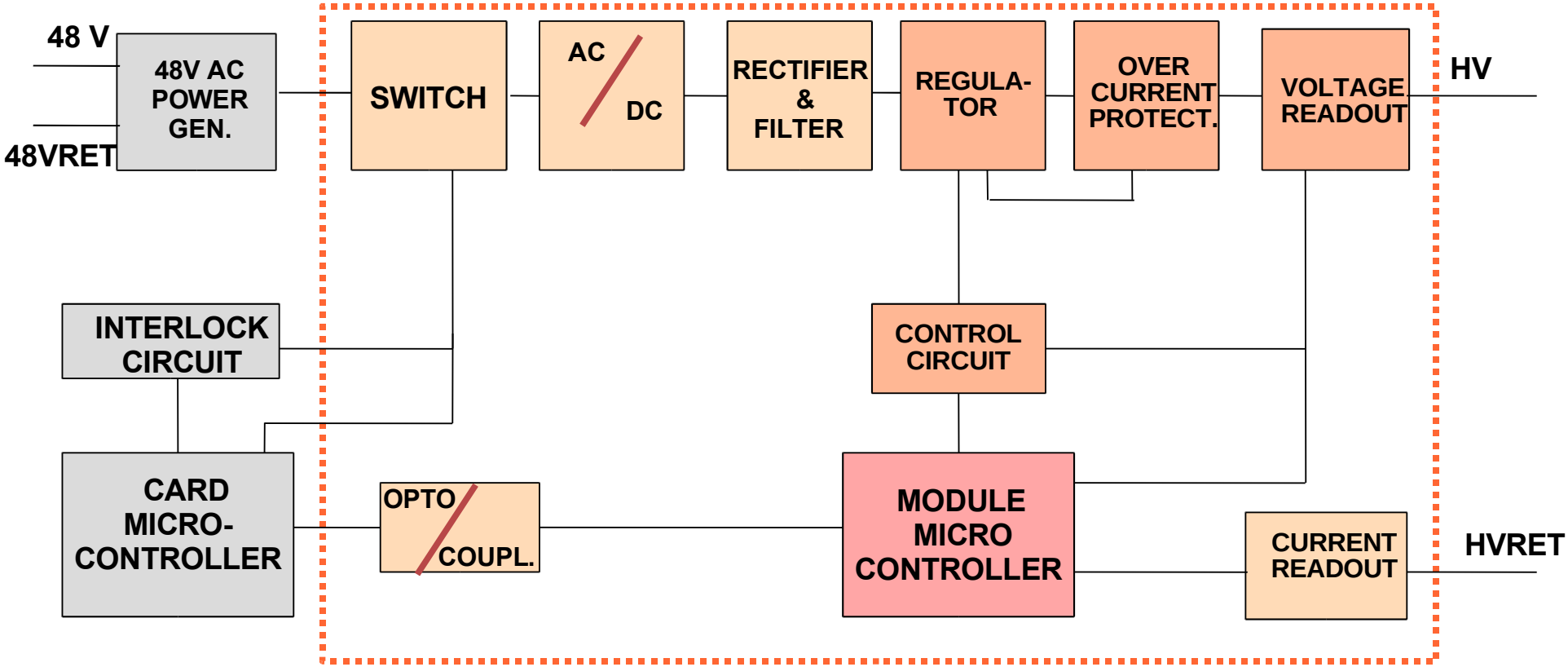
ATLAS SEMI-CONDUCTOR TRACKER
HIGH VOLTAGE POWER SUPPLIES

HV BOARD CONTAINS
8 INDEPENDENT HV CHANNELS (MODULES)

EACH HV MODULE PROVIDES:
NOMINAL VOLTAGE 0 - 500 V
MAXIMUM LOAD 5 mA
DC ISOLATION:
POWER LINES - MAGNETIC
CONTROL LINES - OPTICAL
DIGITAL CONTROL
VOLTAGE RAMPING RATES 50, 20 , 10, 5 V/s
CURRENT MEASUREMENTS RANGE 50nA - 5mA
PROGRAMMABLE OVERCURRENT PROTECTION
OVERVOLTAGE PROTECTION
INTERLOCKS



BASIC HV MODULE DESIGN

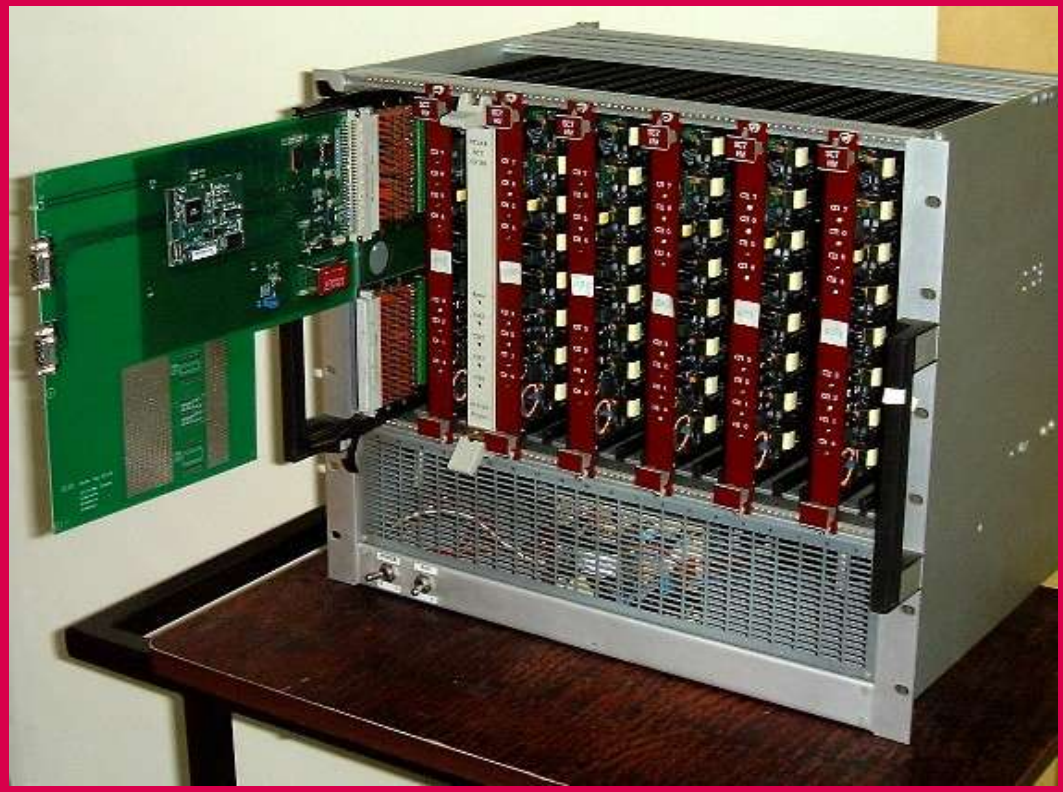


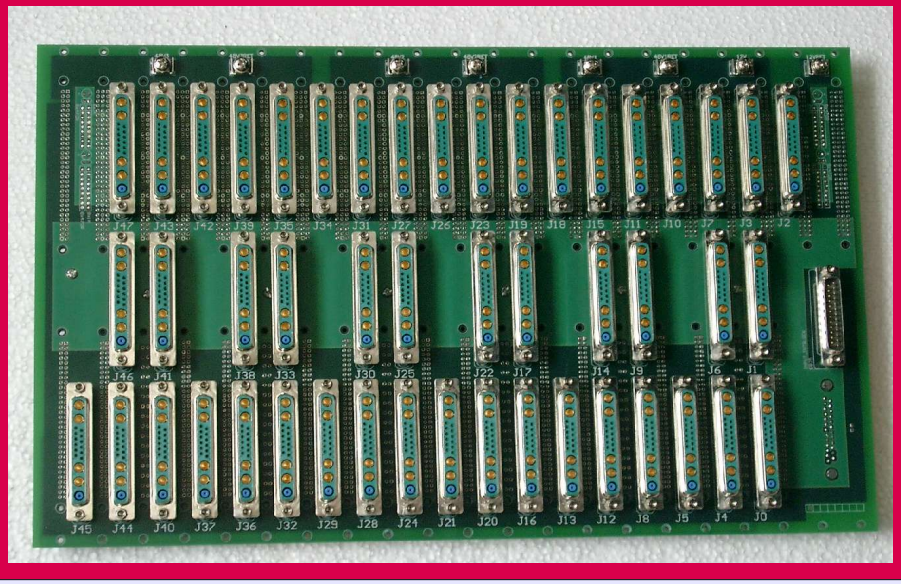
LV / HV INTEGRATION

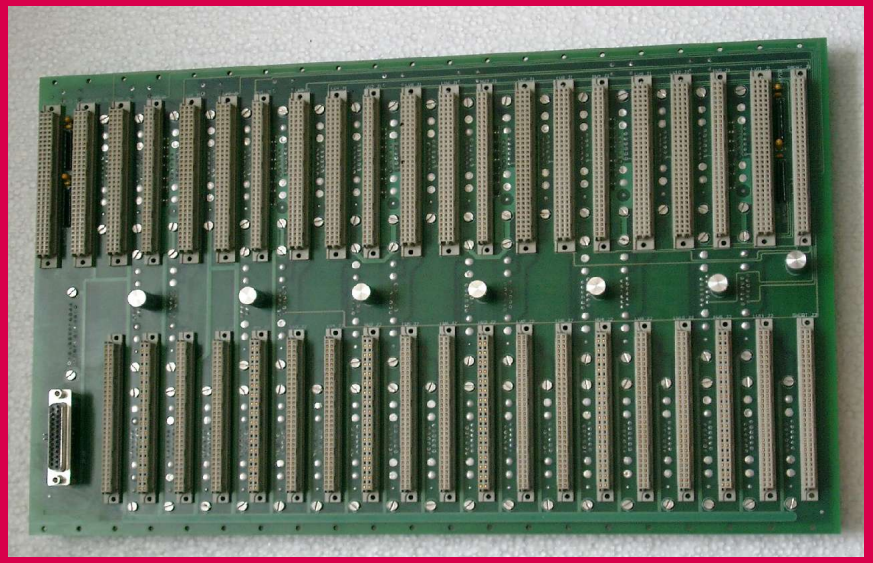
COMMON CRATE HOUSES 48 PS MODULES
- -12 LV BOARDS
- - 6 HV BOARDS
- - CRATE CONTROLLER BOARD
- - INTERLOCK CARD
- - SHORTING CARD

STANDARD 19” MECHANICS

CUSTOM DESIGN BACKPLANE
FOR POWER AND CONTROL TRANSMISSION
CUSTOM COMMUNICATION







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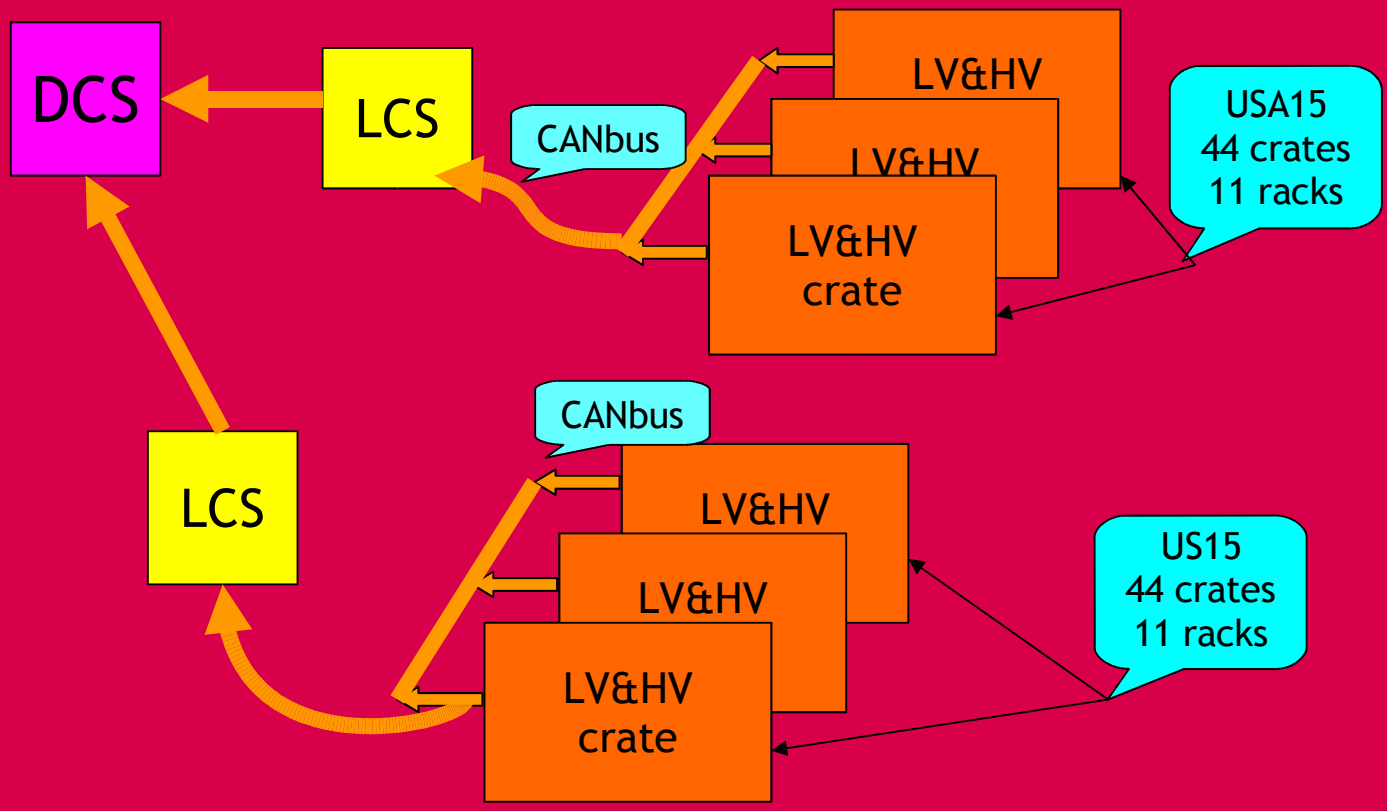
DCS – ANOTHER ASPECT OF INTEGRATION AND STANDARIZATION

CRATE CONTROLLER BOARDS USE **ELMB's** PROCESSOR ATMega128, EXTENDING ITS FUNCTIONS



MULTIPROCESSOR SYSTEM CONTROLLING POWER DISTRIBUTION FOR THE ATLAS SCT

PEOPLE

HARDWARE DESIGN of HV SYSTEM, the CRATE CONTROLLER & BACKPLANE

Edward GÓRNICKI and Stefan KOPERNY
Institute of Nuclear Physics PAS,
Faculty of Physics and Nuclear Techniques
University of Sciences and Technology,
Cracow, Poland

HV FIRMWARE & CRATE CONTROLLER SOFTWARE

Piotr MALECKI and Ewa STANECKA
Institute of Nuclear Physics PAS
and CRACOW UNIVERSITY OF TECHNOLOGY

HARDWARE and FIRMWARE DESIGN of LV SYSTEM

Jan STASTNY and Jan BOHM
Academy of Sciences
of the Czech Republic, Prague

GUI and other interfaces - SOFTWARE of CAN - PVSS ...

Pamela FERRARI, Heidi SANDAKER and Ewa STANECKA,
CERN and INP PAS

ALL THAT COULD NOT BE DONE WITHOUT HELP, MANY ADVICES AND DISCUSSIONS AS WELL AS DEVELOPMENTS OF ASSOCIATED PROJECTS CONCERNING GROUNDIG AND SHIELDING, PATCH PANELS, VOLTAGE LIMITERS, CABLES, CONNECTORS, POWER PACK's CONTROL, INTERLOCKS etc. EQUALLY IMPORTANT WERE AND STILL ARE SYSTEM TESTS AND BEAM TESTS
Am incomplete list of names include Richard Brenner, Alex Grillo, David Howel, Marko Mikuz, Gareth F. Moorhead, Martin Morrissey,Hans-Guenter Moser, Ned Spencer, Jo Pater, Peter W. Phillips, Heinz Perneger, Michał Turała, Mike Tyndel - CERN, NIKHRF, Melbourne,RAL, Santa Cruz, Upsala ...

STATUS OF THE PROJECT

HV and LV cards are now in mass production in Czech Republic and in Poland.
Should be completed by the of 2004.

Pre-production of some 25 Crate Controller boards completed in Poland.
The rest is ordered recently

Pre-production of 10 Backplanes done in Poland and 15 more ordered.
The rest will likely be ordered in Australia.

Firmware and software intesively tested
and slowly improving.

MULTIPROCESSOR SYSTEM CONTROLLING POWER DISTRIBUTION FOR THE ATLAS SCT

The system has grown up to
about 14 000 microprocessors

Real-Time?

Its temporal properties are essential
for reliability and correctness.

Are we aware of all that?

Tests, tests, tests ...

In the following part
some aspects and examples
for the HV sub-system are shown

HV

4088 modules -> 4088 µcontrolers
511 boards -> 511 µcontrolers
==========
4599 µcontrolers

LV

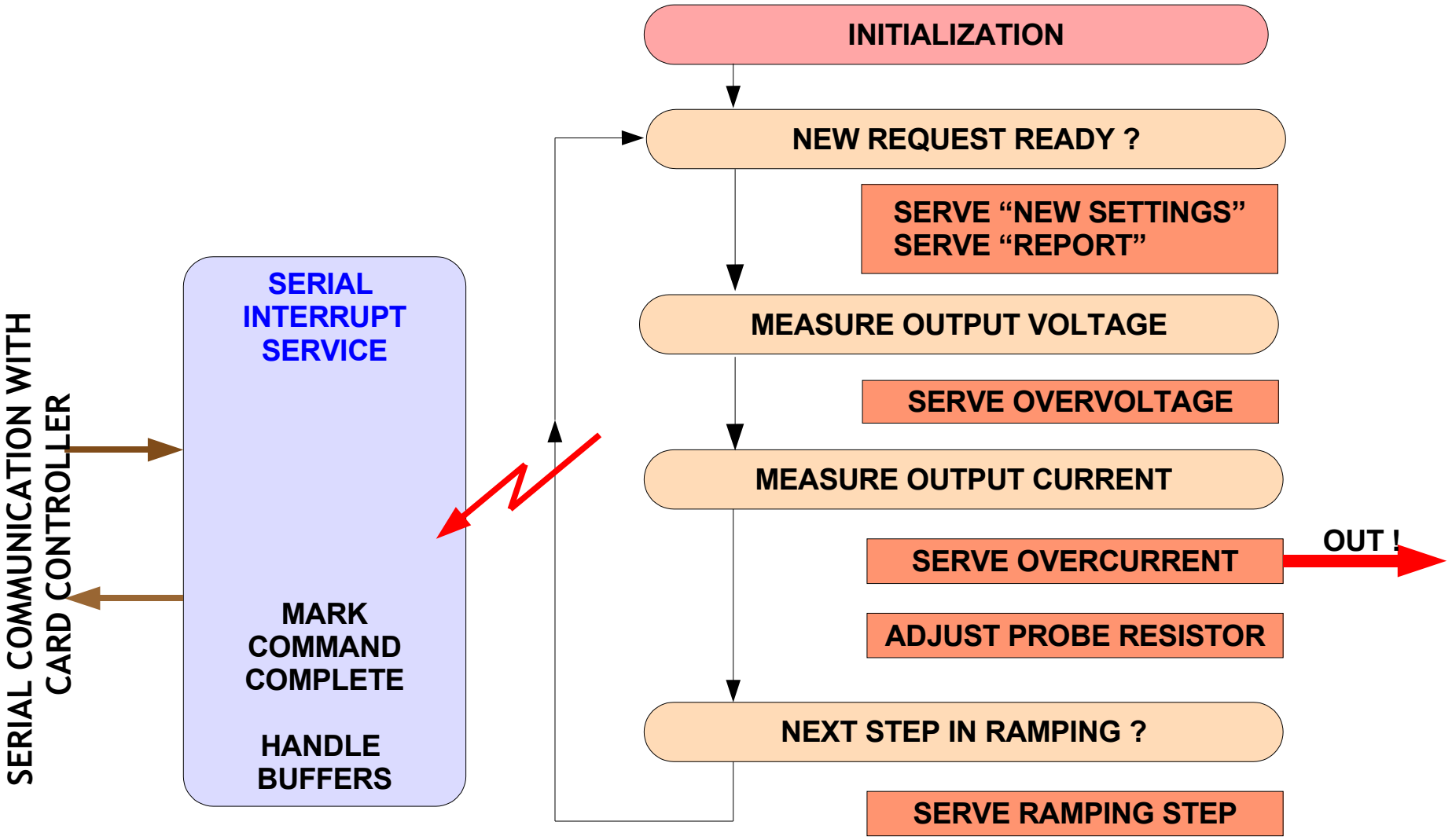
4088 modules -> 1022 µcontrolers
922 boards -> 922 µcontrolers
==========
9198 µcontrolers

13 797 CISC processors, “family 51”
Analog Devices' AduC812, with 12-bit
DACs and ADCs, UART, timers etc
Operate with 16 and 8 MHz clocking

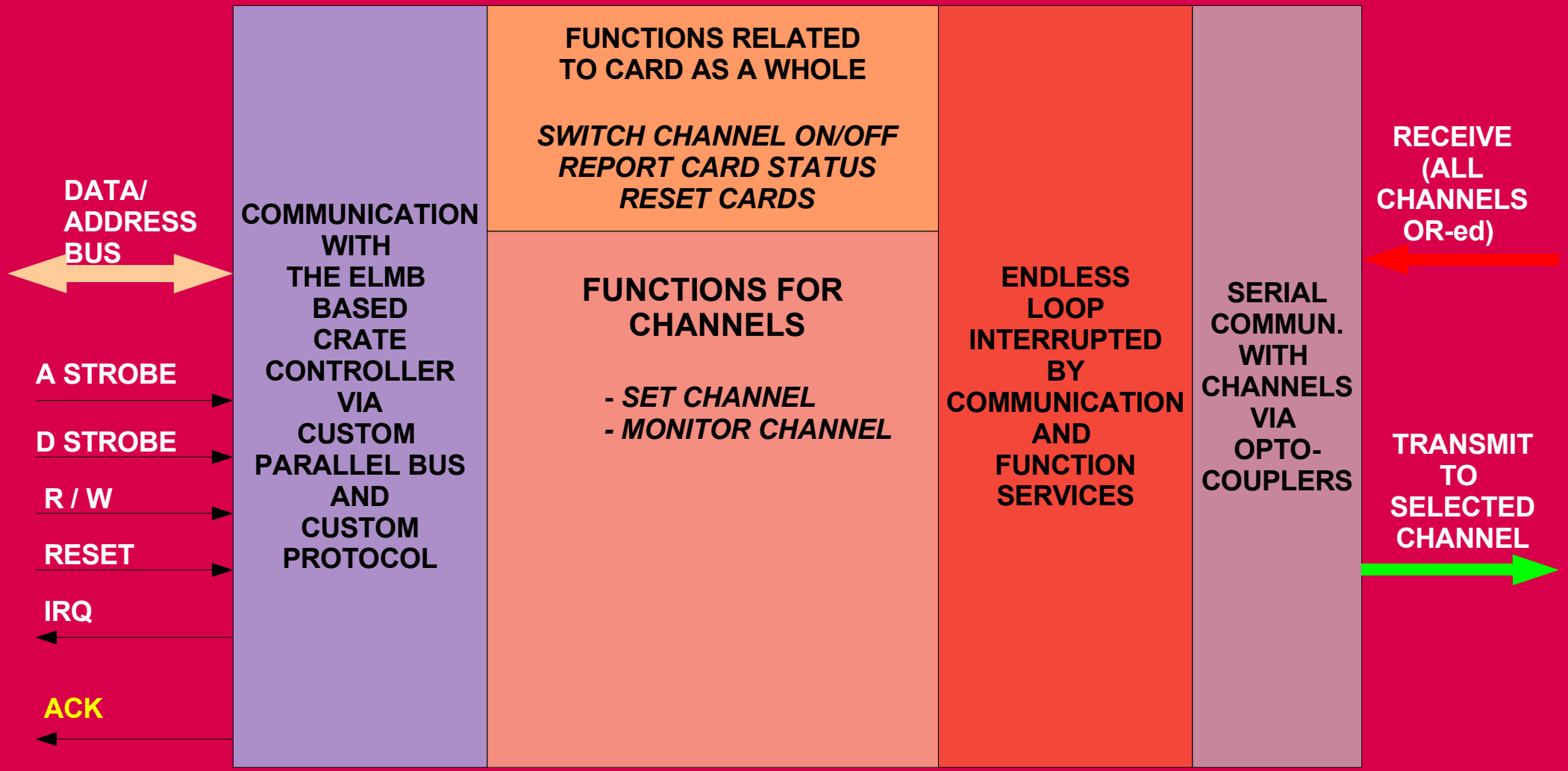
CRATE CONTROL

88 crates (two not fully populated)
controlled by 8-bit RISCs: ATMega128
(our non-standard use of the ATLAS ELMB-
embedded local monitor boards)

HV MODULE's µCODE

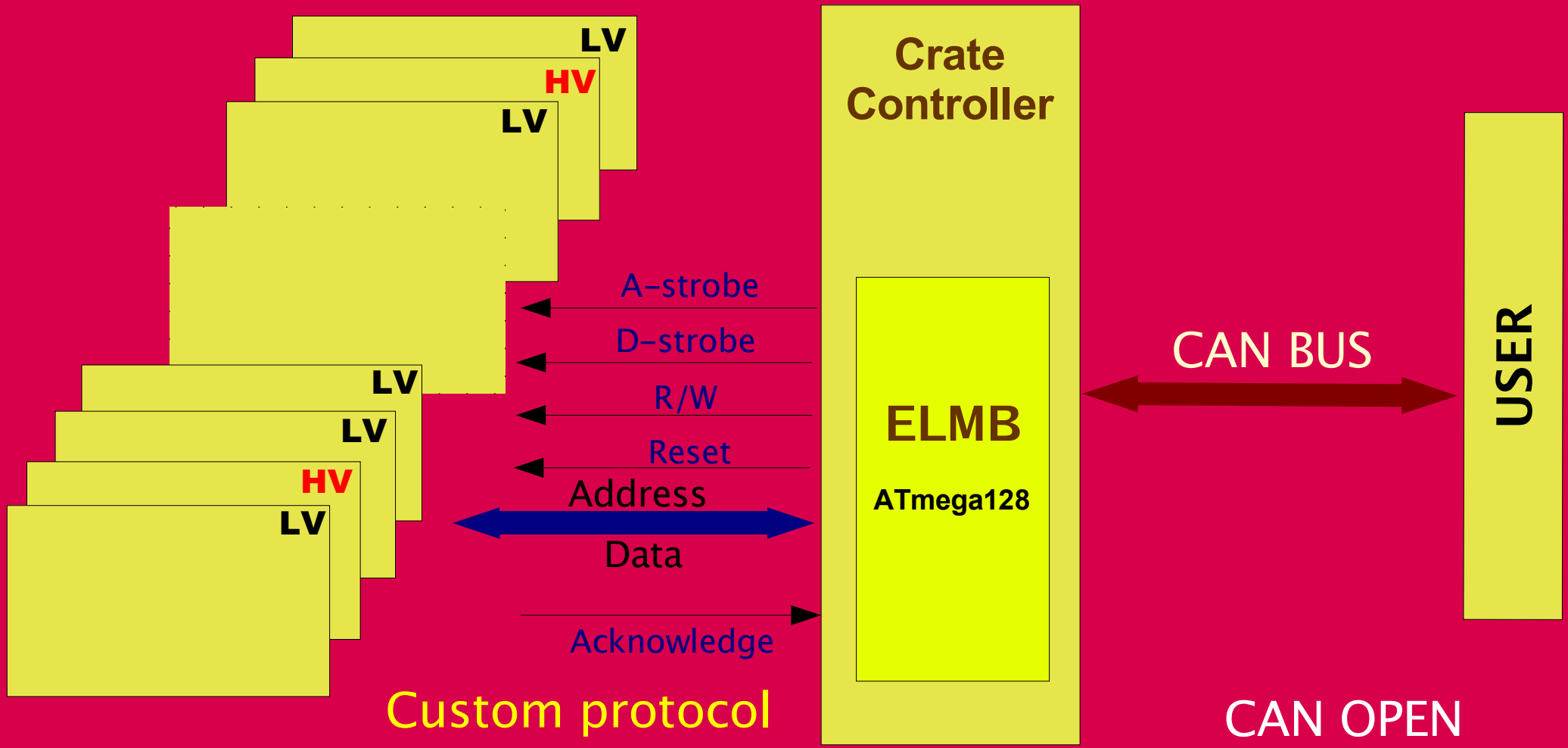


CARD CONTROL



Crate Controller has two faces:

- directed towards hardware of SCT PSs
- directed towards users (DCS)



Life on the custom backplane bus (partial example):

Write HV board

(a routine, extending the ELMBIO.c code loaded into ATmega128L)

data: 1+1 bytes

"FLBOA"	*S/M*	*B/C*	*X*	*board address*				
	bit 7	*bit 6*	*bit 5*	*bits 4 - 0*				
"MASK"	*CH7*	*CH6*	*CH5*	*CH4*	*CH3*	*CH2*	*CH1*	*CH0*
	bit 7	*bit 6*	*bit 5*	*bit 4*	*bit 3*	*bit 2*	*bit 1*	*bit 0*

Write LV board

(a routine, extending the ELMBIO.c code loaded into ATmega128L)

data: 1+2 bytes

"FLBOA" , "MASK", as above except : only 4 lsb bits in MASK

"PML" unsigned byte, "power" limit in units of 0.4 V

Write HV channel

(a routine, extending the ELMBIO.c code loaded into ATmega128L)

data: 1+13 bytes

FLBOA, CHANNO, VNOMH, VNOML, CTL0H, CTL0L, CTL1H, CTL1L, CTL2H, CTL2L, CTL3H, CTL3L, RCODE, CNTRLBYTE

Write LV channel

(a routine, extending the ELMBIO.c code loaded into Atmega128L)

data: 1+ 10 bytes

FLBOA, CHANCB, VCC, ICCTD, VDD, IDDTD, VPIN, VCSEL, OVTWRNL, TTLIMIT

On the CAN BUS ...

Rather fresh field for us, we have profited from help, advice and discussions with Henk Boterenbrood, Helfried Burckhart, Serguei Basiladze, Jola Olszowska, ...

All the “real time” actions taking place on the custom bus correspond to certain class of activities on the CAN bus.

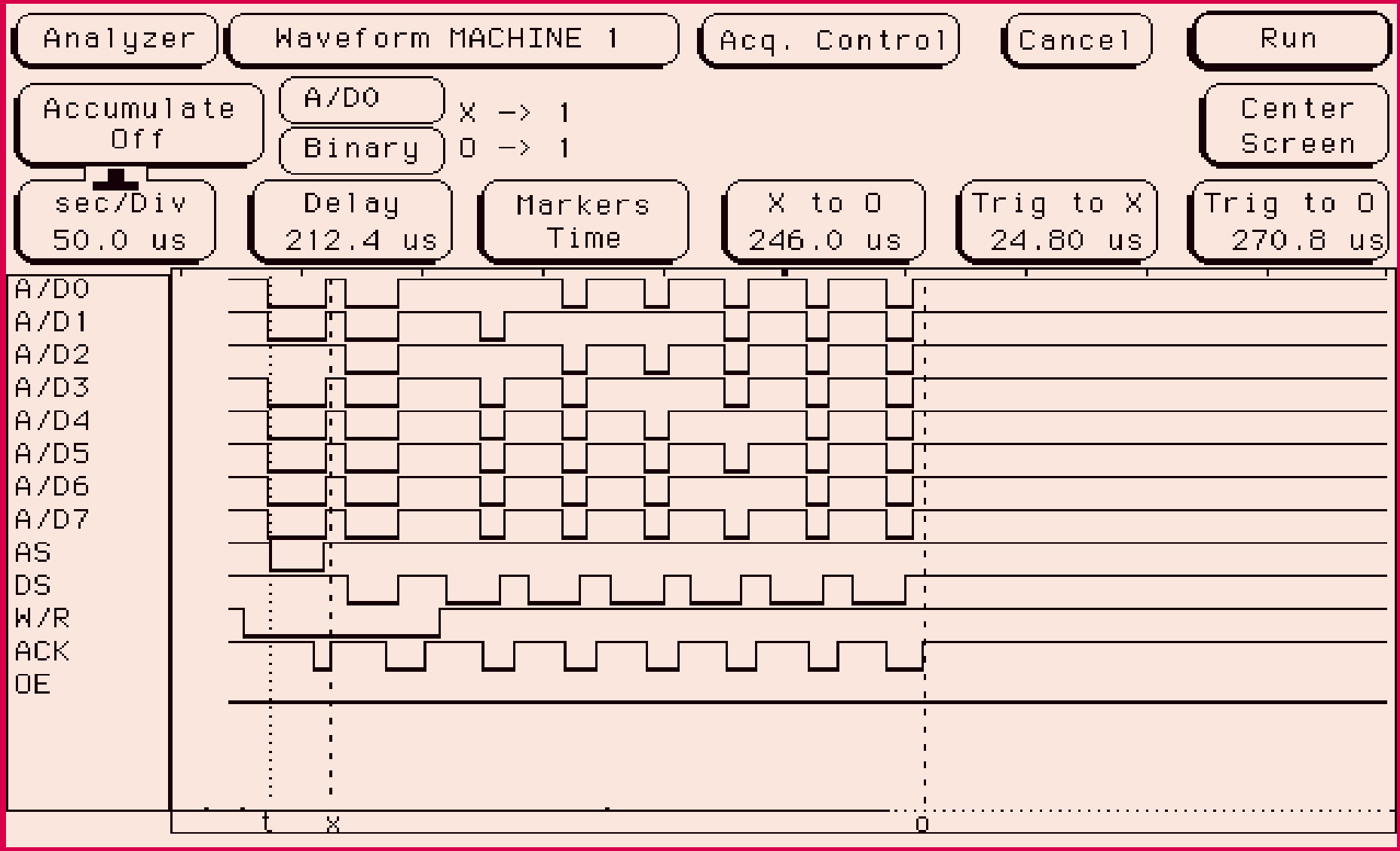
The original code for the ELMB has been substantially modified for our non-standard use of the ELMB.

All control and monitor parameters are represented by dedicated objects in an object dictionary.

Control parameters are configured using standard SDO (service data objects) message while real time data read from LV and HV modules are transferred from ELMB to DCS via multiplexed PDOs (process data objects)

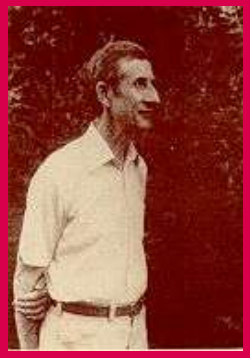
Our non-standard use of ELMB creates a rather large project.
Our CAN network will comprise some 88 ELMB nodes.

CUSTOM PROTOCOL AT WORK
(timing of the “read module” function for the HV card)



Time for somewhat controversial sense of humor and reflection ...

A good engineer is a person
who makes a design that works
with as few original ideas as possible



Freeman Dyson