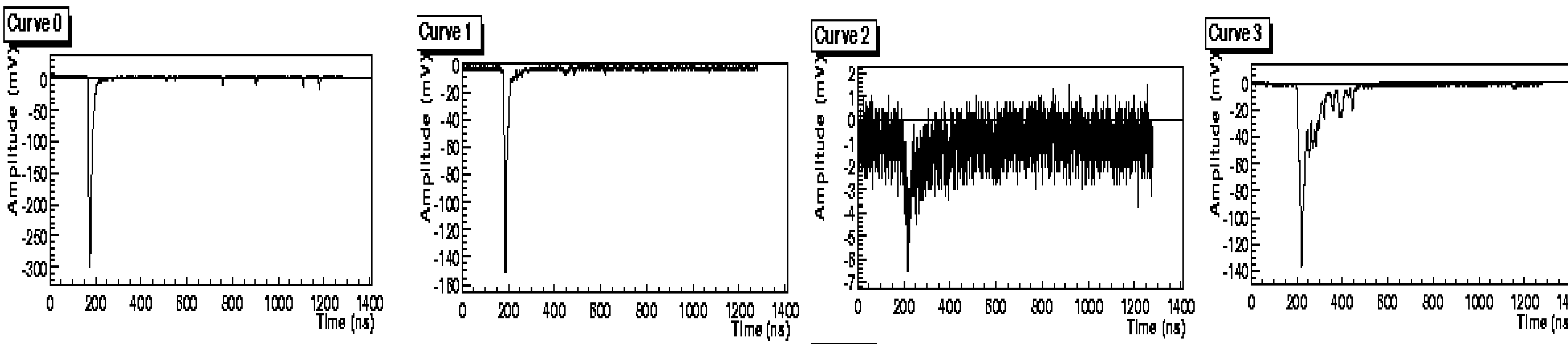
Very high dynamic range and high sampling rate VME digitizing boards for physics experiments.



(4 synchronous PMT data acquisitions at 2GS/s with a MATACQVME board)

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Introduction

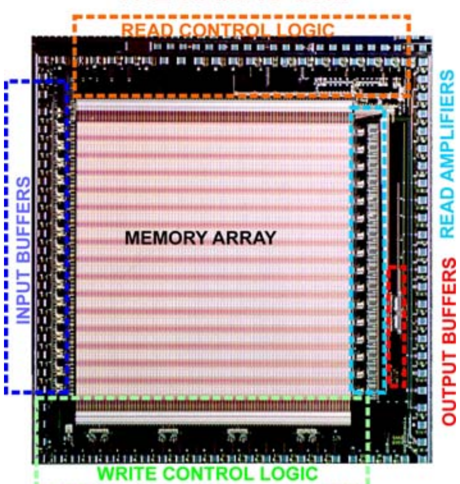
- **The idea**: replacing the oscilloscopes or the very expensive digitizers and improving the measurement quality when a very high sampling rate and a large number of channels is needed.
- **Basis of the study**: developing a new VME board with a minimum of 4 channels for fast data acquisition with high precision, low power and low cost.
- **The target numbers**:
  - **2 GigaSample/s.**
  - **Bandwidth >= 300MHz.**
  - **SNR: 12 bits (or 72dB) RMS.**
  - **1W maximum on each analog channel.**
- **Solution for the sampling**:

A NEW AND PATENTED FAST ANALOG MEMORY : "MATACQ".

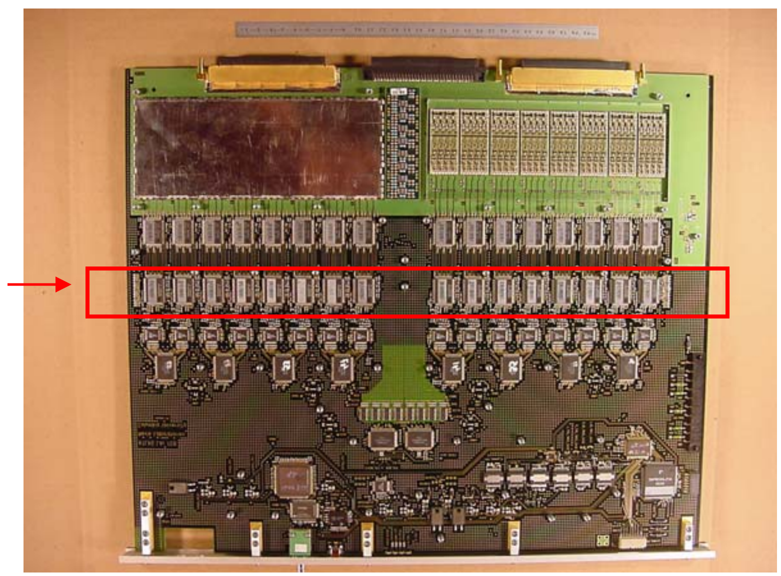
Our former experience.

- We had a long experience of 10 years in the analog memories.
- We co-designed and were in charge of the production of the 85,000 rad-hard analog memories for the ATLAS LARG calorimeter (DMILL process).
- The latter are 12-channel dual-port random access analog memories, with a depth of 144 cells in each channel.
- They were simultaneously written at 40MHz and read at 5MHz, yet with a SNR of 13.5 bits RMS (~80dB).

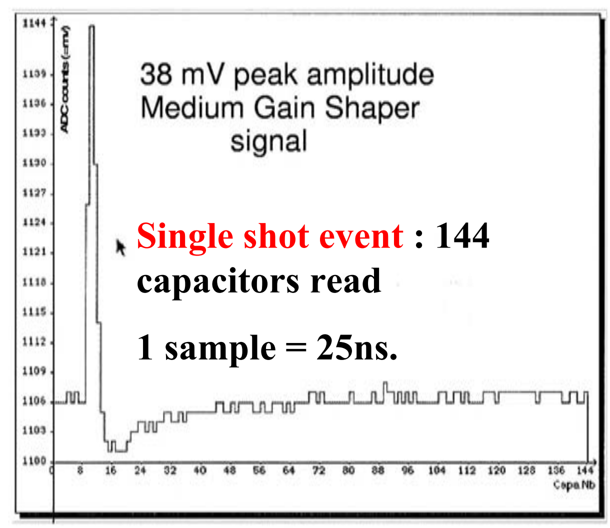
MICROPHOTOGRAPHY OF THE HAMAC CHIP



25000 transistors / 30 mm2



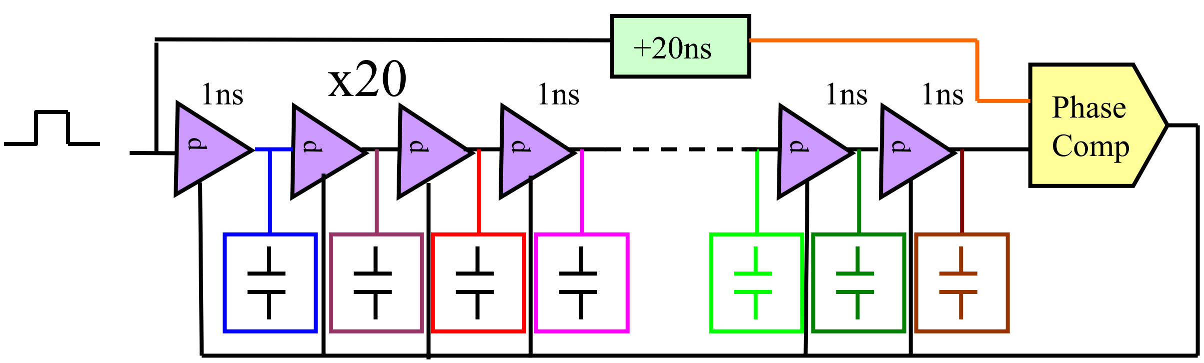
The ATLAS LARG 128-channel front-end board

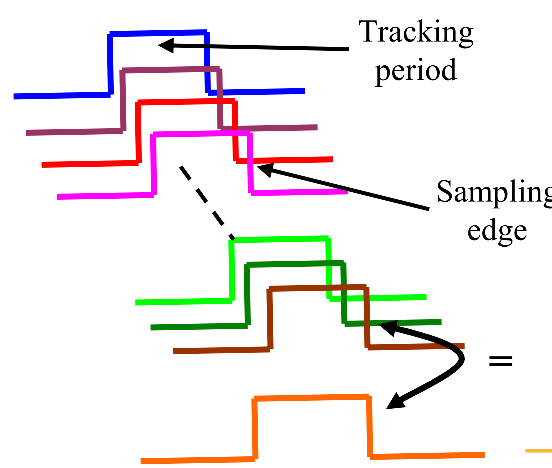


The new analog memory : MATACQ.

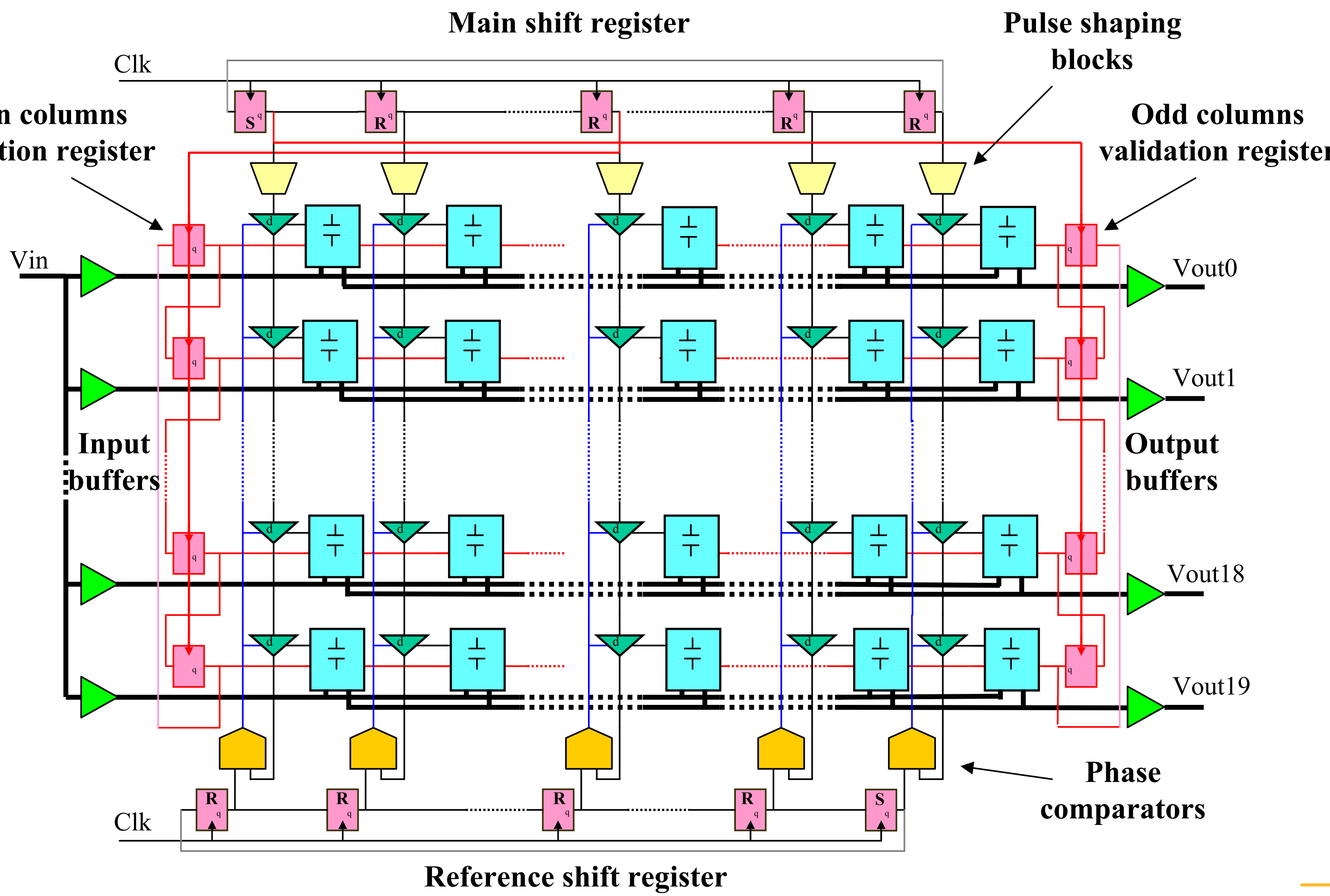
- Circular buffer of 2560 cells based on a innovative matrix structure (20 lines and 128 columns => see next slide).
- 2520 usable points.
- Both voltage writing and voltage reading to ensure the independence from the cell characteristics.
- One independent servo-locked DLL in each column to ensure a perfect sampling time precision.

Principle of the DLL: how to get 1GS/s with a 50MHz clock.





The new patented structure.



More details.

- The analog signal input is split and buffered into 20 independent lines to ensure no sampling crosstalk may take place.
- There is a possibility to mask the input of selected sampling lines, thus permitting to divide the sampling frequency by 2, 4, 5, 10 or 20.
- Acquisition is stopped by the arrival of a stop signal.
- The latter is derived from an asynchronous trigger signal.
- Said trigger signal is internally dated by a dedicated timing system with a precision (~25ps RMS) much finer than the sampling period (500ps at 2GS/s).
- The readout is made either from the first cell up to the last, or from the column where the acquisition was stopped => a partial and selective readout is possible.

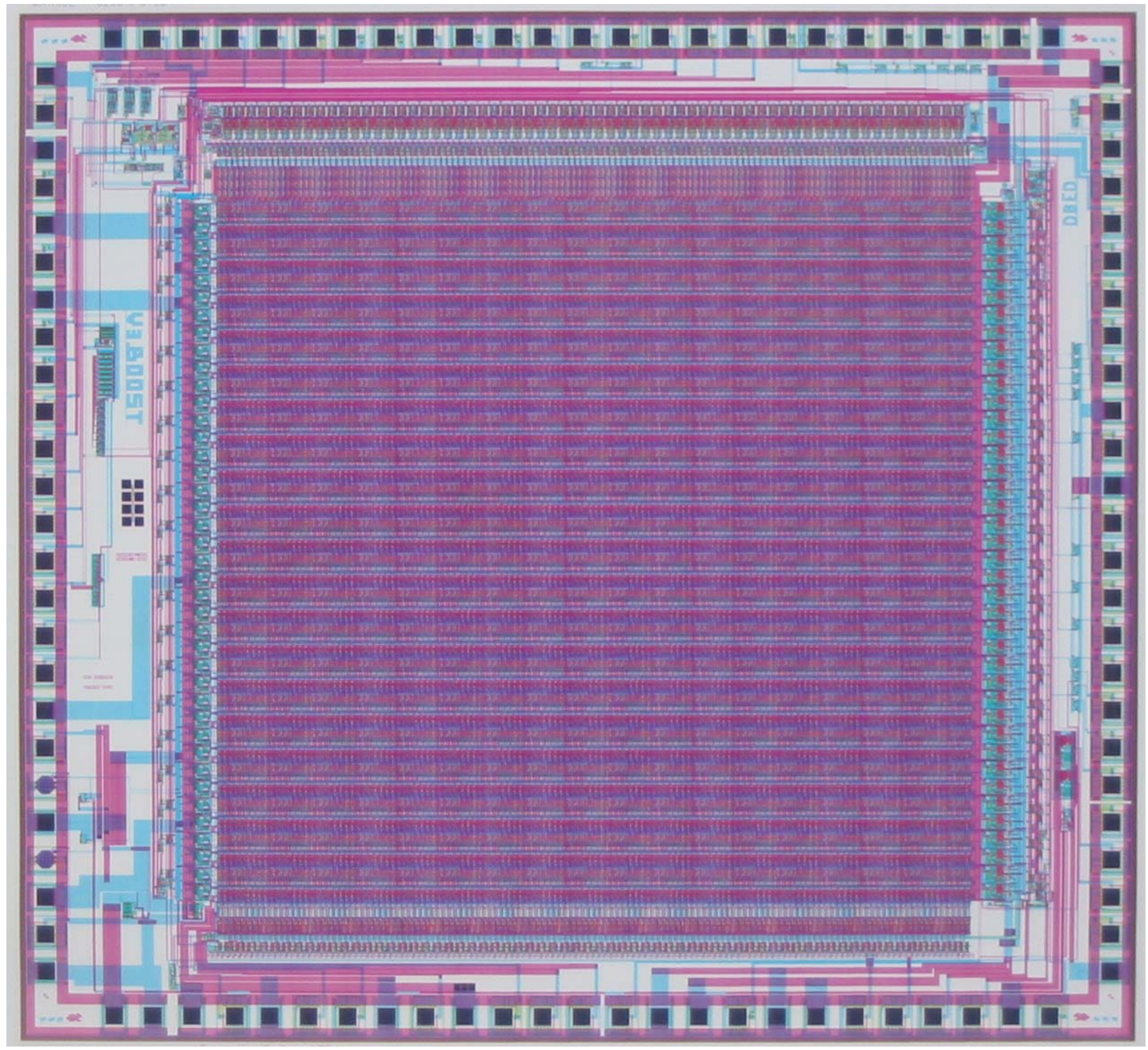
Still more …

- The available dynamic range is +-2V.
- The most difficult is to optimize the input bandwidth of the cell, including the input amplifier.
- The input buffer bandwidth thus the chip power consumption are actually programmable by software: 1W for 300MHz, 1/2W for 250MHz, 1/4W for 200MHz, below 100mW in stand-by.
- One specificity: there is one constant pedestal value per line (20 in total), which has to be calibrated once and subtracted by software after data readout.
- The current technology was the cheapest available up to now (AMS pure CMOS 0.8µm). But it's unfortunately becoming obsolete …

  => a new 0.35µm version is currently under design.

The chip layout.

- CMOS 0.8µm.
- All full-custom.
- 30 mm².
- 100,000 transistors.
- 100 pads.
- packaged in a PQFP 100 pins.



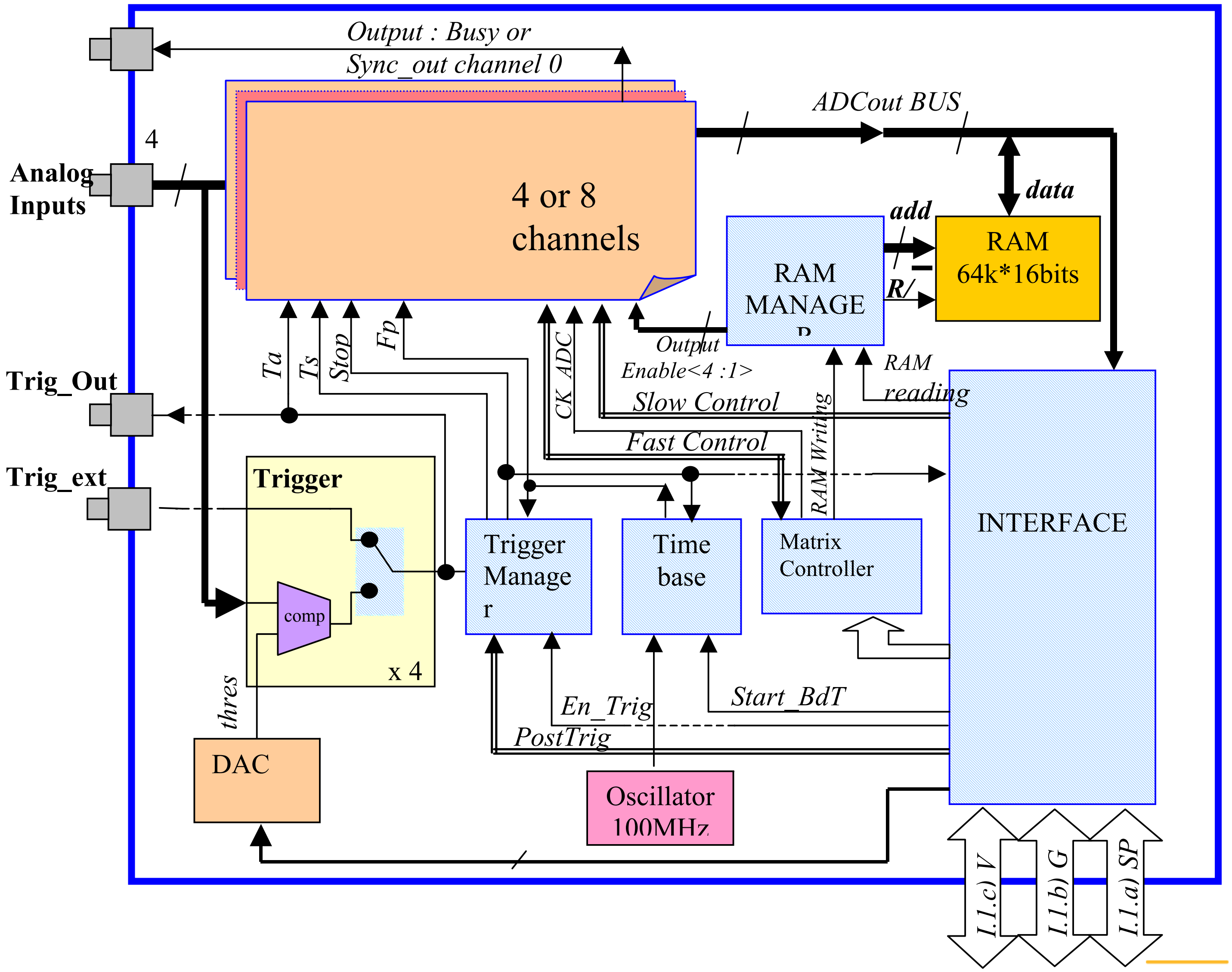
The MATACQVME board.

- The standard version of this board houses 4 analog channels (6U VME).
- An 8-channel version is also available (9U VME).
- It can be used alone or in parallel with any number of channels.

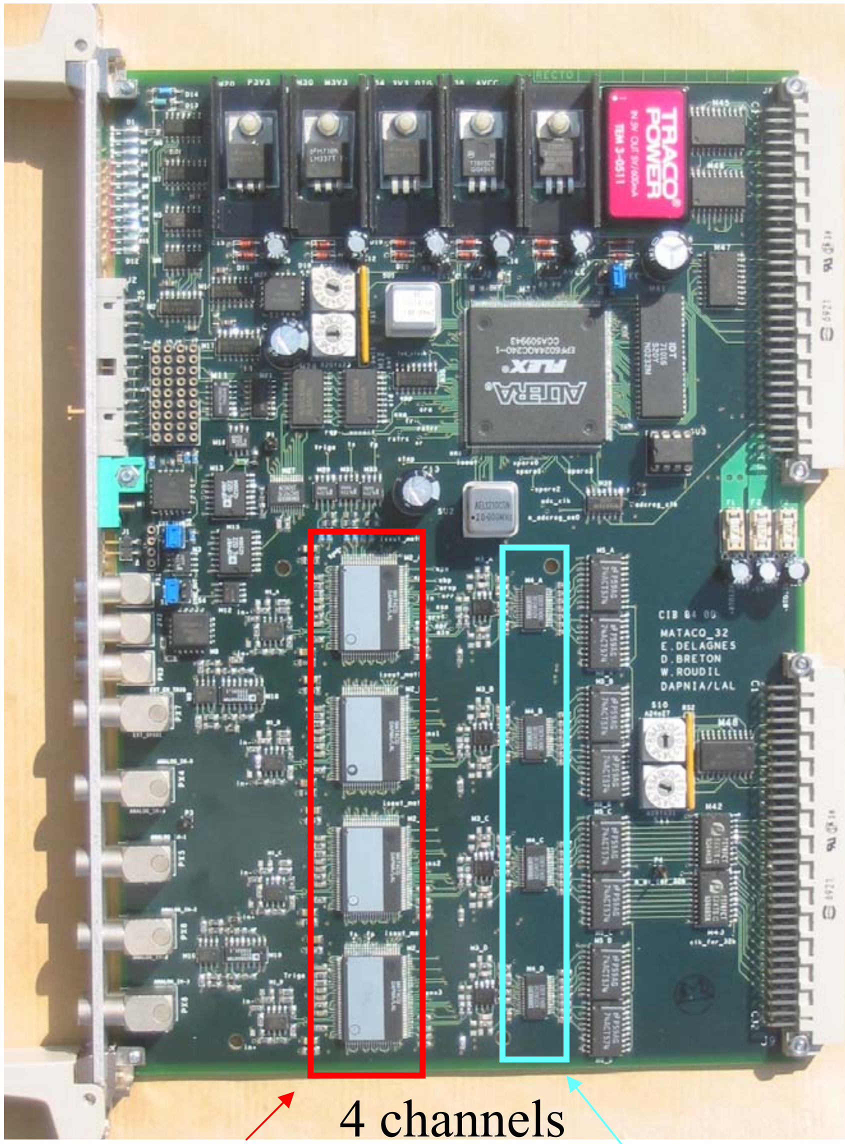
  => synchronization features for multi-board systems are implemented.
- It houses both a 32-bit VME and a fast GPIB interface (up to 3MBytes/s).
- Peak acquisition rates for 4 complete channels (2560 points each) vary from 80Hz in GPIB to 500Hz in 32bit-VME with block transfers.
- Acquisition can be performed in real time or equivalent time like with an oscilloscope.

Block diagram of the board.

- All the logics is integrated in a single Altera FPGA (in blue).
  - All the critical signals travel in low level and differential mode.



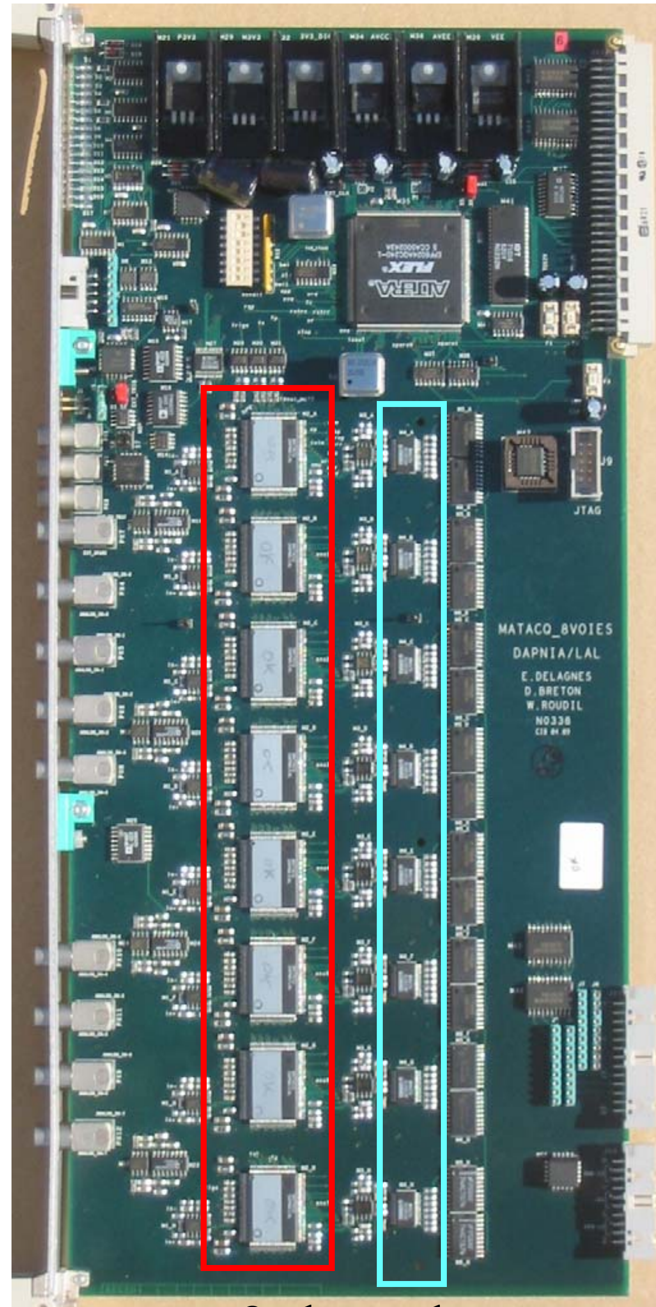
The boards.



4 channels

Analog memories

ADCs



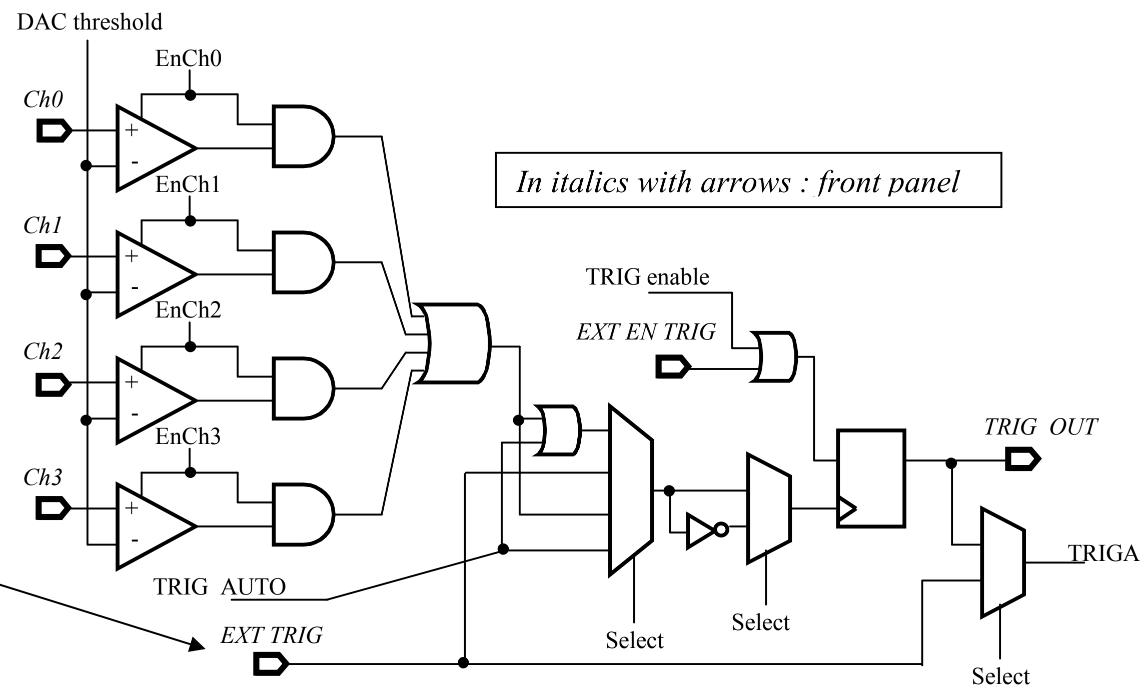
8 channels

LABORATOIRE DE L'ACCÉLÉRATEUR LINÉAIRE

cea DAPNIA

Trigger mode selection.

- Different trigger modes are available:
  - Internal: single (software), continuous, or deriving from a threshold on input signals.
  - External: NIM input.



The *EXT_TRIG* input can be used directly in order to allow the synchronization of any number of channels.

The acquisition sequence.

- Once the acquisition is launched by the user, and after a dead time of 100µs, it will run until a trigger is received.
- The latter will be precisely dated and after a user defined delay called post-trig (set in number of clock periods), acquisition will be stopped. This delay permits placing the data wherever aimed at in the 2500-point window (or even out of it).
- Analog data is then converted into digital over 12 bits and stored in the event RAM (this takes 650µs for 4 channels).
- A flag is then raised and/or an interrupt sent on the chosen bus to allow the software to perform the readout of the RAM. The latter can be selective thus very fast for every data can word be accessed directly.
- Then acquisition may restart …

The board main characteristics (1).

Input analog signals	
• Number of channels	4 or 8
• Input impedance	50 Ohms
• Dynamic Range	+/- 0.5V
• Bandwidth	300MHz
• Noise/signal ratio	> 12bit RMS (noise < 200 µV RMS)
• Harmonic distorsion	< -60dB for sinusoidal input at 25MHz
• LSB (digitization step)	0.25mV
• Integral Non Linearity	< 1 per mil
• Differential Non Linearity	< 0.5 per mil
Sampling	
• Max Frequency	2GS/s
• Min Frequency	1GS/s
• Time precision	60ps RMS (includes sampling and trigger)
• Depth per channel	2560 points (of which 2520 are usable)
Trigger	
• Threshold setting dynamic range	+/- 0.5V
• Threshold setting step	0.25mV

The board main characteristics (2).

Analog to Digital Conversion

• Conversion frequency	5MHz (4 channels), 3MHz (8 channels)
• Resolution	12 bits
• Time to empty the matrices into the RAM	650µs (4 full channels), 1ms (8 channels)

Acquisition

• Acquisition rate (VME)	Up to 500 acq/s over 4 full channels
• Acquisition rate (GPIB)	Up to 80 acq/s over 4 full channels

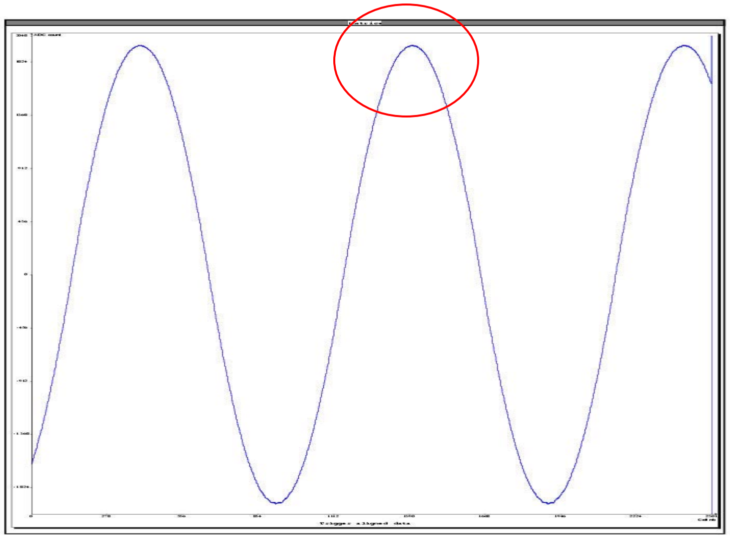
Front Panel Digital Signals (TRIG_OUT, SYNC_OUT, TRIG_EXT)

• Standard	NIM (negative logics)
• Input Impedance	50 Ohms

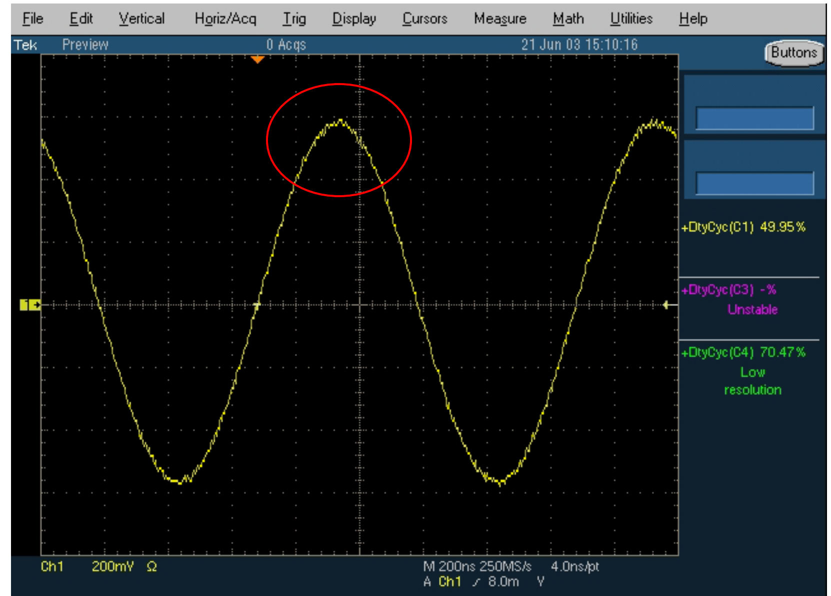
Power Supplies

• Consumption on +5V	0.5A
• Consumption on +12V	typ 1A (4 channels), typ 1.5A (8 channels)
• Consumption on -12V	typ 1A (4 channels), typ 1.5A (8 channels)

Comparison MATACQVME/TDS 7104 (25,000$)

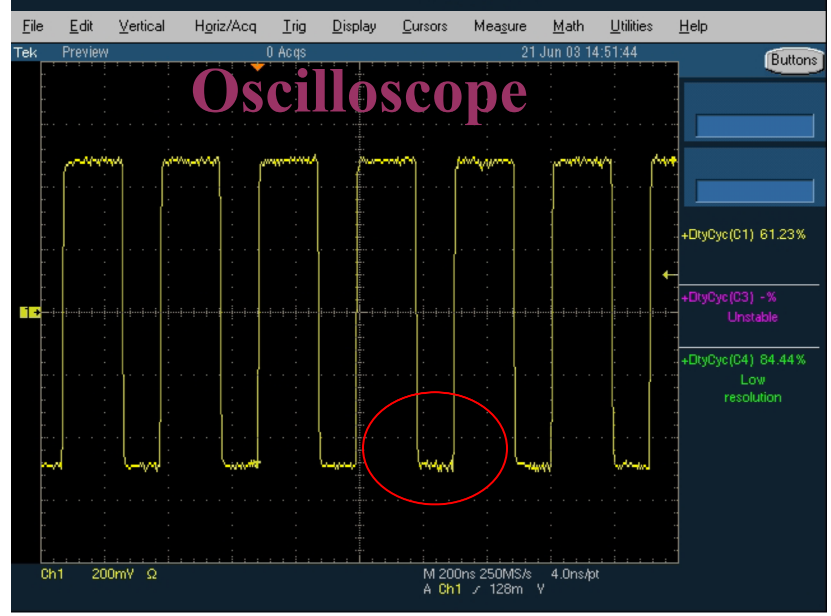


Sinus
1MHz
~1Vcc



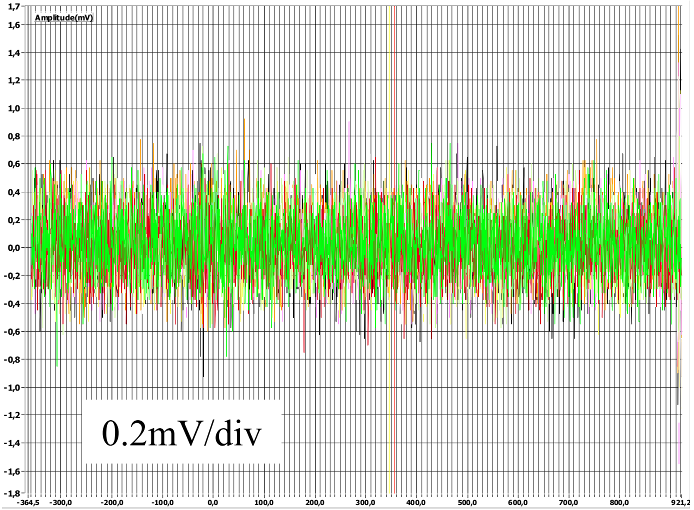
MATACQVME

Square
5MHz
~1Vcc

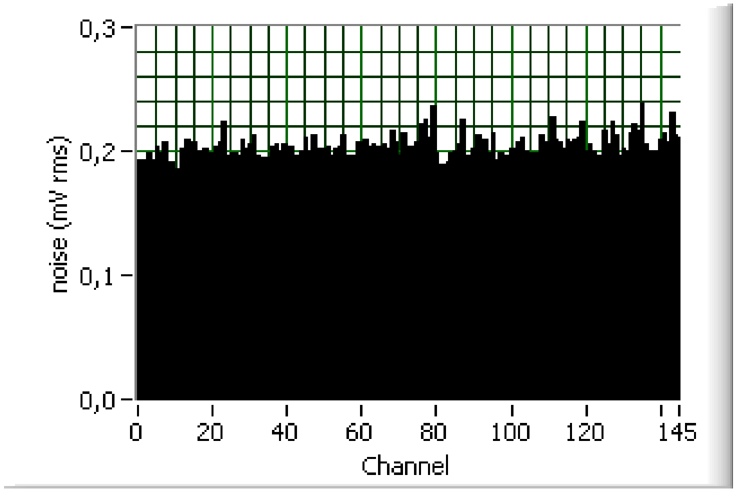


Some characterizing plots.

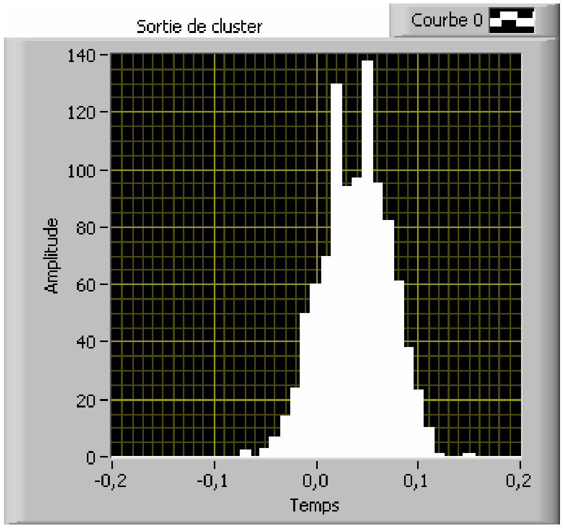
One shot pedestal distribution of 160 channels in the same crate.



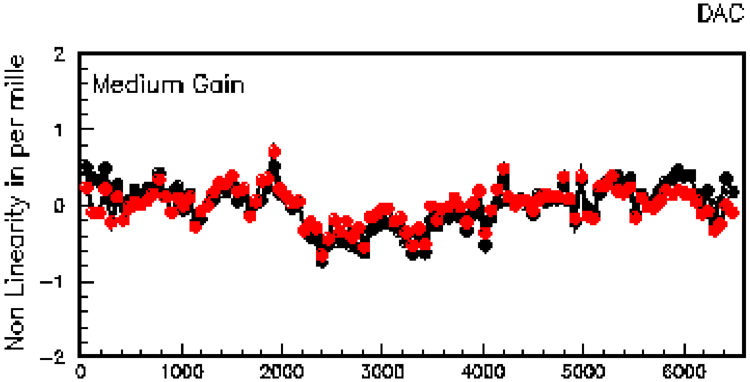
RMS of the pedestal distribution (~200µV).



Inter-channel time alignment (RMS = 23ps).

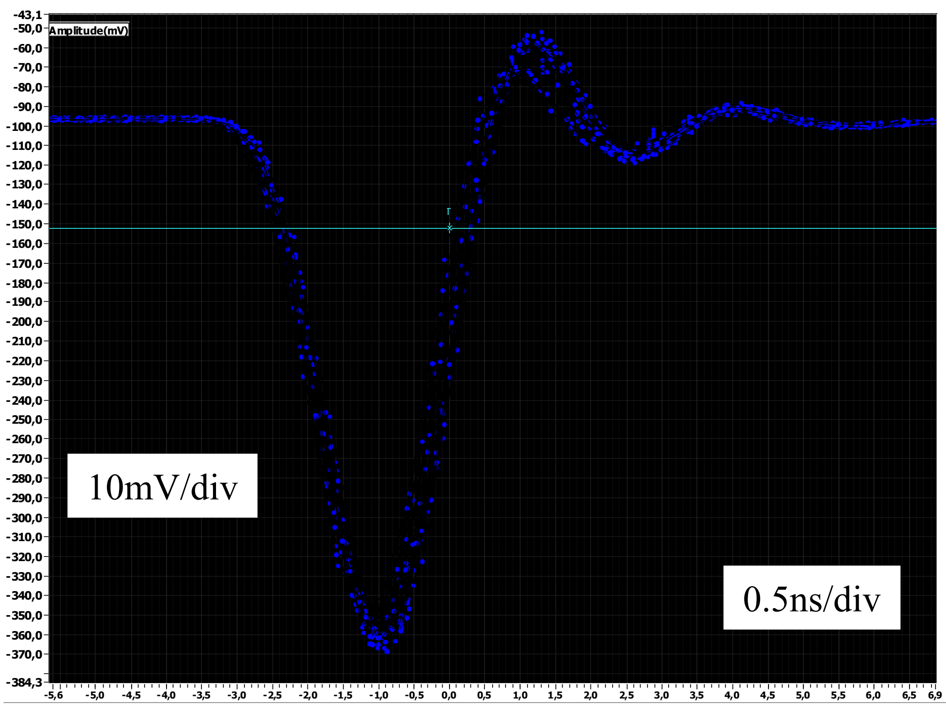


Integral non-linearity over the whole range.

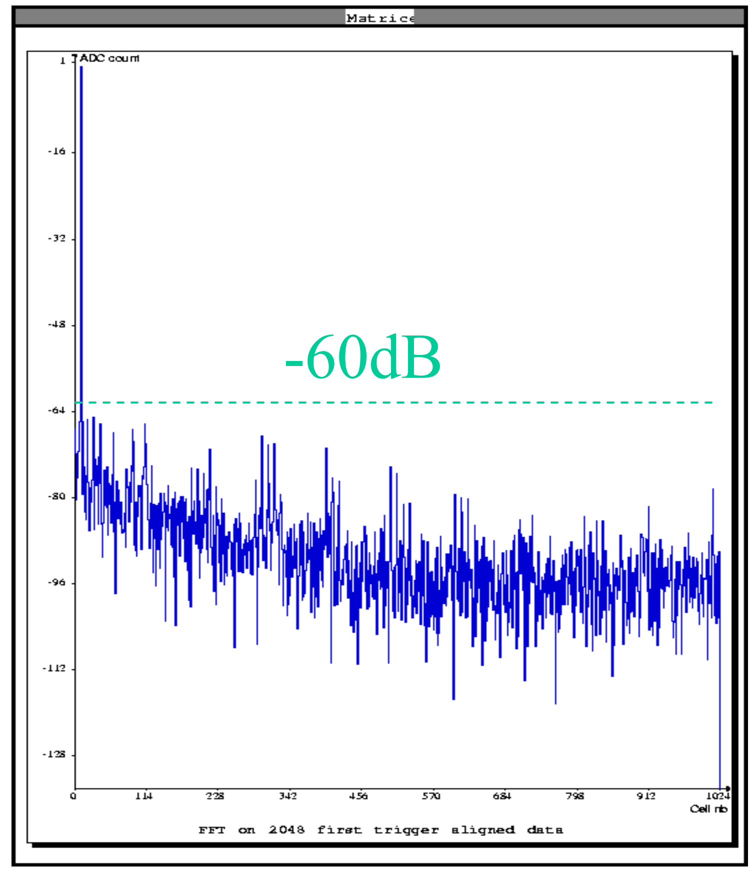


Equivalent time and real time FFT.

A 2ns-wide repetitive pulse recorded in equivalent time.



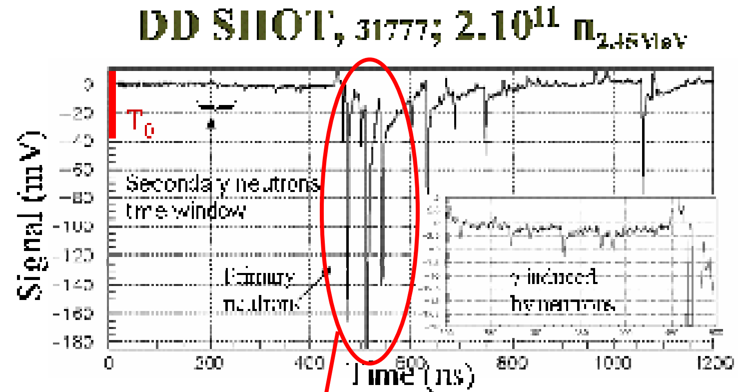
FFT on a single acquisition of a 10MHz sine wave.



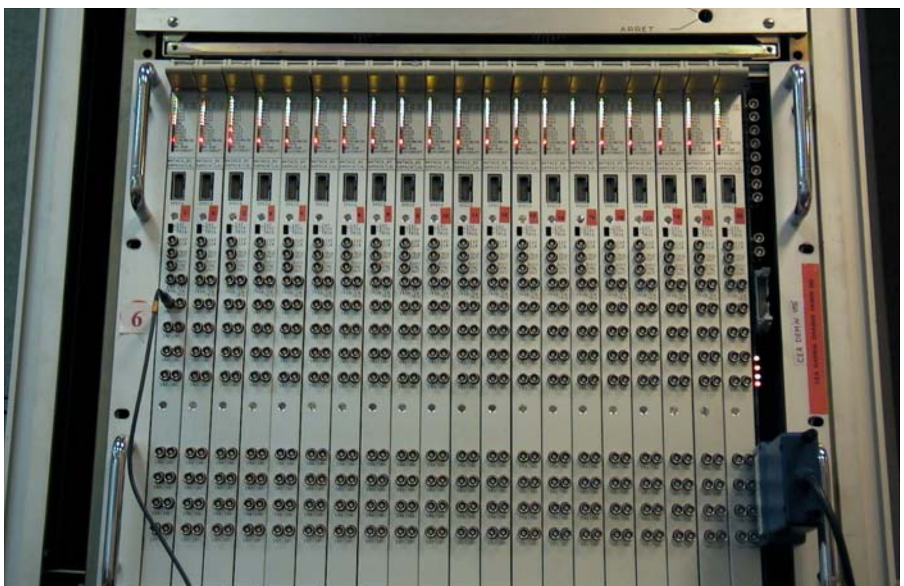
The MATACQVME boards in DEMIN.

- **Goal: detection of neutrons, Micromegas detector.**
- **Time of flight spectrometry => chronometry.**
- **Eventually 1000 acquisition channels.**
- **LabView acquisition with GPIB !!!**

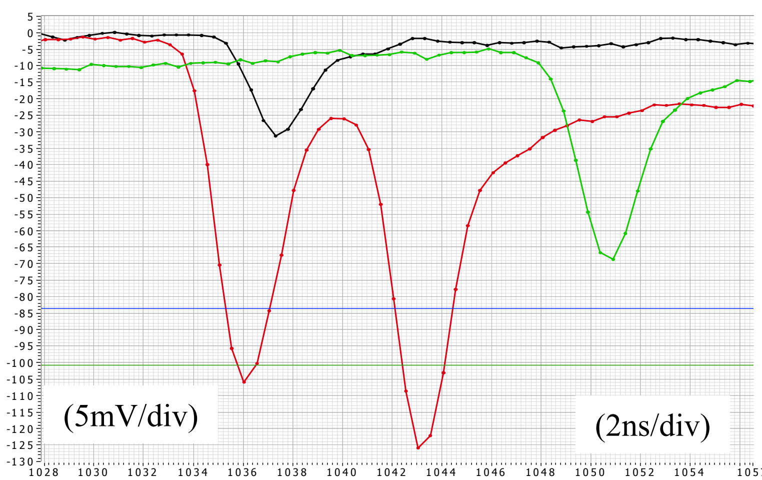
⇒ Test of a 32-channel prototype detector + data acquisition in May 2003 on Omega (Rochester) => ***setting up of a demonstrator system with 160 channels.***
Partial tests in May 2004, complete tests during the fall of 2004.



A zoom on signals …



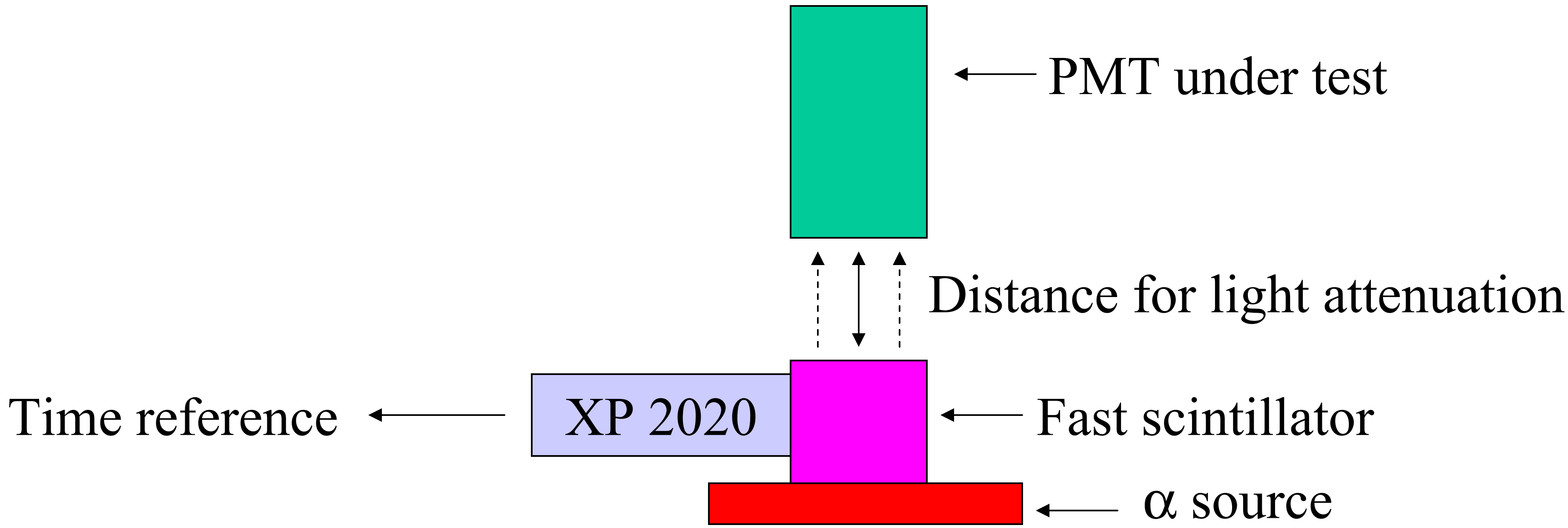
A 160-channel 2GS/s 12-bit digitizer in a single crate !



Power of the solution: the ability to deal with pile-up.

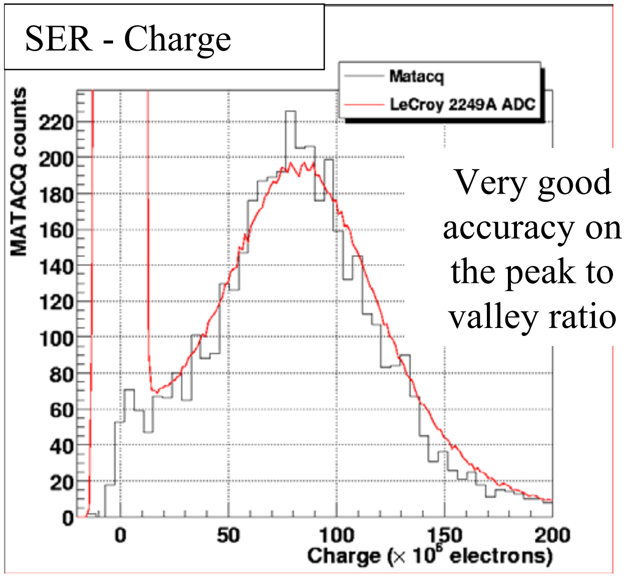
LabView interface.

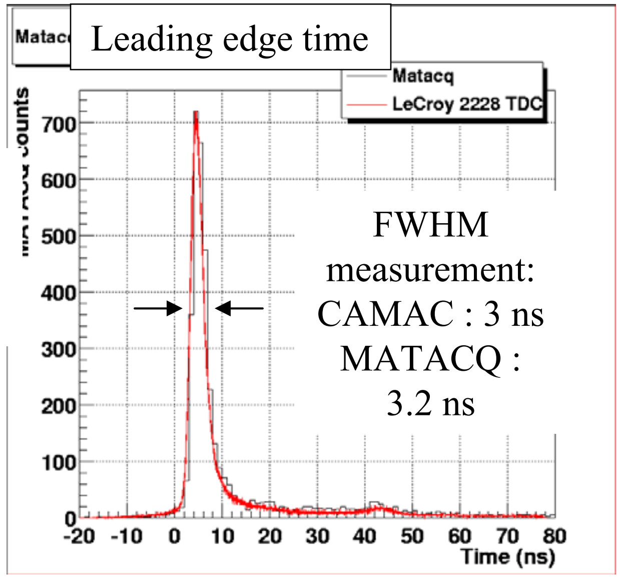
Fine PMT characterization at IPN Orsay (setup).

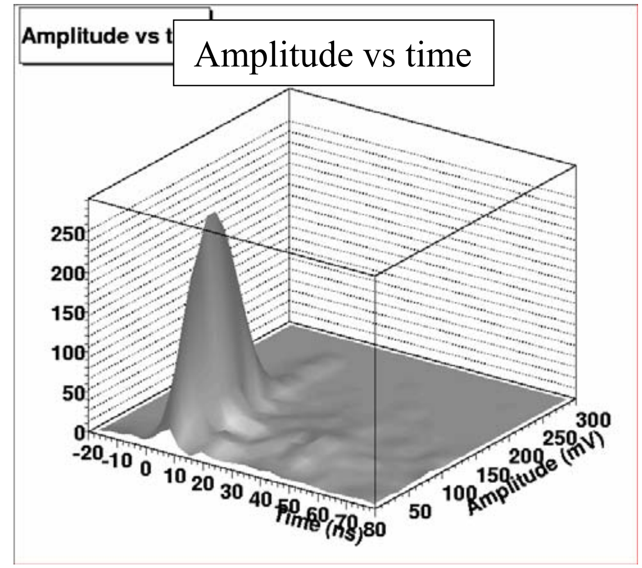


- <u>Measurements</u>:
  - Transit time spread, single electron response, late pulses (type I afterpulses).
- Fast scintillator.
- Fast PMT (Photonis XP2020) used as a time reference, with around 100 photoelectrons.

Fine PMT characterization at IPN Orsay (results).





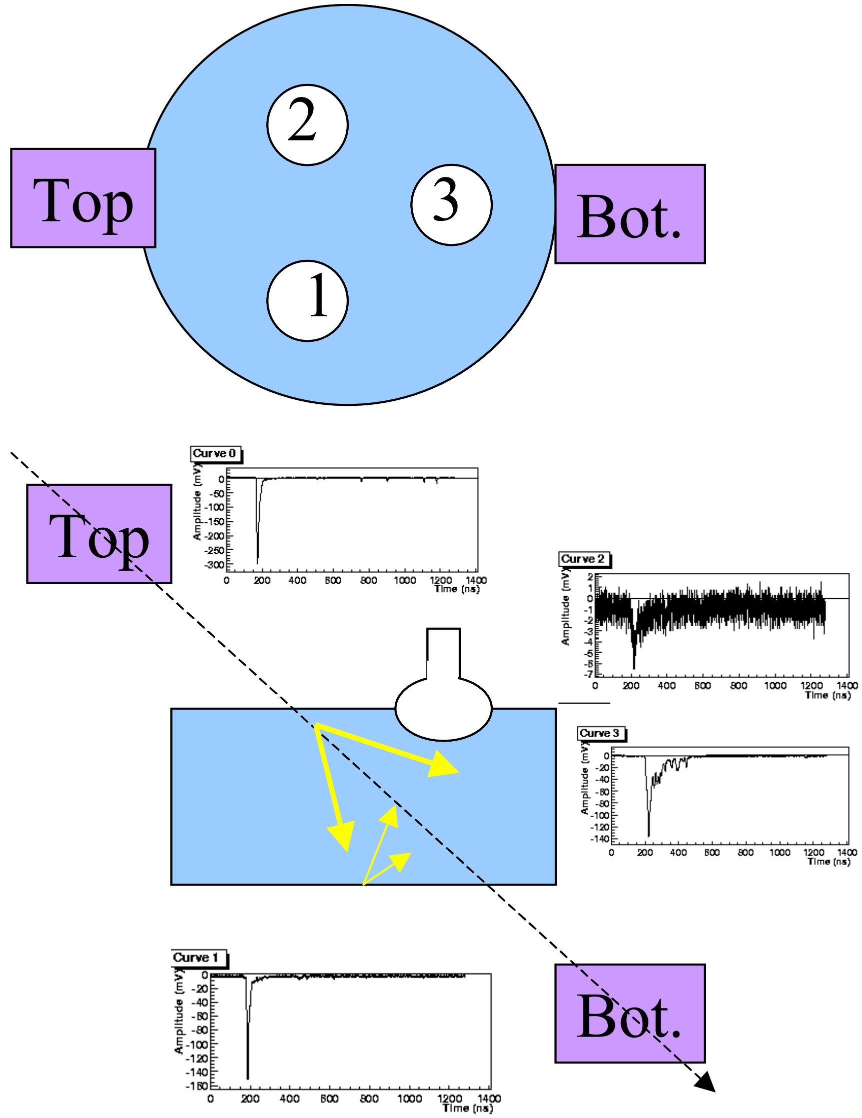


- **Single- and multi- pulse characterization**
- Single electron response: charge and amplitude (compared with a LeCroy 2249A charge ADC, 0.25 pC/bin, 80 ns wide gate)
- Transit time measurement (compared with a LeCroy 2228 TDC, 50 ps/bin)
- Amplitude vs time for all the pulses in one single electron response (photocathode and first dynode characterization)

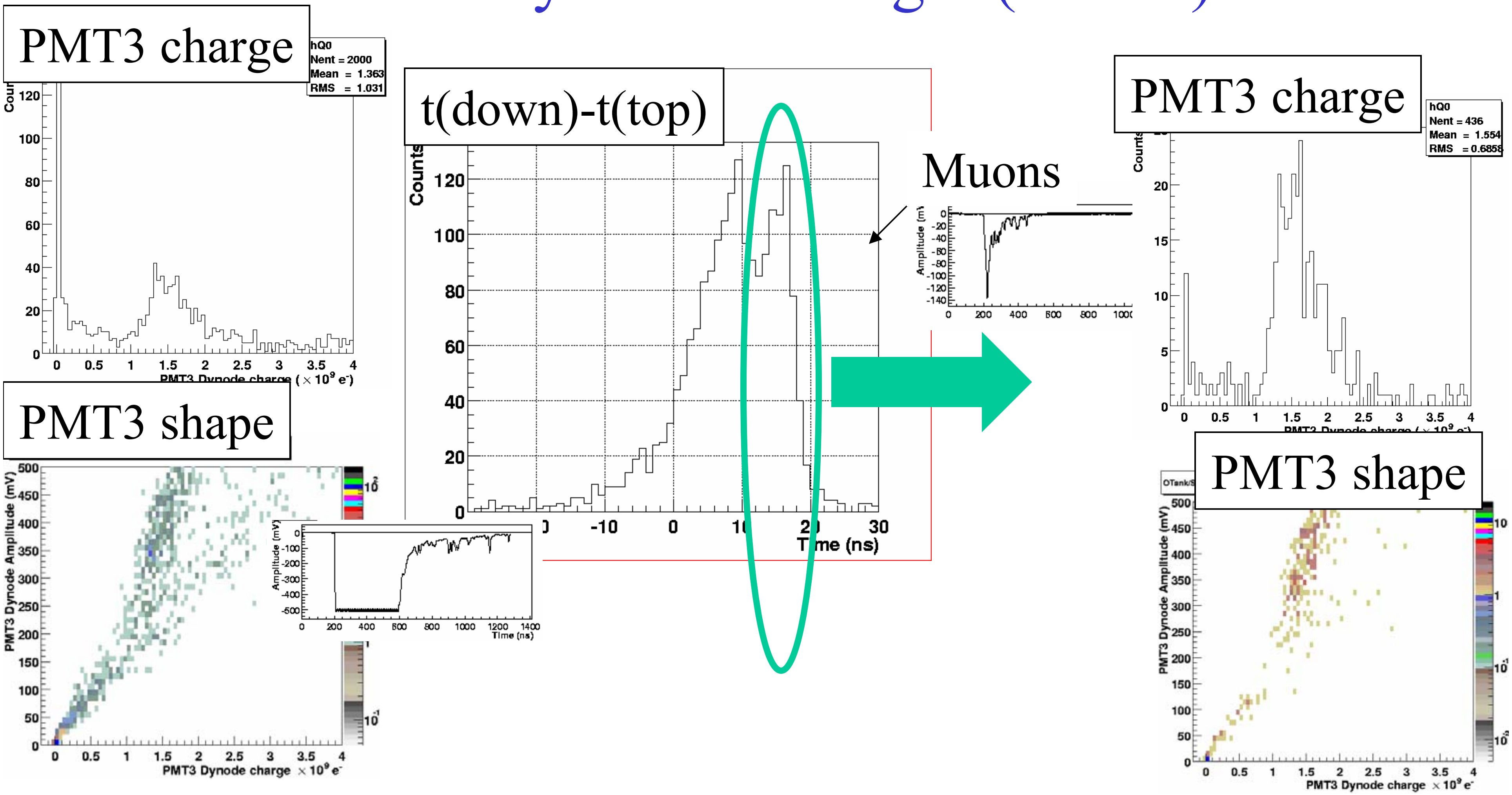
IPN Orsay tank for Auger (setup).

- 12 m^3 water tank (cf. Pierre Auger Observatory).
- Cherenkov light diffused.
- 3 hemispherical photomultiplier tubes.
- Trigger: scintillator placed above and under the tank to study a selected direction of incoming particles.
- Signal: large dynamic range (single muon to air showers), covered by two outputs per tube (one standard output + one with a gain of 32).
- Signal duration: 100 ns for single muons to several 100ns for multi-muon and air showers.
- Total of 8 synchronous channels

$\Rightarrow$ perfect adequation for an 8 channel MATACQVME board.

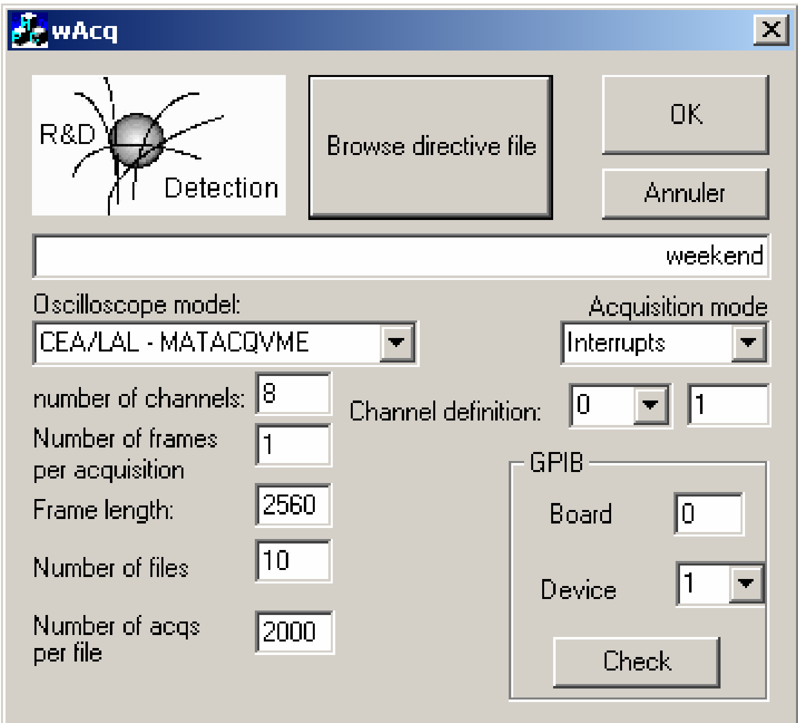


IPN Orsay tank for Auger (results).



- Arrival time calculated by interpolation on the leading edge (CFD equivalent).
- Analysis allows to discriminate muons from showers and other physical events.
- Shape (decay time) studied with the amplitude versus charge plot.

A graphical user interface.

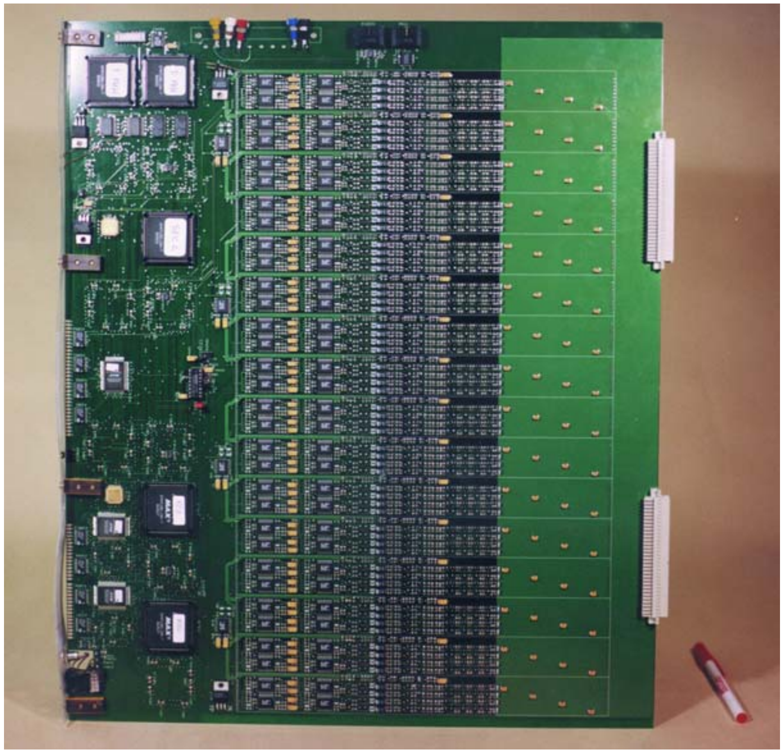


- Designed for small systems at IPN Orsay.
- Developped in C++.
- Running under MS Windows, for GPIB.
- Acquisition speed (8 channels):
  - Recording on hard disk: 12 evts/s.
  - Without recording: 15 evts/s.
- Acquisition sequence defined through the form or by a directive file (text).
- Possibility to program software conditions for recording through the directive file.
- Compatible with some digitizing oscilloscopes.
- Extendable (data source and data processing) because of object oriented programming.
- Available data processing: time, charge, amplitude, FFT, wavelet transform, correlation, etc…

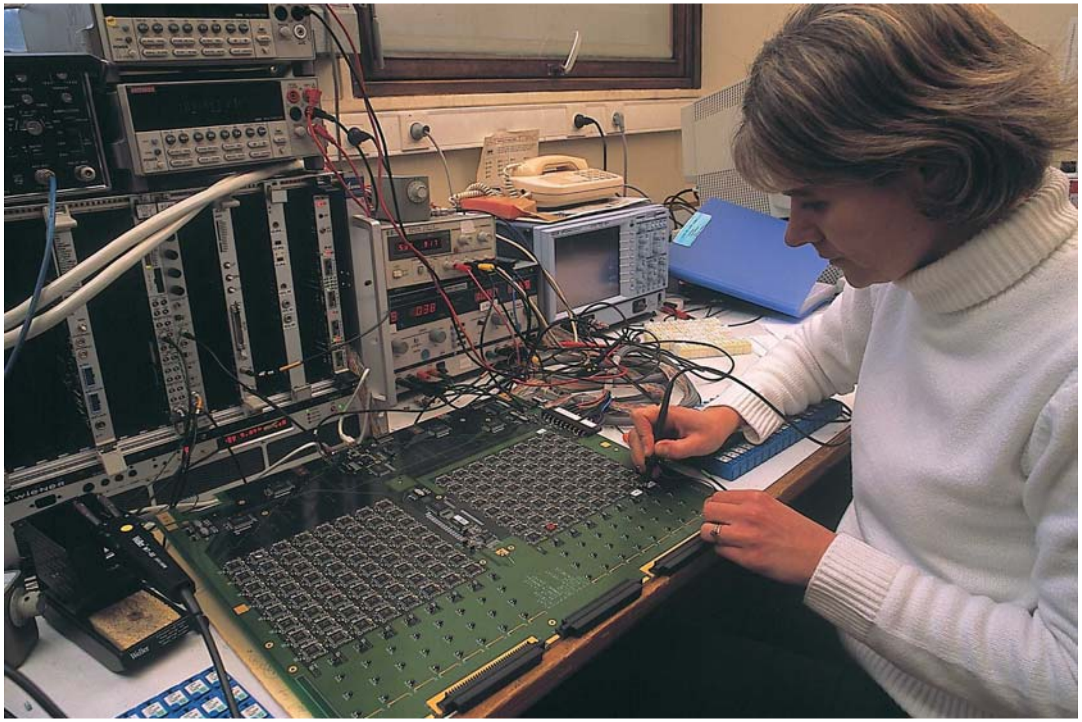
<u>Contact</u>: Bernard Genolini (genolini@ipno.in2p3.fr)

Serial test of ATLAS LAR calibration board at LAL.

- This board produces 128 LAR-like pulses with a dynamic range of 16 bits.
- Formerly, an usual 12-bit ADC was used for the test but there were problems of channel inter-calibration which forced our colleagues to also make use of an oscilloscope to observe the whole shape and measure the relative timing.
- Now with the MATACQVME board, they get all the necessary information in a single acquisition, and can even measure the onboard pulsers' jitter.



The board.



CNRS photothèque – R.Lamoureux

The test bench.

Some other applications …

- **CMS (CERN)**: shape measurement of the calibration laser pulse for the ECAL.
- **Nançay observatory**: detection and measurement of particle showers in the radio-frequency domain.
- **CAST (CERN)**: detection of solar axions. Energy measurement and pulse shape discrimination. One board has therefore been working continuously over the whole last year.
- **GANIL (Caen)**: particle identification with semiconductor detectors via pulse shape discrimination.
- **Soon**:
  - PMT cosmic test bench (GAM Montpellier).
  - Recoil detector (timing at 100ps in nasty environment and heavy pile-up).

Conclusion

- From above, the board clearly addresses three main types of applications:
  - Test benches for fast detector characterization
  - Pulse shape identification
  - Timing measurement in very high rate or noisy environments.
- This can be envisaged even for a large number of channels.
- A detailed documentation is available on request.
- As described, acquisition software has already been developed in different labs.
- **Current and future developments (with 0.35µm technology for the chips):**
  - Designing an evolution of the memory structure targeting 5GS/s and 500MHz.
  - Getting more points in depth.
  - Increasing the readout speed and selectivity.
  - Integrating the Analog to Digital conversion inside the chip.
  - …
- **Important information:** the 4-channel board described here will soon be distributed by CAEN under the reference V1729 (see them next door).