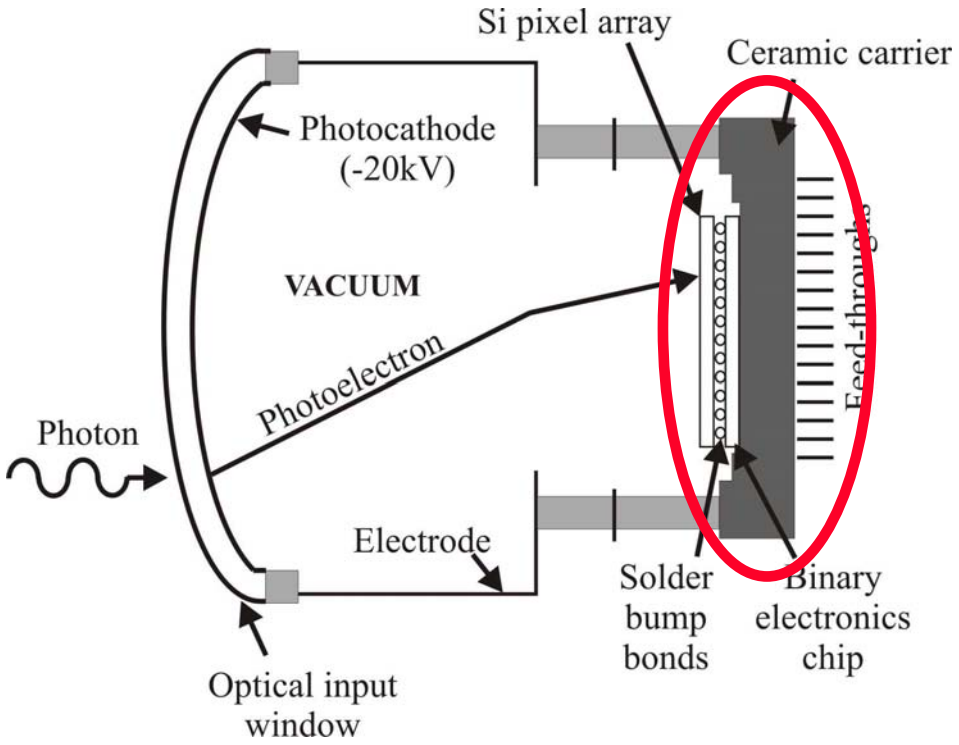
Readout of the LHCb pixel hybrid photon detectors

Ken Wyllie on behalf of the LHCb collaboration and industrial partners

- The pixel hybrid photon detector (HPD)
- Requirements for the electronics
- Design of the pixel chips
- Test results
- Design of the sensors
- Bump-bonding and packaging
- Conclusion

HPD details and tests presented by Laura Somerville earlier today

The pixel hybrid photon detector

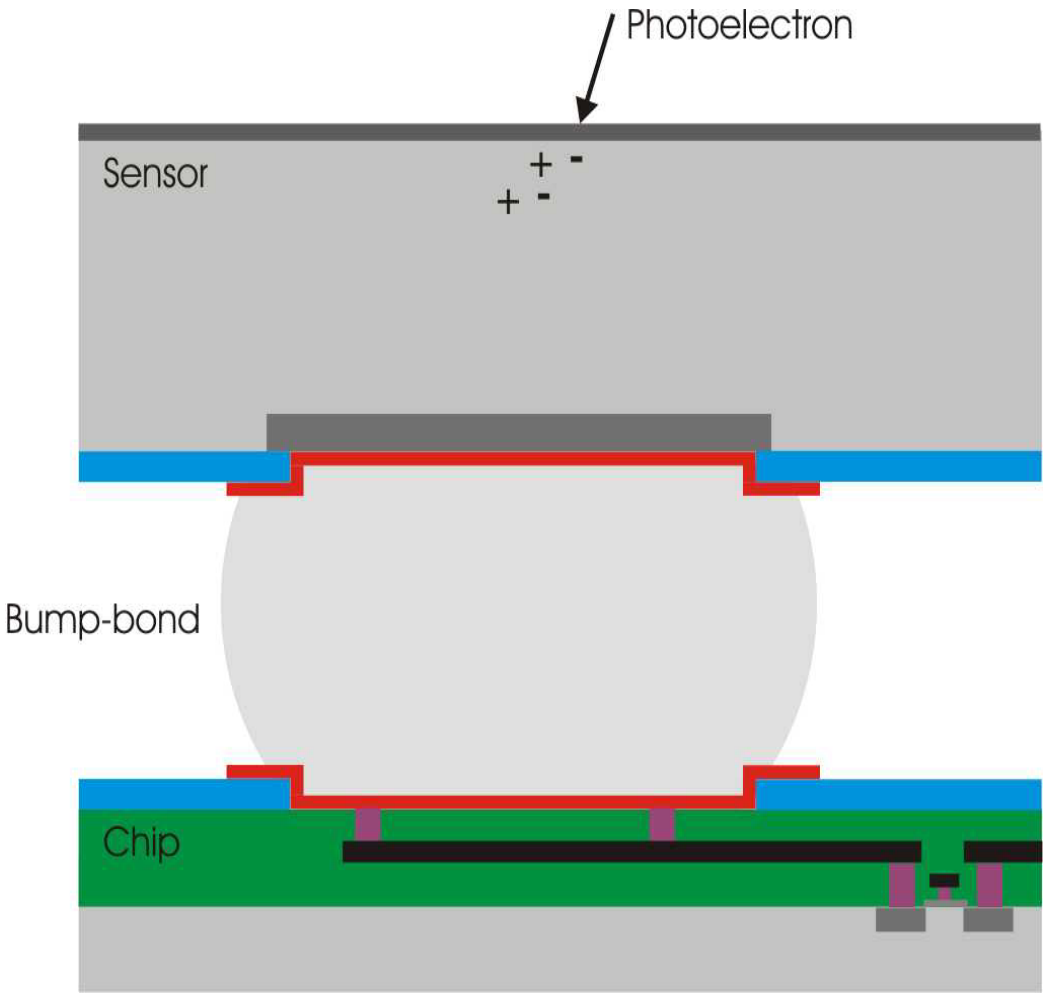


Electronics inside HPD:

- **Low noise (low capacitance)**
- **High channel density possible (data processing inside)**

~ 500 HPDs will equip the LHCb RICH

Hybrid pixel detector



Requirements for the electronics

- Low noise – pattern recognition
- Low & uniform detection threshold ~ 2000e^- (signal <= 5000)
- 25ns time precision (LHC)
- 500μm x 500μm channel size (factor 5 demagnification)
- 16mm x 16mm active area
- 4% maximum time occupancy
- External trigger at ~ 1MHz
- Compatible with HPD manufacturing

Design choices:

Physics performance not enhanced by resolving 1 or 2 or 3 photoelectrons

$\Rightarrow$ choice of binary architecture (0 or 1)
$\Rightarrow$ all digital I/Os – try to make it plug-and-play!

Design of the pixel chip

History: Omega 1, 2, 3
ALICE1test (use of radiation-tolerant layout)
ALICE2test (0.25μm CMOS & radiation-tolerant layout)

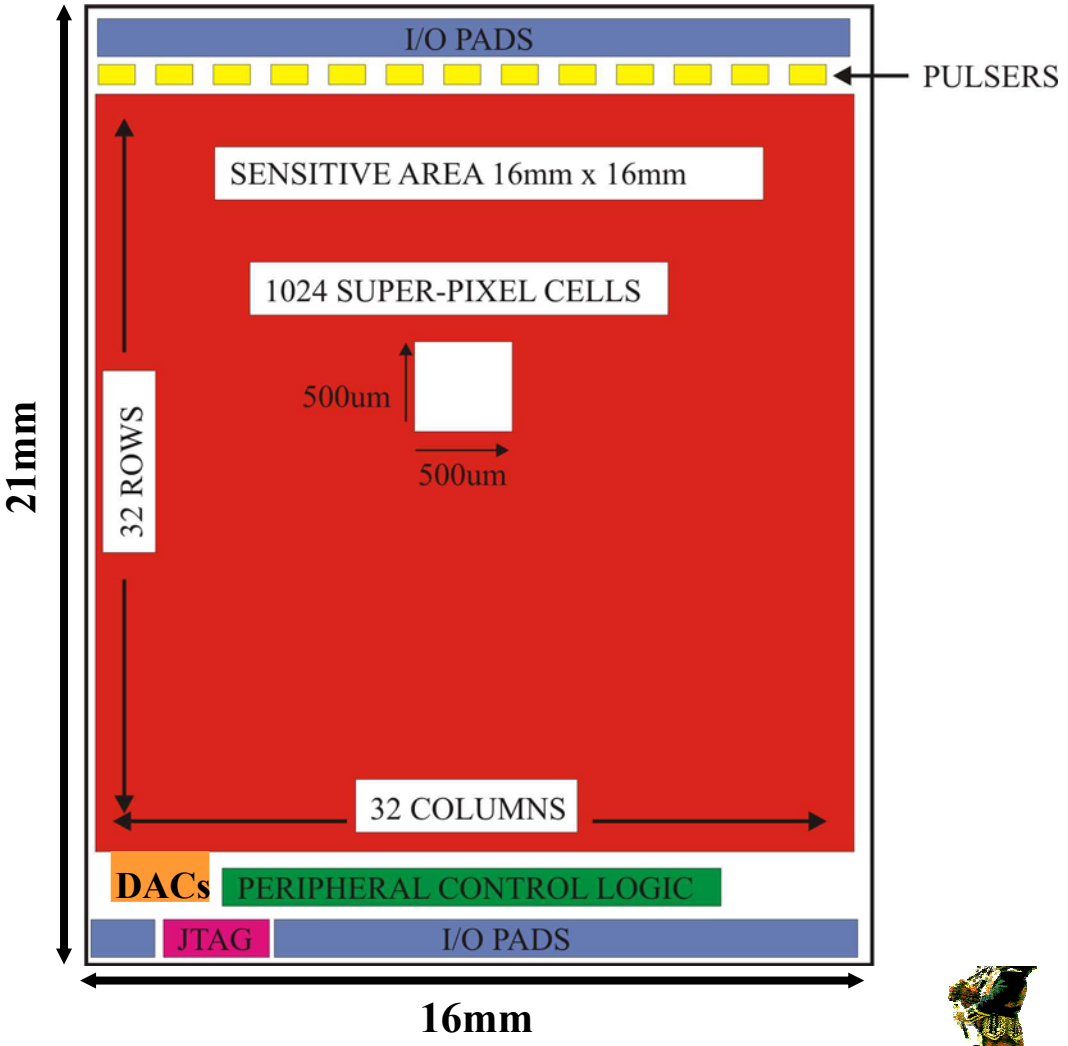
ALICE1LHCB (2000): full scale pixel readout chip
two applications, chip configured appropriately

ALICE happy LHCb almost happy

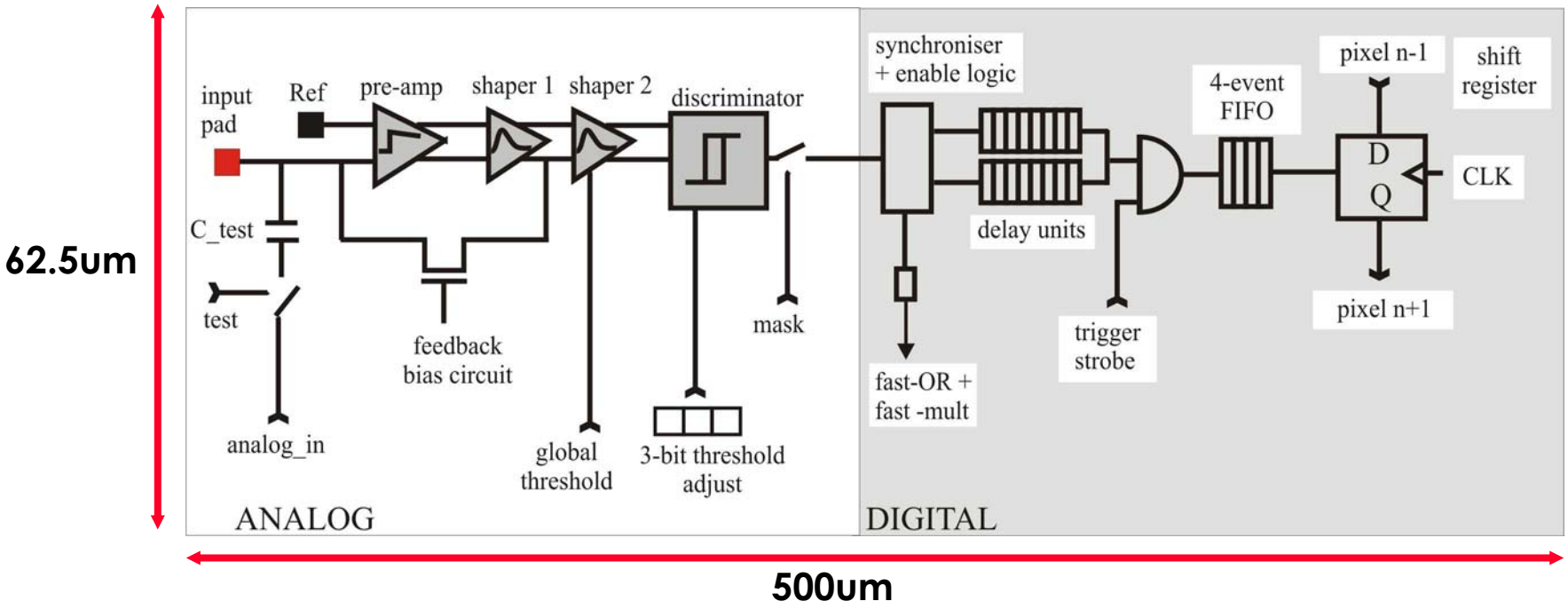
LHCBPIX1 (2001): dedicated to LHCb

LHCBPIX1 chip

- Commercial 0.25μm CMOS process
- 6 metal layers
- Radiation-tolerant layout
- 13 million transistors
- 1.8W total power (40MHz clk, 1MHz trig)
- Current-starved logic
- Internal DACs for biasing



Pixel Cell Description

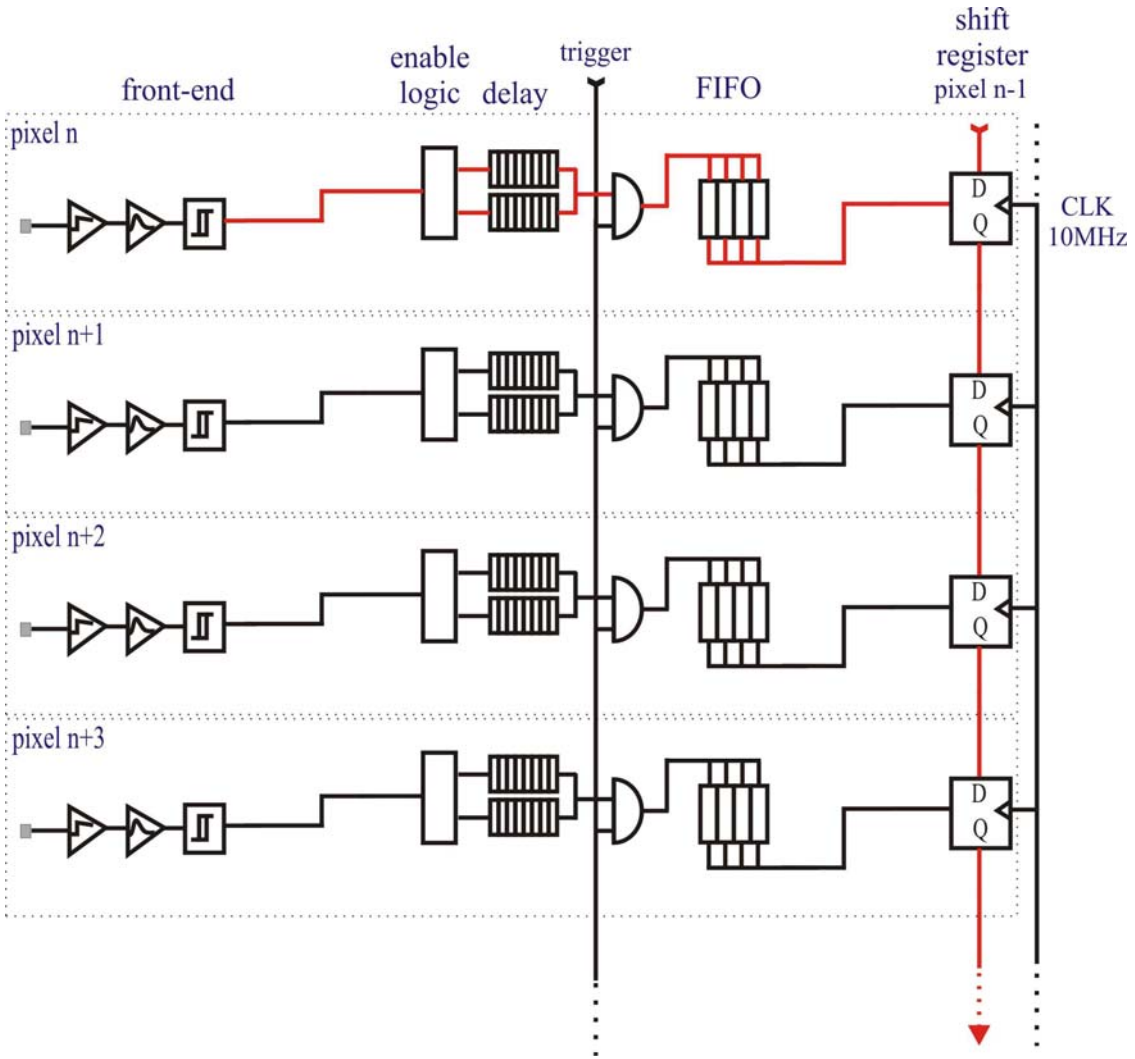


One super-pixel (500um x 500um) = 8 pixels (62.5um x 500um)

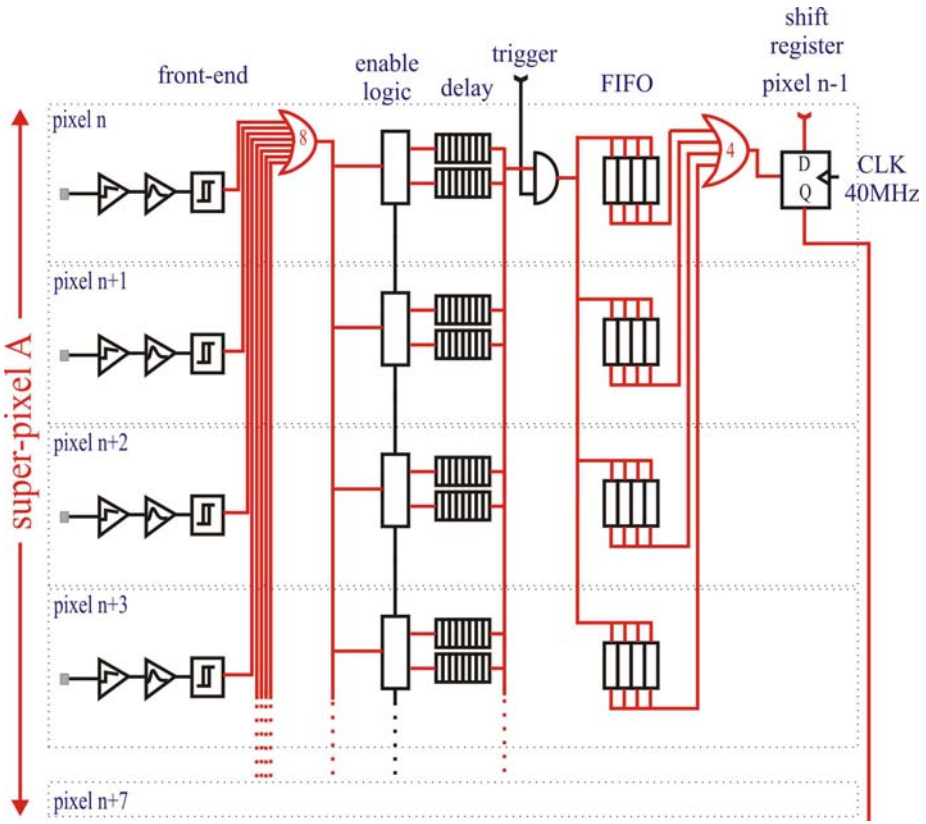
User can select:

1. ALICE mode = 8192 pixels
2. LHCb mode = 1024 super-pixels

ALICE mode


front-end
enable
logic
delay
trigger
FIFO
shift
register
pixel n-1
pixel n
pixel n+1
pixel n+2
pixel n+3
D
Q
CLK
10MHz

LHCb mode



Advantages:

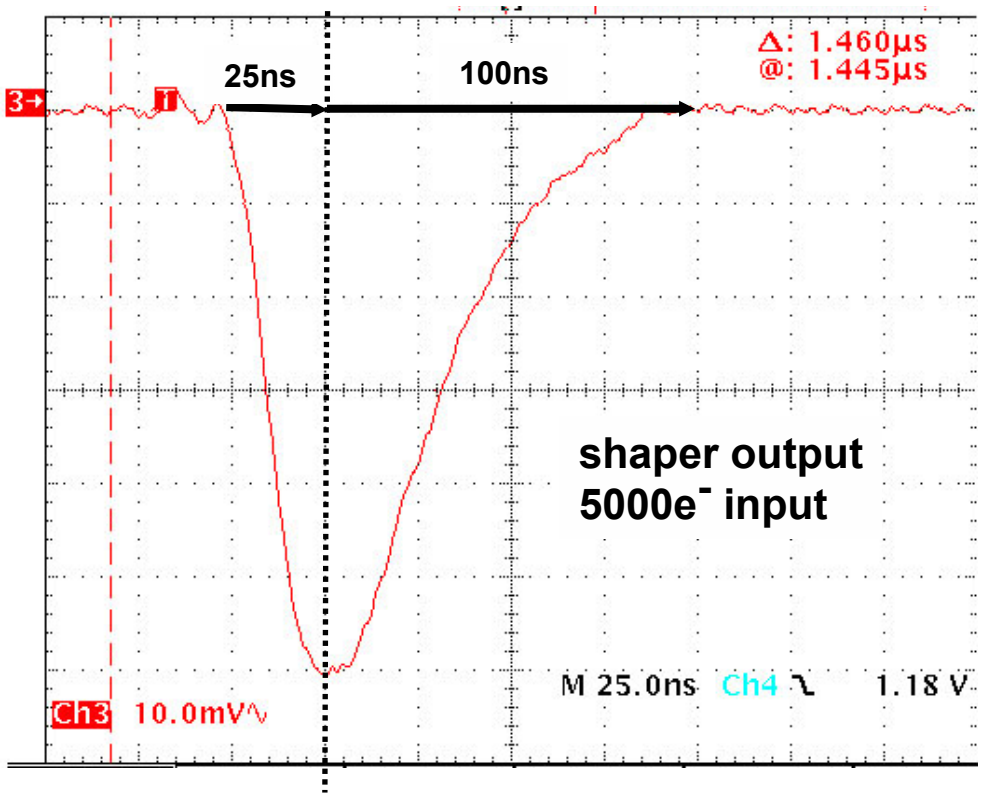
- **Small input capacitance**
- **Front-end occupancy divided by 8**

Electrical Test Results (1)

Using calibration pulse

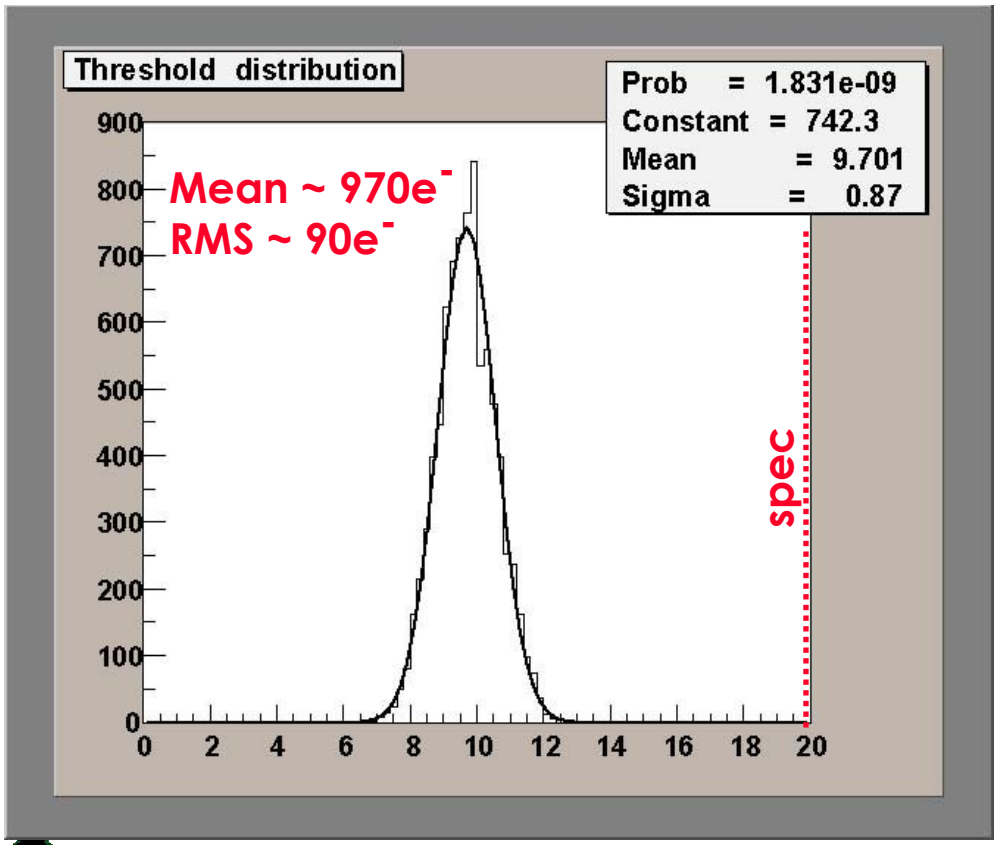
Analog front-end fast recovery – low risk of pile-up

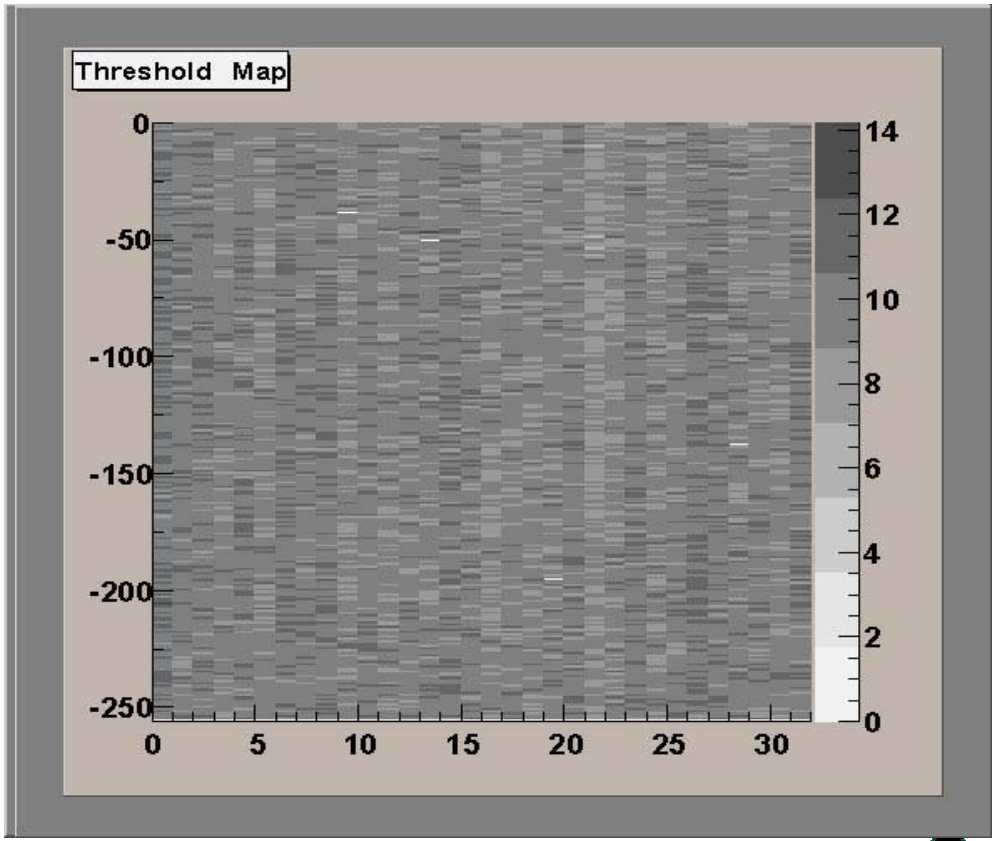
Shaper output



Electrical Test Results (2)

Discriminator threshold & noise





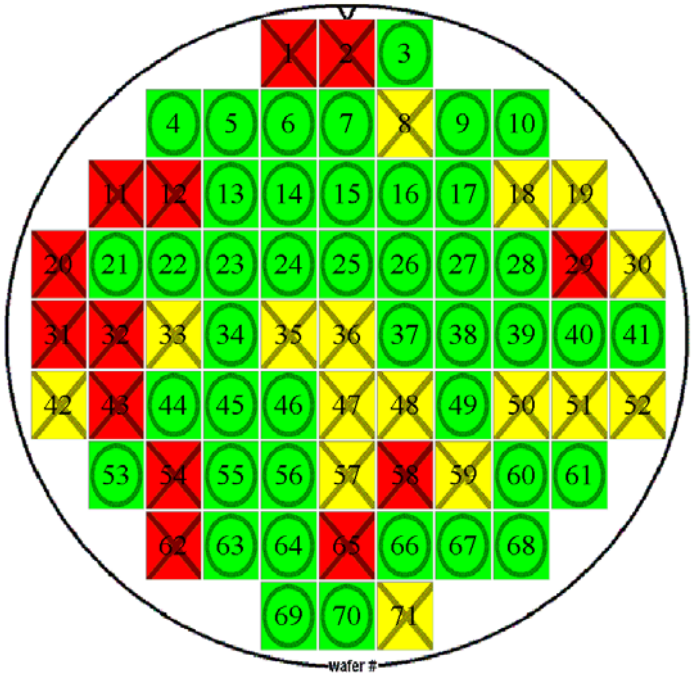
(Without individual threshold adjustment)

Chip testing

Custom test system designed for probe testing of wafers (& bump-bonded assemblies, anodes, HPDs……..)

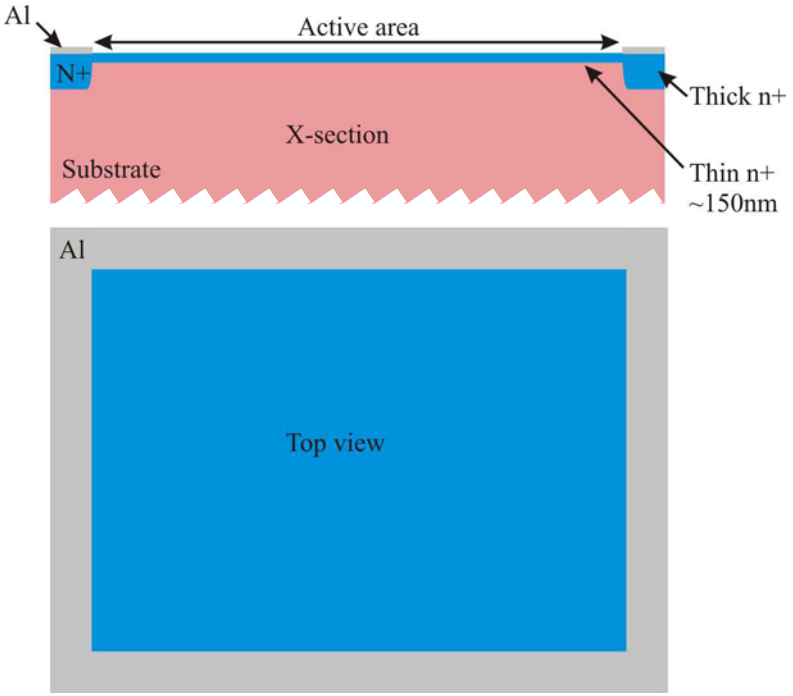
Known-good-die identified before bump-bonding

55% yield of good chips



Silicon Sensor

Optimised for photoelectron detection (Canberra, Belgium)
Minimise energy lost on ohmic side of detector
Diode side: simple p-on-n pixel diodes



Ohmic side

20keV electron penetrates
~ 5μm depth of Si

Bump-bonding (1)

Two 'standard' methods of fine-pitch bump-bonding (in High Energy Physics)

- Indium bumps – compression or reflow, melting point 156°C
- Solder bumps – reflow, eutectic (SnPb 60/40) melting point 183°C

Problems with both because of:

1. high T curing of glue (non-outgassing) used for packaging at 400°C
2. high temp processing of HPD at 300°C (bake-out to remove contaminants)

Eutectic bumps melt:

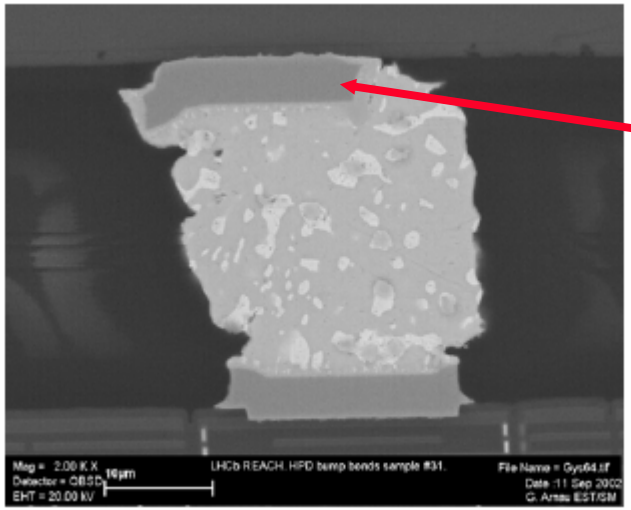
- Connections suffer during thermal expansion/contraction
- Dissolution of under-bump-metals into molten solder

Eutectic before bake

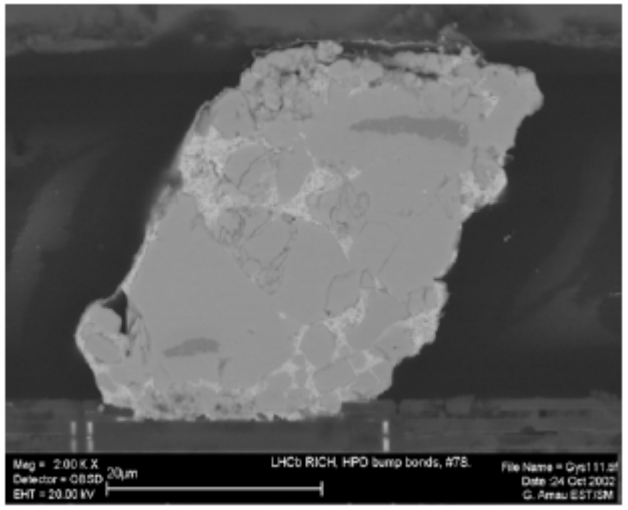
Eutectic after bake

Sensor

Chip



Under Bump Metal (UBM)



Bump-bonding (2)

VTT, Finland: bump-bonding recipe using solder with high melting-point (SnPb 10/90)

25um

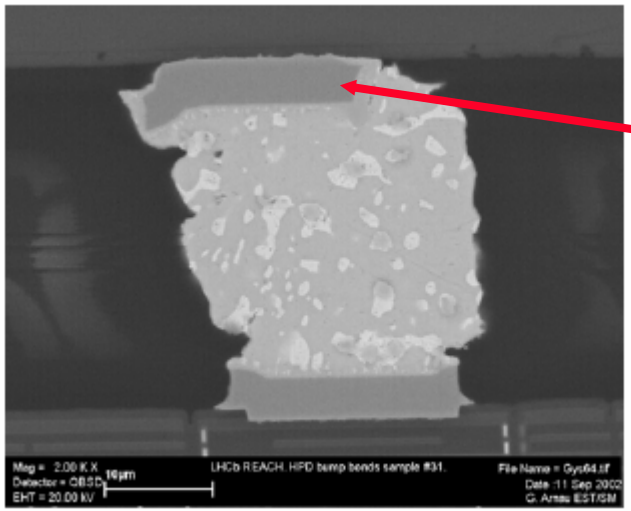
Long programme of tests (bake-outs, SEM photos, pull-strength tests, prototype HPDs) has successfully proven the bump reliability

VTT producing assemblies with > 99% good bumps

Eutectic before bake

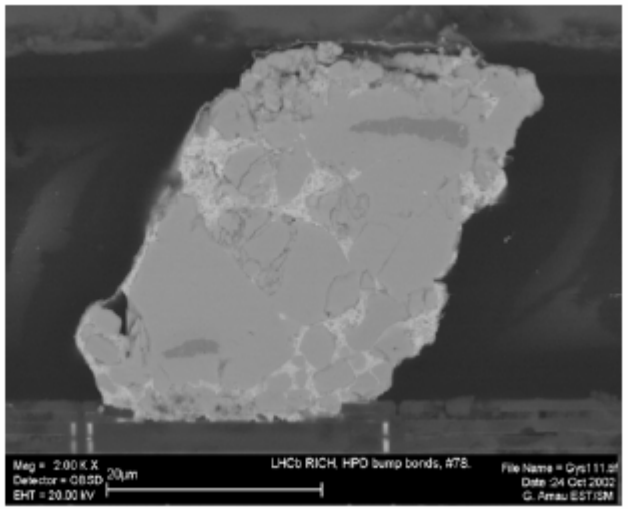
Sensor

Chip

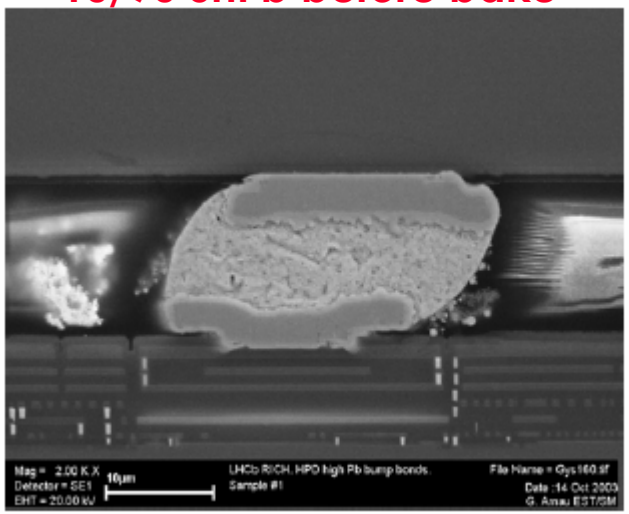


Under Bump Metal (UBM)

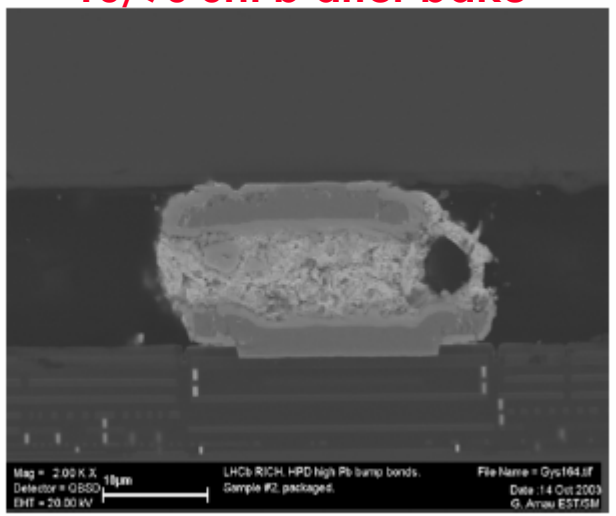
Eutectic after bake



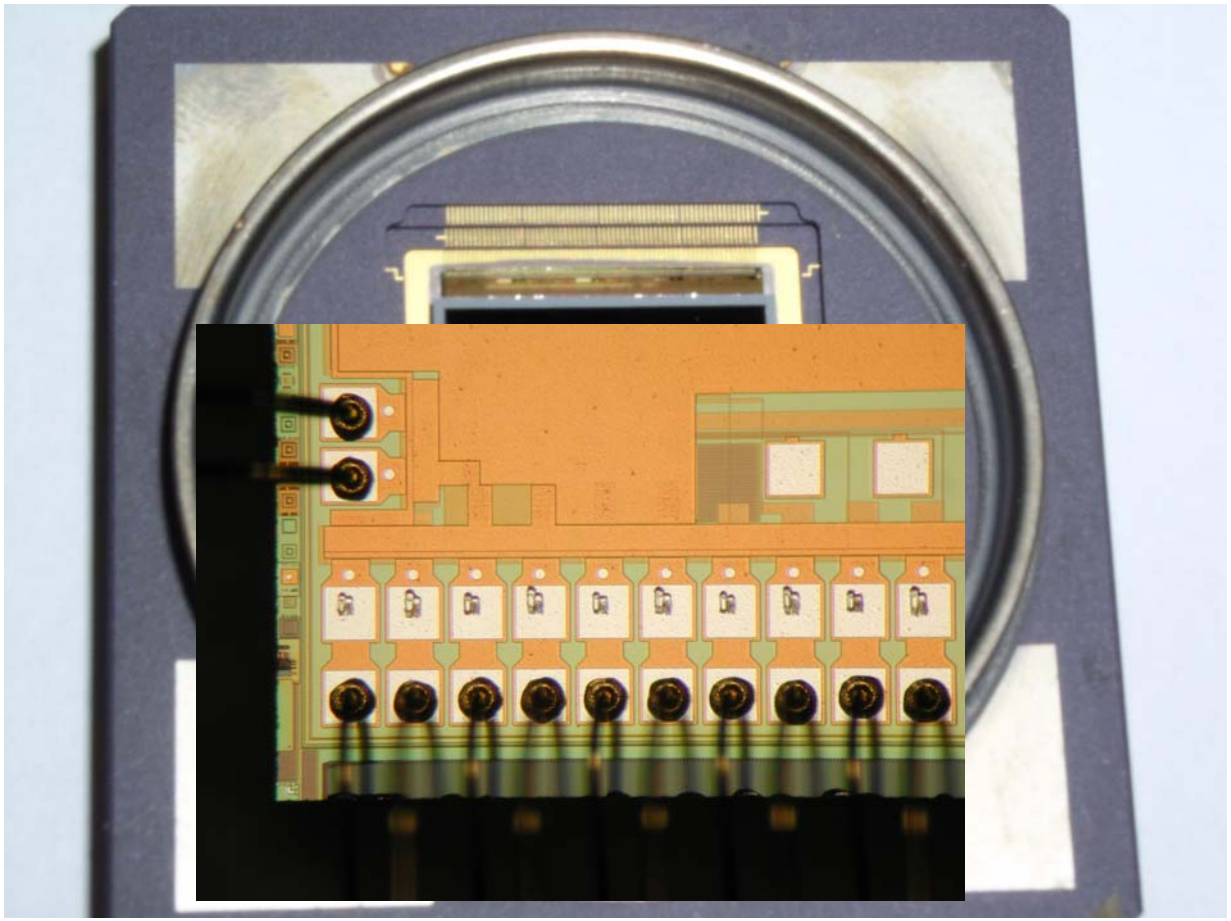
10/90 SnPb before bake



10/90 SnPb after bake



Packaging



Ceramic carrier produced by Kyocera, Japan

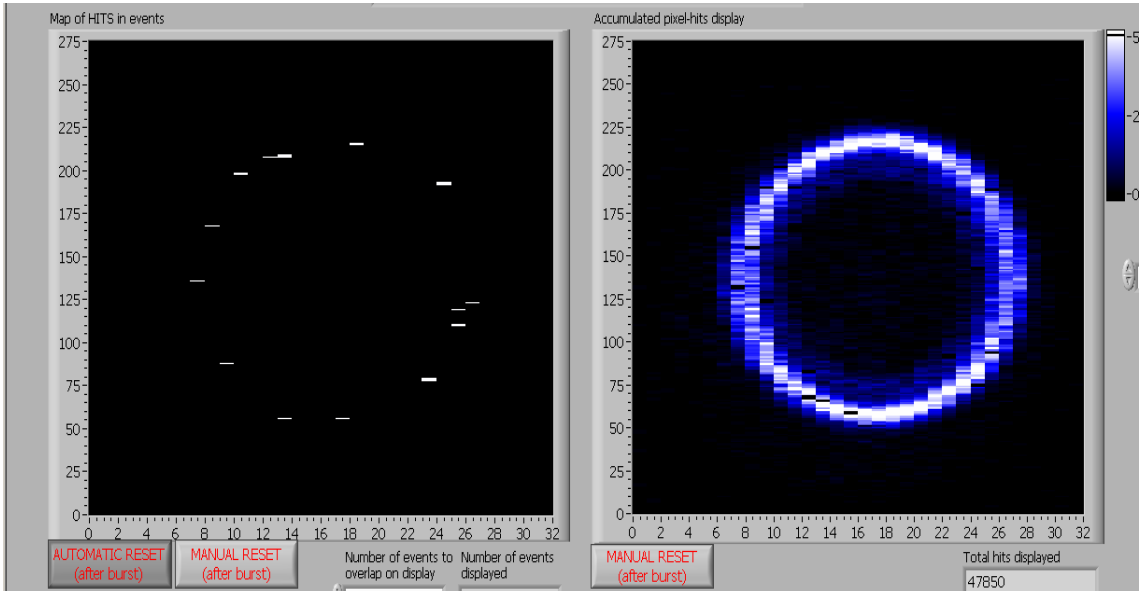
- Good thermal conduction

….. and finally the HPD

Since solving bump-bonding challenge, 6 prototype HPDs produced by DEP, Holland

All tested in lab with excellent efficiency & low noise (dominated by dark counts from photocathode)

Testbeam results – clean Cherenkov rings (see Laura's talk)



Conclusion

- Silicon pixel sensor & electronics chip designed for HPD application
- Electrical requirements of chip fulfilled
- New bump-bonding process developed & verified
- Prototype HPDs produced & meet requirements
- The long production process is underway……..

- **Spare slides**

Production

Production is underway – final goal = 500 HPDs for LHCb

Challenge of logistics: we have 6 industrial collaborators in Japan, Belgium, France, Finland & Holland

Many testing stages:

1) Identify Known-Good-Die of pixel chip
2) Test bump-bonded assemblies
3) Test packaged assemblies (anode)
4) Test HPDs

Stages 1) – 3) at CERN, 4) in collaborating institutes

Intermediate verification steps by companies => yield factor at every step

Custom test system produced for institutes & companies

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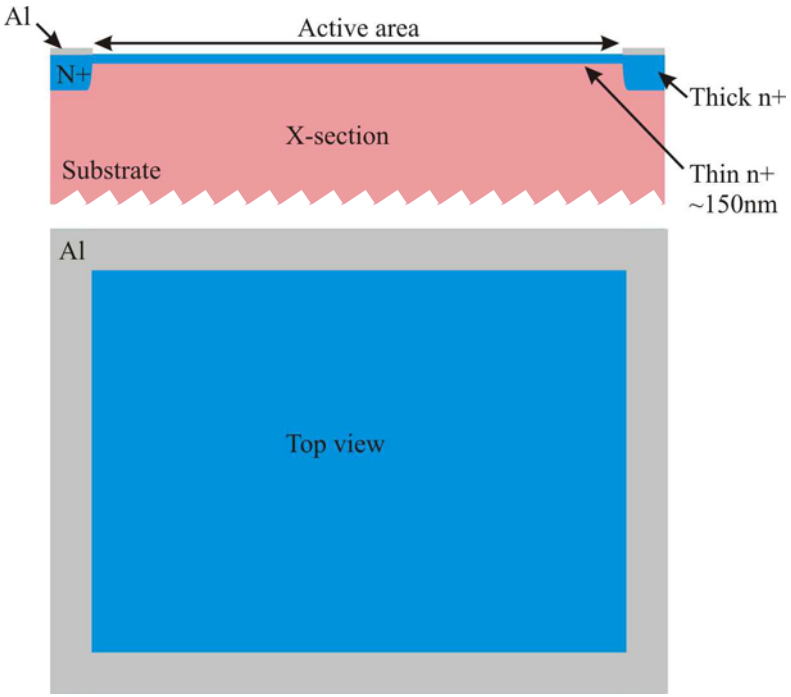
Ohmic side:



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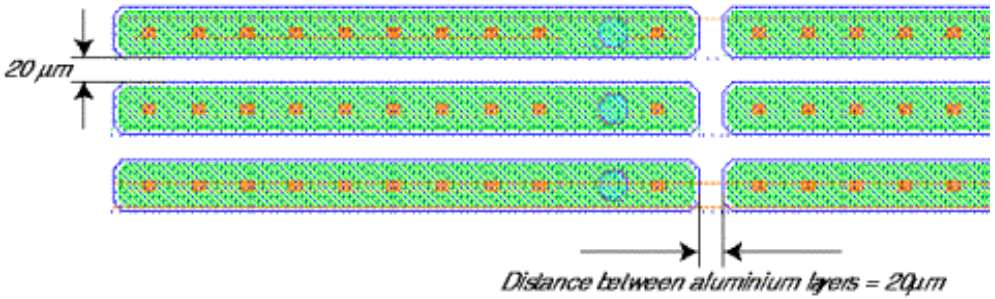
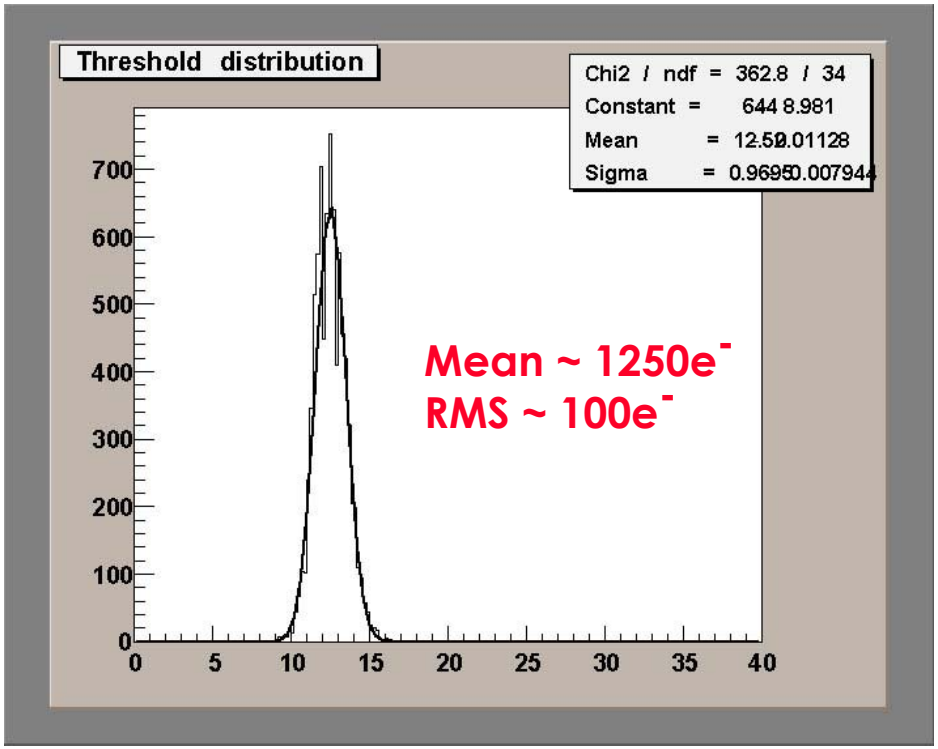
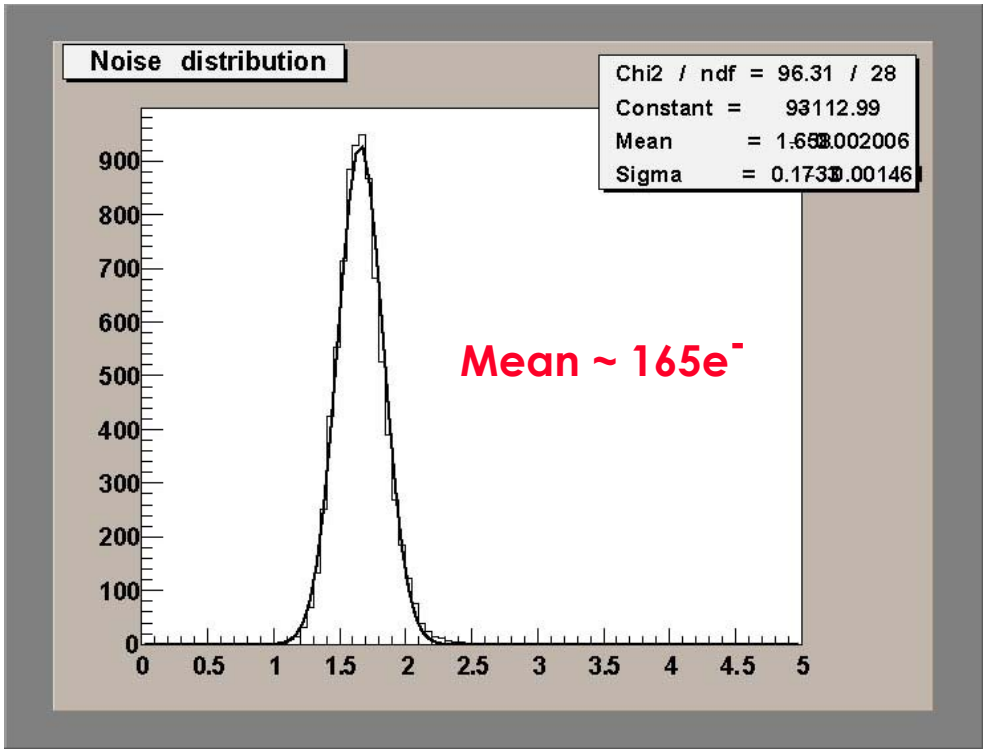
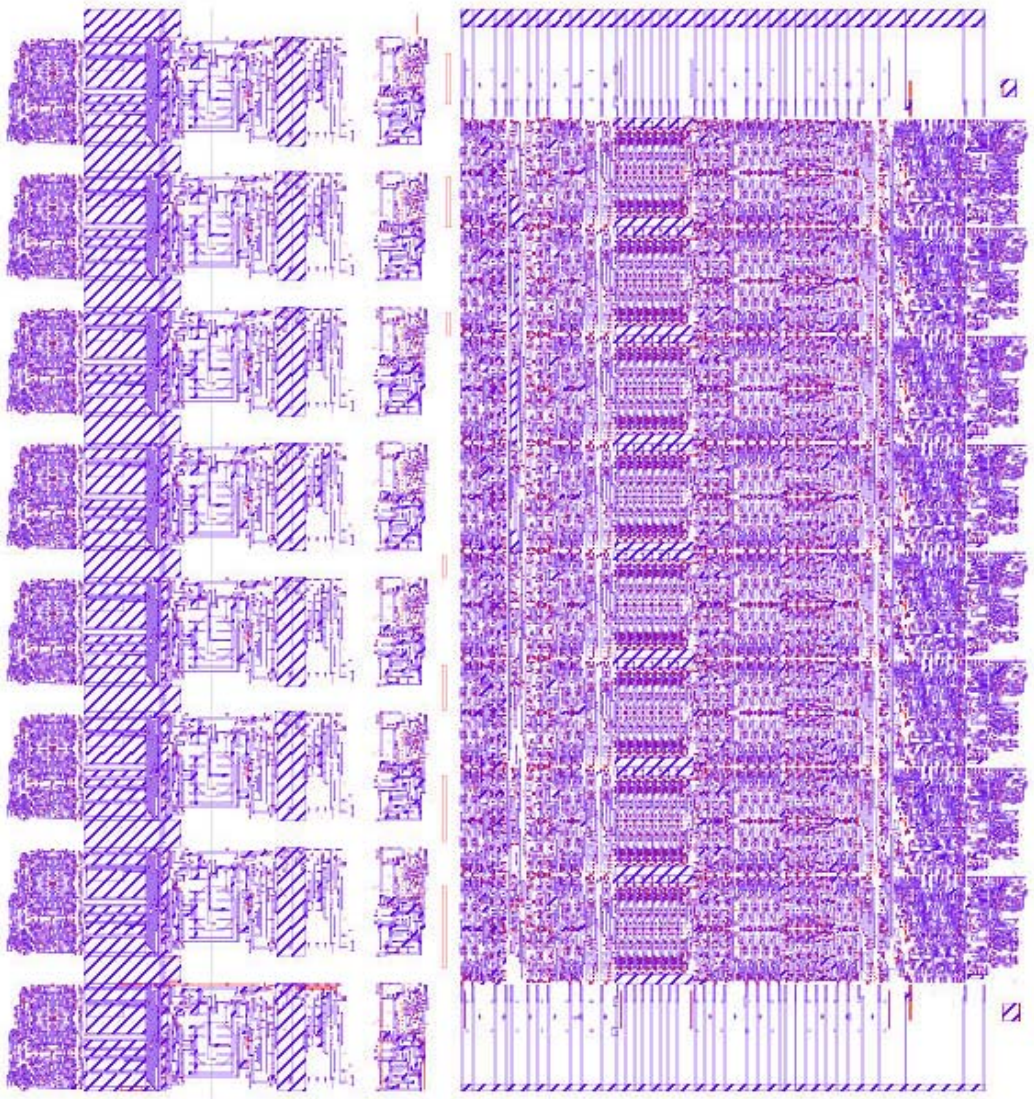


Electrical Test Results - assembly





Super-pixel layout




SAVE THE
HAGGIS