Measurements and Simulations of Charge Collection Efficiency of p+/n Junction SiC Detectors

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Outline

- Introduction
- Technological processes and I/V C/V measurements on p⁺/n diodes
- CCE setup and measurements
- Modeling of SiC detectors
 - Motivations and simulation tool
 - Results
- Conclusions









Introduction



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- Large Hadron Collider (LHC) experiment (upgrade)
- Fast hadron fluences above 10^{16} cm⁻² (after 10 years)
- Current silicon technology is unable to cope with such an environment
 - Unreachable full depletion voltage
 - Very high leakage current
 - Poor charge collection

efficiency







Silicon Carbide

- large $E_{g}(3-3.3 \text{ eV})$ \longrightarrow very low leakage current
- MIP (Minimum Ionizing Particle) generates 55 e/h pairs per µm
- radiation hardness (?) (high atomic binding within the material)
- high quality crystals now available
- Schottky barrier detectors have been studied as α -particle detectors (100% of charge collection efficiency (CCE))*
- complex radiation detectors an integrated electronic readout on board of the detector chip. p/n junctions are needed

* F. Nava, et al., IEEE Transactions on Nuclear Science, Vol. 51, No. 1 (February, 2004).







SiC Process: p⁺/n



Epi (40 µm) doping: $1 \times 10^{15} \text{ cm}^{-3}$



Al (350 nm) / Ti (80 nm) deposition



Ion implantation Al⁺ @ 300°C Annealing 1650°C 30 min p^+ doping (0.4 μ m) $= 4 \times 10^{19} \text{ cm}^{-3}$ p^{-} doping (0.6 μ m) $= 5 \times 10^{17} \text{ cm}^{-3}$



Annealing 1000°C in vacuum 2 min









- 75% of diodes have good I-V curves ullet
- V_{BD} is about 4 kV
- Theoretical limit for this device: 5 kV









CV measurements



Epi doping (1.1×10¹⁵ cm⁻³) confirmed •









CCE measurements setup









CCE measurements

- Measurements on p+/n diodes: epi $1.1.10^{15}$ cm⁻³ 40 μ m,
- Max. applied voltage: 900V (30 μ m depleted). V_{dep} (from theory) =1600V



100% collection efficiency in the 30 µm deep depleted region using measured lengths of depleted region



Filin Imaging Des







Motivations for simulation

- Very high cost of SiC wafers
- Trade off between SiC wafer quality and available budget
- Suitability of device simulation for design optimization
- Introducing traps, we will be able to analyze which defects ulletare important to decrease the CCE Simulation Tool
- DESSIS ISE-TCAD
 - Discrete time and spatial solution to the fundamental semiconductor equations
 - 6H-SiC model available











p⁺/n diode output signal

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- 3x10⁻⁶ Collected Charge Current A Current A Current A Current A $CC = \int_0^t I \cdot dt$ • Particle crossing
 - at 2.5 ns



 p^+ doping (0.45 μ m) = 4×10¹⁹ cm⁻³



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Simulations of CC of Schottky diodes lmaging 50 µm Collection length (⁹⁰Sr source, β particles) Scho<u>ttky contact</u>: $q\phi_{\rm B}$ =1.6 eV 40 38 µm 35 epi n 30 L (µm) 25 simulations substrate n⁺ measurements 20 15 20 40 60 80 100 0

Ohmic contact



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F. Nava, et al., IEEE Transactions on

Nuclear Science, Vol. 51, No. 1 (February, 2004).

* Measurements from:



Voltage [V]





Conclusions

- p⁺/n junctions have been realized and electrically characterized. Good forward and reverse characteristics have been obtained
- First CCE experimental results on SiC pn junctions: 100% collection efficiency in 30 μ m using measured lengths of depleted region
- Development of a simulation model for SiC to obtain good agreement with CC measurements on Schottky and p+/n SiC diodes









Future developments

- Radiation hardness will be verified.
- New SiC detectors will be realized taking into account the simulation results.
- Using DLTS measurements and simulations, we will be able to analyze which defects are important to decrease the CCE





