# The ATLAS Pixel Detector

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On behalf of ATLAS Pixel Detector collaboration
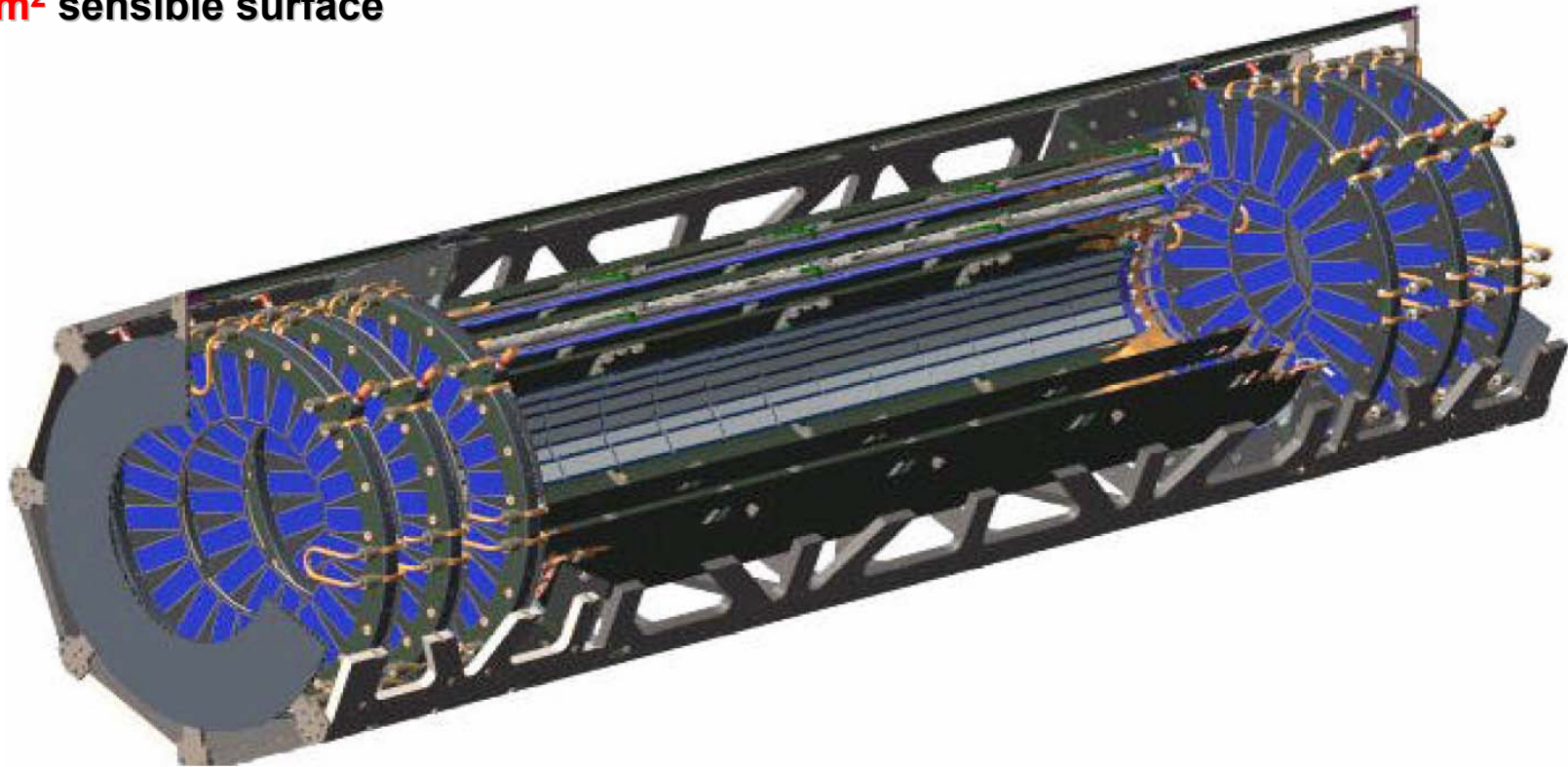
**3 Barrel layer + 6(3+3) Disks**
**5 pseudo rapidity unity**
**Inner Barrel Layer (B-Layer) at 5 cm from beam interaction**
**38 cm by 185 cm size**
**1.7 m² sensible surface**

# Pixel Detector and LHC/ATLAS

## LHC

- The LHC beam crossings at full luminosity will produce ~40 primary vertexes and some $10^3$ ionizing particles into the 5 units of pseudo rapidity at a 40 MHz rate

- The expected integrated dose in 10 y of LHC operation for the middle layer of the Pixel Detector is ~50 MRad, while for the B-Layer the expected dose is ~5 times higher.

- Silicon Pixel detectors have the low occupancy - $10^{-4}$ particle/(interaction channel) - to vertexing in the LHC environment

- Silicon Pixel detector have the low noise - < 500 $e^-$ - to continue vertexing at the end-life of the ATLAS detector

## ATLAS

- ATLAS LVL1 accepted rate is ~100 KHz, with a latency time of 2 µs

- Pixel detector readout electronics is bump-bonded to the silicon sensor and provide local buffering memory and the computing power for early sparsification of the data

# Pixel Detector Module

- Key element of the ATLAS Pixel Detector is a module.

- There are 1456 modules in the barrel, 288 in the disks. Barrel and disks modules are the same so that the uniformity in production is improved.

- Each module has 47520 channels

- The module readout electronics is made by 16 FE chips and one Module Controller chip

- A Flex-Hybrid circuit glued on the sensor backside provides the signal/power routing.

- A pigtail (barrel) + Al/Cu wire bundle connect flex hybrid to optoboards on the patch panels at either end of pixel detector. Pigtail is the only difference between barrel and disks modules, where the routing is directly wire bonded on the flex
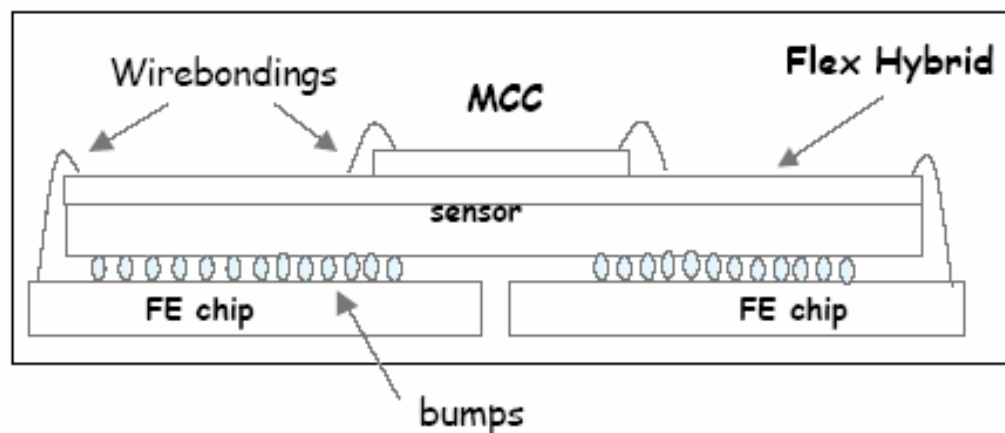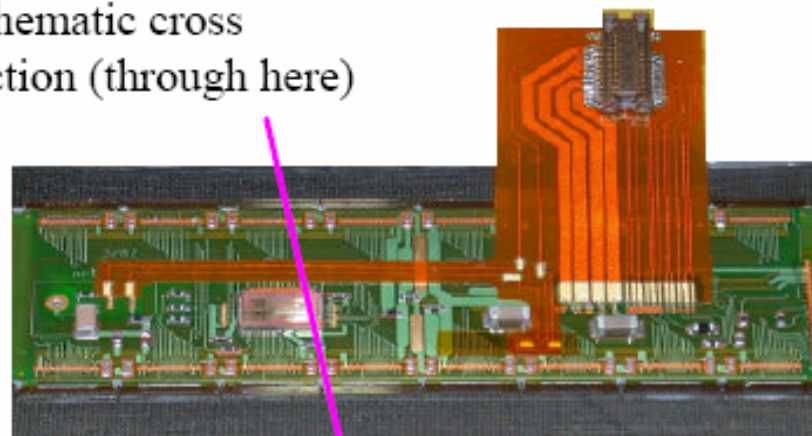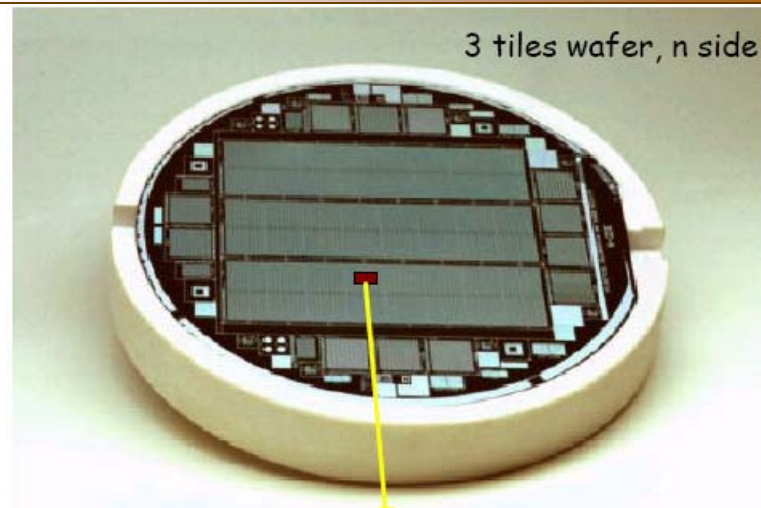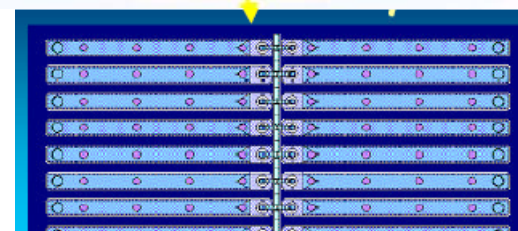
# Sensors

- **n+ on n silicon sensors**
  - ↙ After type inversion the depleted region extends from the implantations
  - ↙ Oxigenated silicon to improve the annealing
- **Moderated P-spray insulation**
  - ↙ Resistance to the radiation damage
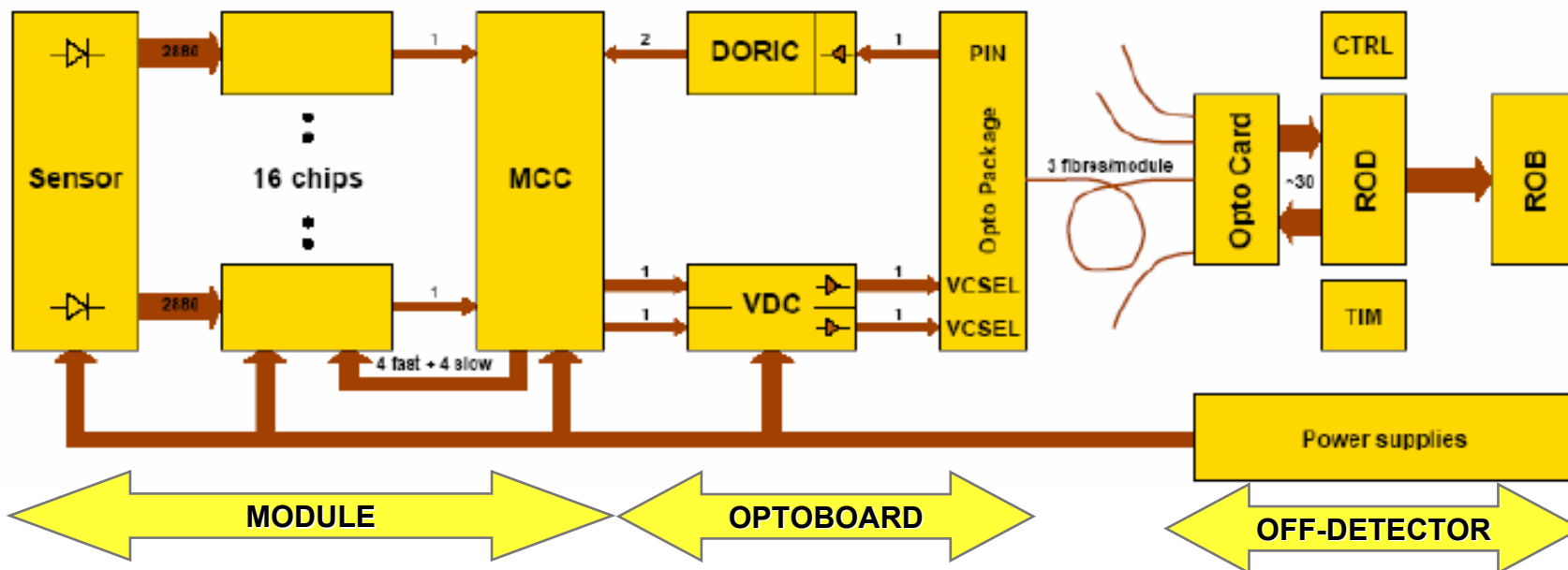  - ↙ Allows bias grid – standalone test of the sensor

3 tiles wafer, n side

n+ implants and bias grid

*AMS 310b,Tesla sensor, irr. 600 V*
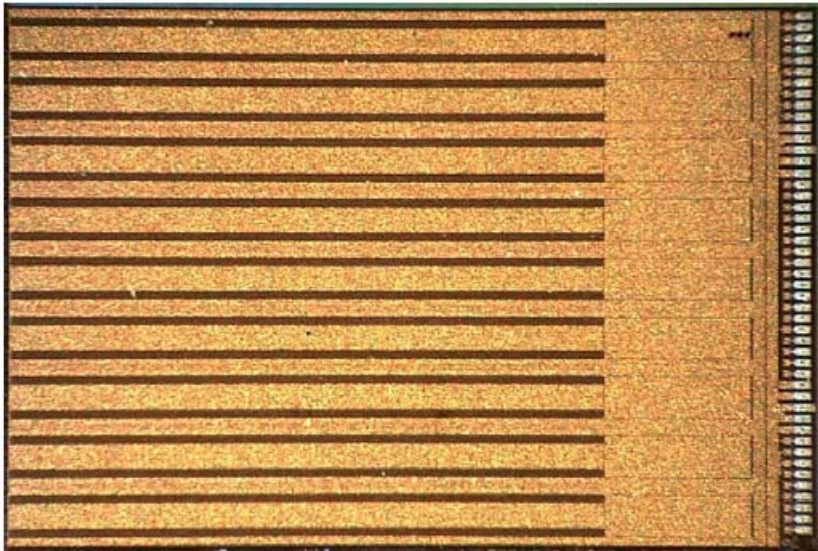
efficiency vs time

- Efficiency after irradiation 97%
- Unchanged spatial resolution
- 200 μm depleted region at 600 V on 300 μm thick sensor
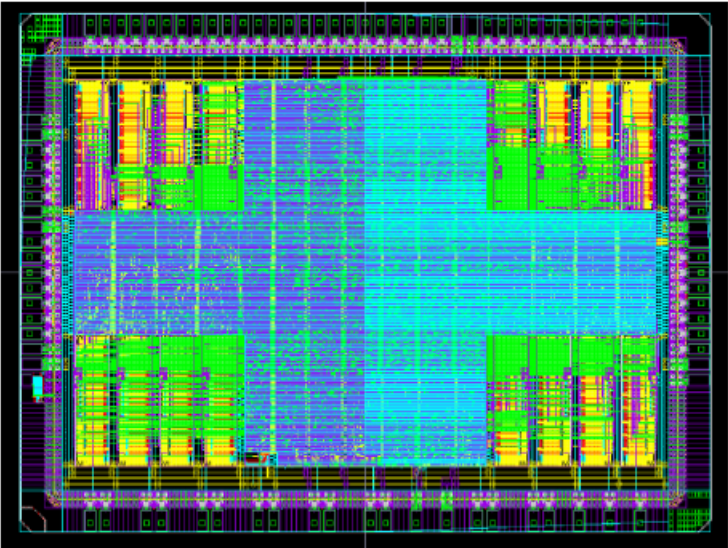  - ↙ Pixel detector sensors will be thinned to 250-200 μm

# Read-out architecture



- Two level on-detector data push readout architecture with star topology (minimize single point failure)
  - LVDS signal
- FE Chips
  - Amplify and digitize the ionizing particle signal
  - Sparsify the event data
  - Buffering of the event data during LV1 latency time

- Module Controller Chip (MCC)
  - Configuration of the 16 FE chips.
  - Event building
  - Overflow recovering
  - Trigger signal handling
- Optoboard with tx and rx chips
  - Three optical lines – one for control, two for data
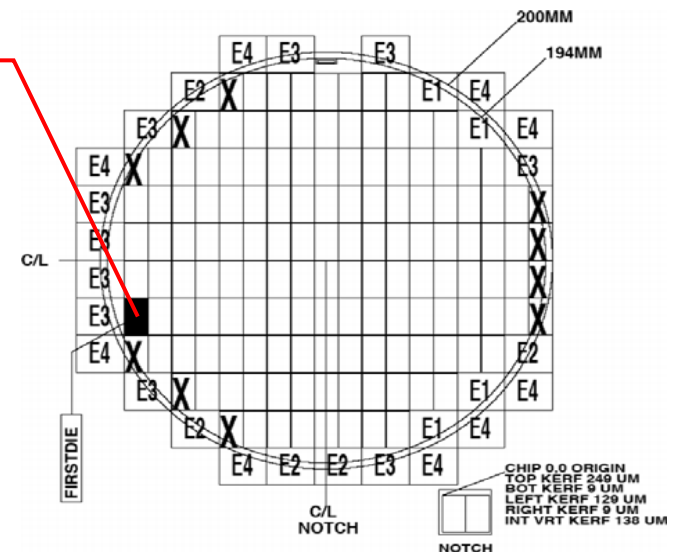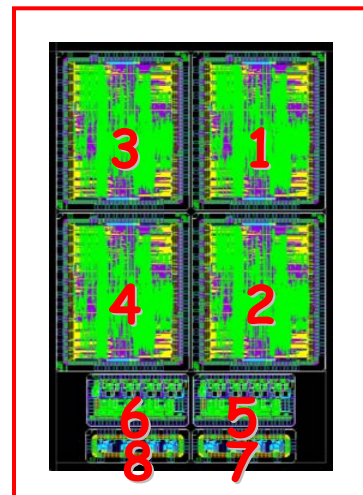  - 40/80 Mbit/s per data line – up to 160 Mbit/s bandwidth

# FE-I3 chip

- The ATLAS Pixel FE-I3 chip is the final ATLAS Pixel detector FE Chip

- IBM CMOS6SF process (0.25 μm)

- Dice size 7.2mm by 10.8mm

- ~3.5M transistors for 2880 channels of charge sensitive amplifiers attached to fast digital readout.

- 18 columns of 160 pixels

- Each individual 50 μm by 400 μm front-end consists of a high-gain, fast preamplifier using a DC feedback scheme, a threshold discriminator and a digitizing logic. The linearity of the return to the baseline is used to compute the ToT and digitize the pulse height

- Hits from FE. are stored into 64 EOC Buffers at the bottom of each column pair during the LVL1 latency – 576 hit memory



- Threshold tunable by a 5-bit GlobalDAC for the chip and by a 7-bit TuningDAC for each channel – up to $26e^-$ ($300\ e^-$ after irradiation)

- Noise ~ $200\ e^-$ ($400\ e^-$ after irradiation)

- Chips survive and are operative after 60 MRad

- SEE improved with combination of techniques: majority logic for static registers, binary logic for configuration load FFs
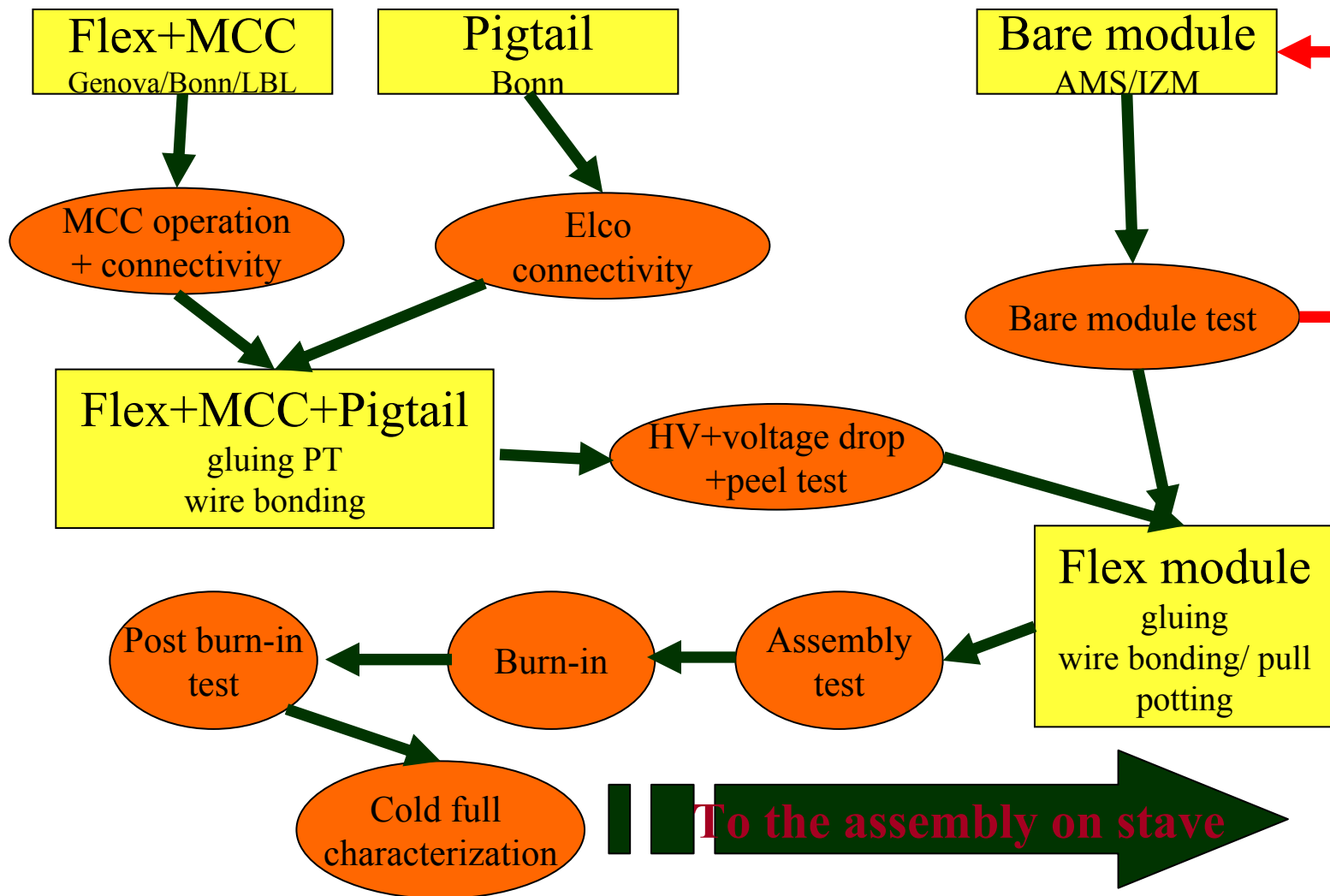
# MCC-I2 chip

- The MCC-I2 is the final MCC for the ATLAS Pixel Detector

- Standard cell CMOS technology 0.25 µm - 67.000 cells, 880 k transistors – dice size 35.2 mm$^2$

- Sixteen 128 word FIFO as buffers for LVL1 accepted event fragments from each FE chip – once all FE has sent their fragments, an event is build and sent to the optoboard

- 40/160 Mbit/s programmable output bandwidth

- SEU/SEE TOLERANT by triple majority logic of most of the FF in the chip state machines and the configurations registers



- MCC-I2 survive with no sensible effects to a integrated dose > 50 MRad (24 GeV protons at CERN PS)

- No system reset or power cycle during irradiation

- SEU cross section has been measured for triplicated registers as < 5 10$^{-17}$ cm$^2$

# Module component production

- The sensor production is carried on by two vendors
  - CiS delivered 1120 sensor (~95% tested at the moment)
  - Tesla (ON) had yield problems – production of 900 modules delayed by 2 months
- The delivery of the FE-I3 and MCC-I2 wafer has started
  - 6 wafers MCC-I2 produced and tested industrially – 3216 chip tested, 2666 good – yield 83%
  - 6 + 48 wafers FE-I3 – 266 chip per wafer – yield ~65%
    - ★ More 196 wafer – at constant yield, enough for ~2400 modules

# Putting things together

Flex+MCC
Genova/Bonn/LBL

Pigtail
Bonn

Bare module
AMS/IZM

MCC operation
+ connectivity

Elco
connectivity

Bare module test

Flex+MCC+Pigtail
gluing PT
wire bonding

HV+voltage drop
+peel test

Flex module
gluing
wire bonding/ pull
potting

Post burn-in
test

Burn-in

Assembly
test

Cold full
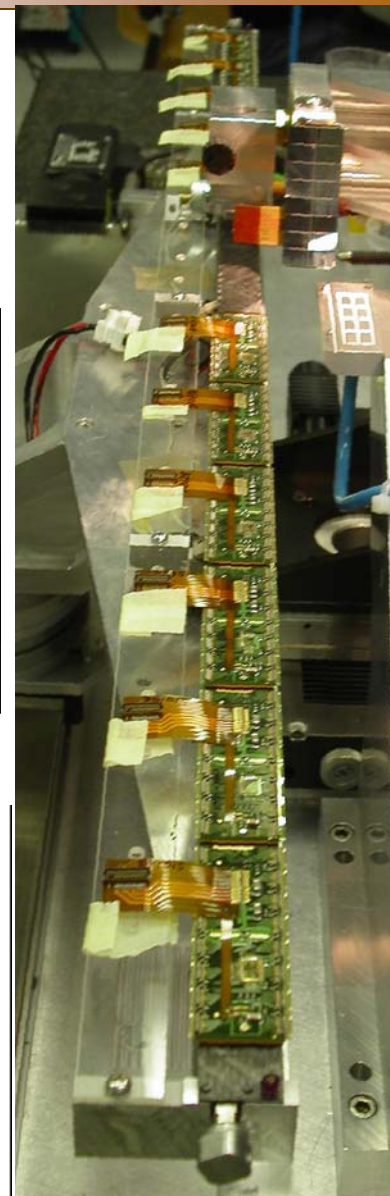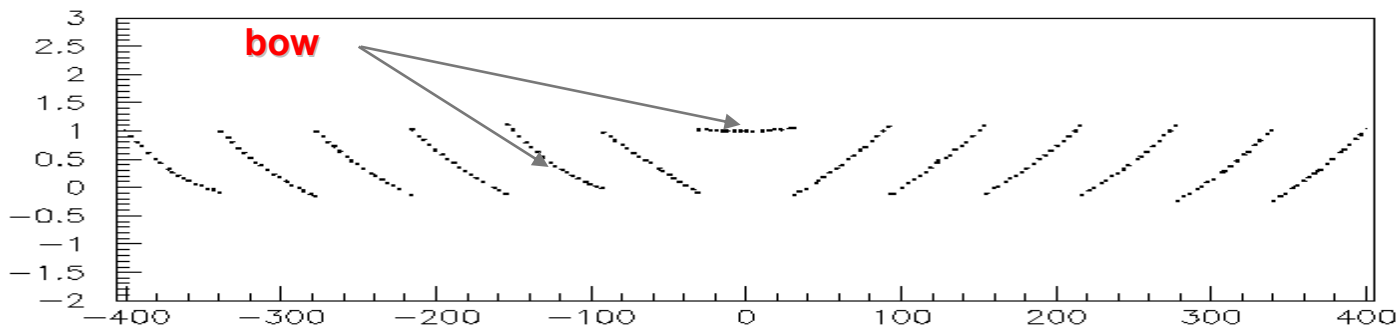characterization

**To the assembly on stave**

- VERY preliminary total yield 66 good over 76 assembled modules

# Macroassembly production

- A 13 module stave has been produced using pre-production modules

- Mechanical measurements performed in three dimensions:

  ↙ Transversal position precision achieved - ±25 μm
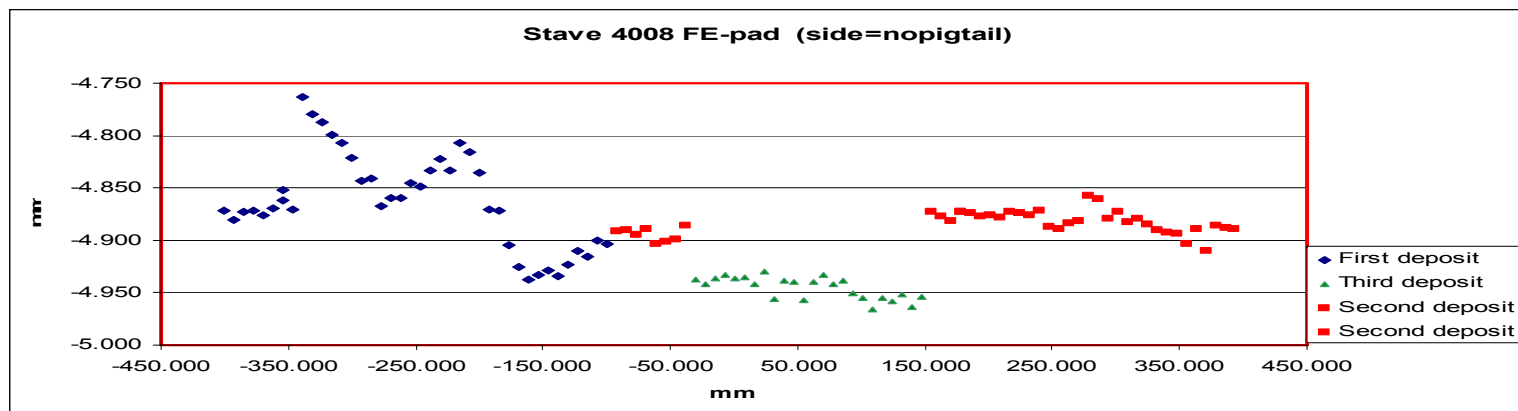


  ↙ Radial position measurement show a bow ~ 60 μm

# Conclusions

- The final generation of readout electronics built in rad-hard DSM technology meets the ATLAS requirements

- Both FE and MCC chips have shown to resist to the high integrated and instantaneous particle flux expected in LHC

- Production of modules for the barrel and the disks of the Pixel Detector has started.

- First large scale assemblies (stave and disks) produced