Status and Performance of the CDF Run II Silicon Detector

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on behalf of the
CDF Silicon Operations Group

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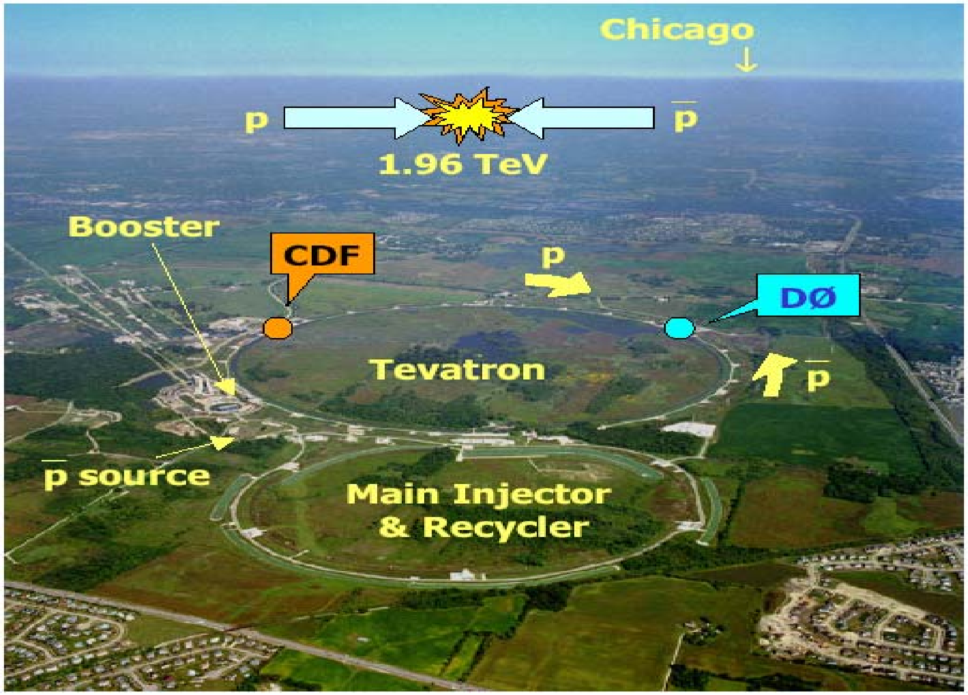
Tevatron Run II Upgrade

- Original Tevatron Design (Run "0"):
  - $10^{30}\ \mathrm{cm^{-2}\,s^{-1}}$
- Run I (ended Feb 1996)
  - Lum ~$2.5\times10^{31}\ \mathrm{cm^{-2}\,s^{-1}}$
  - CDF integrated 110 $\mathrm{pb^{-1}}$
- Run II Upgrades:
  - Main Injector (factor of ~5)
    - Improved pre-acelerator to TeV
    - Higher pbar production efficiency
  - Recycler (factor of ~2)
    - High capacity antiproton storage device
    - Electron cooling (being commissioned)
  - 36x36 bunches at 396 ns
  - $\sqrt{s}$ = 1.96 TeV (was 1.8 TeV)

    => Currently the World's highest energy collider
  - Final goal 2-3 x $10^{32}\ \mathrm{cm^{-2}\,s^{-1}}$

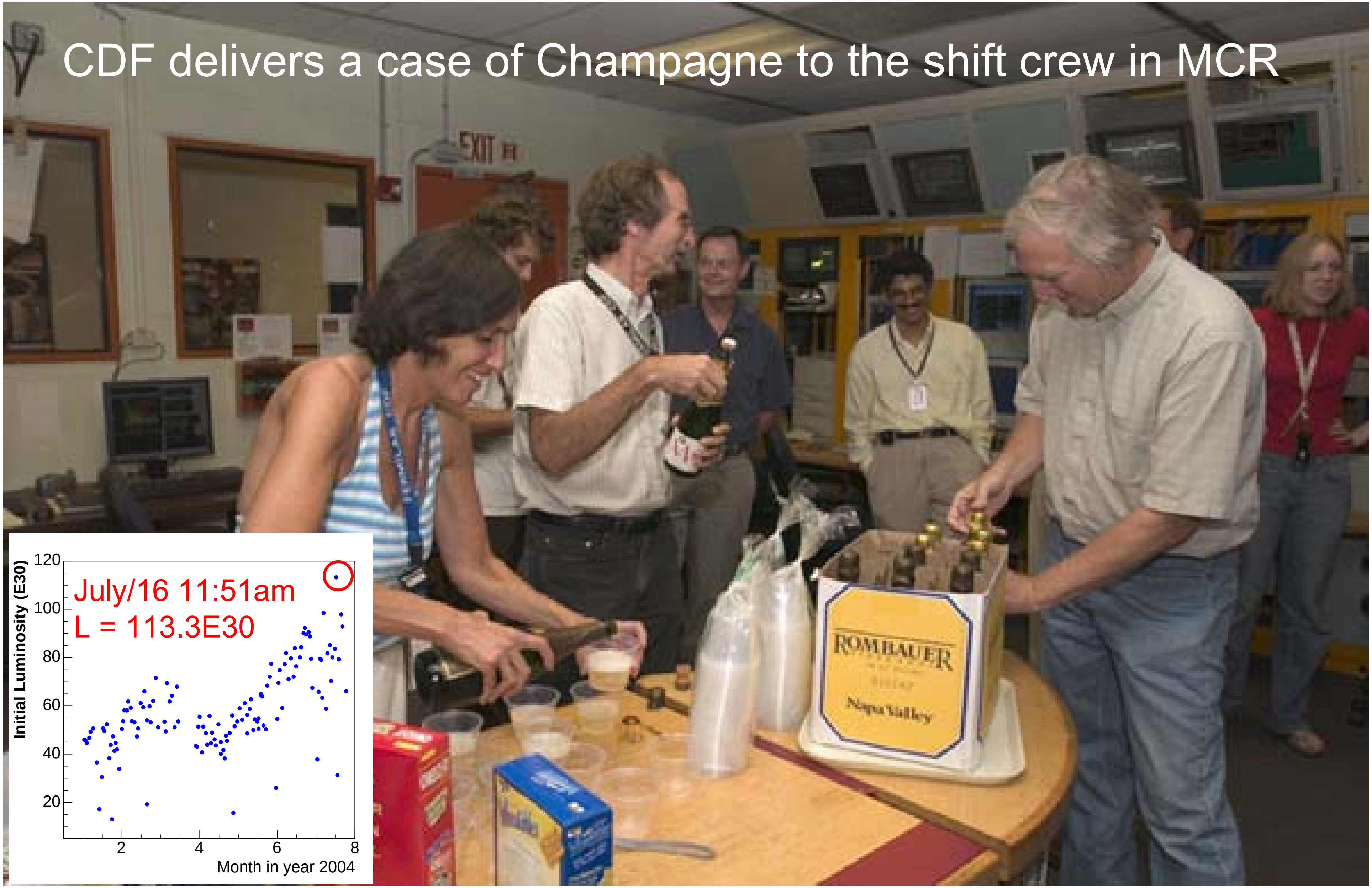
=> Increased demand on detector as regards readout speed, radiation hardness and capability to handle multiple interactions @ high luminosity



Run II Physics Goals:

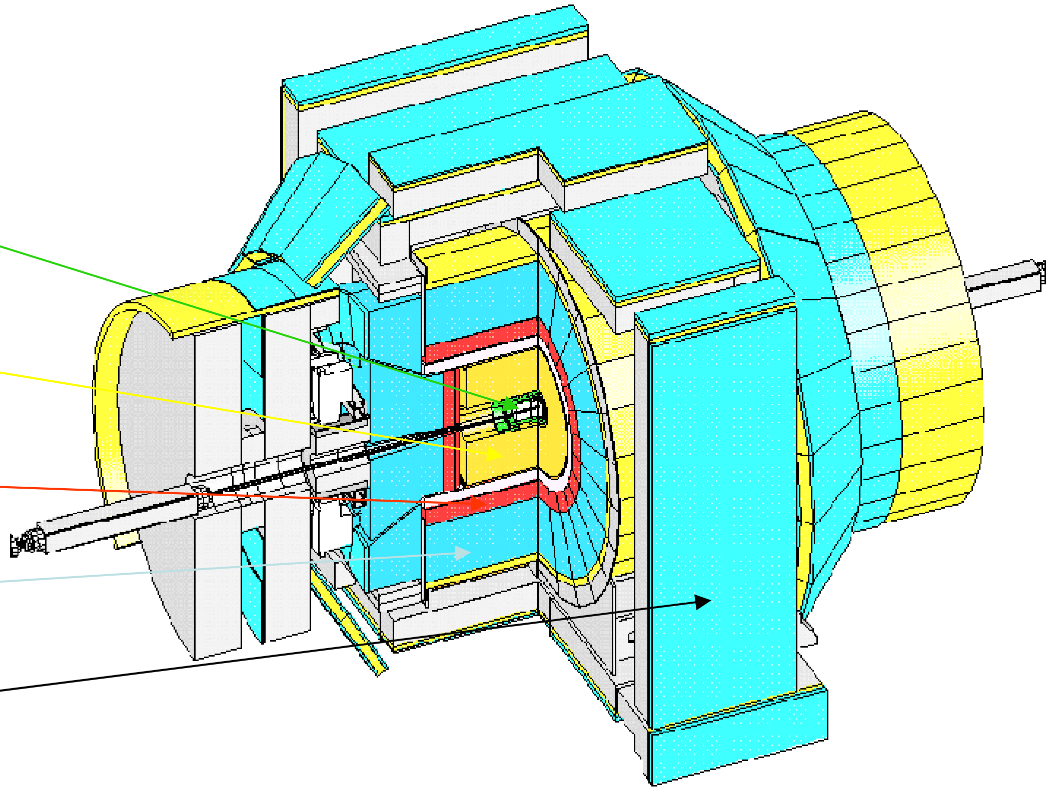
- Properties of top quark
- Precision Electroweak Physics
- CKM, B_s Mixing
- Searches for new phenomena
- Tests of QCD

CDF delivers a case of Champagne to the shift crew in MCR



http://www.fnal.gov/pub/today/archive_2004/today04-07-22.html

CDF Run II Detector



Si tracker

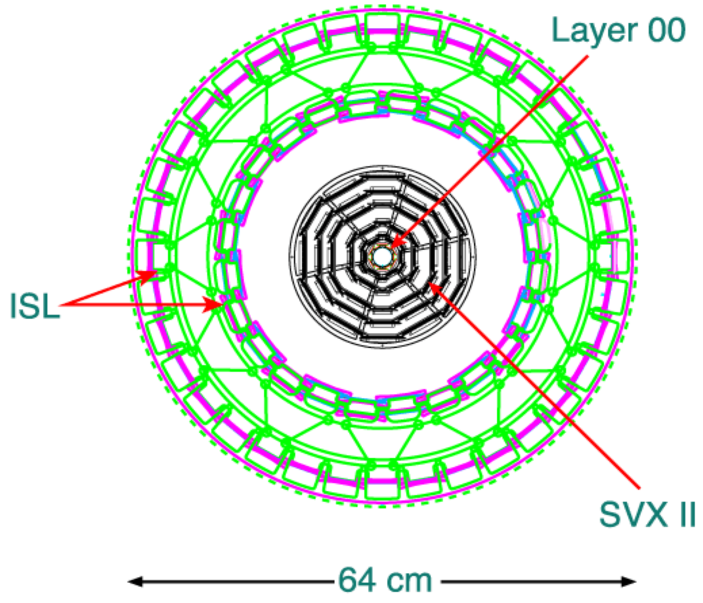
large radius tracking
wire chamber (COT)

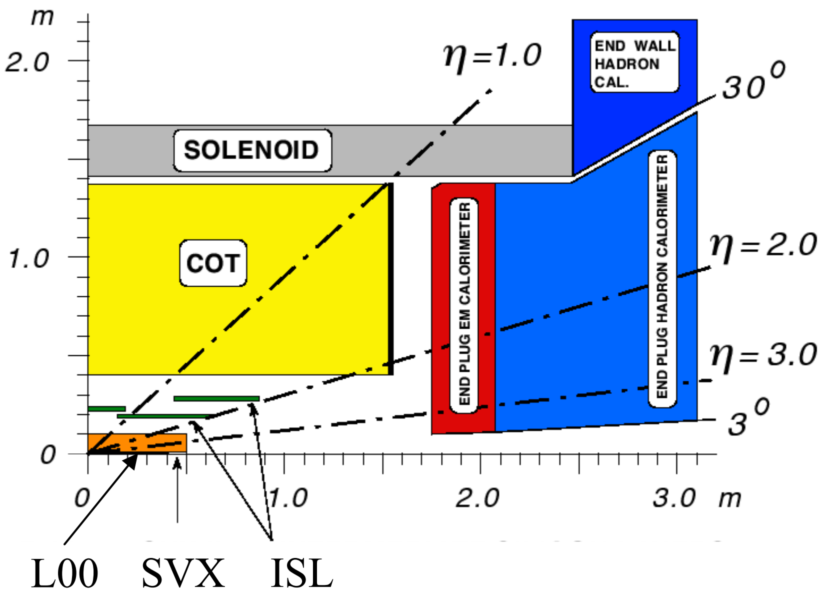
Magnet

Calorimeter

muon chambers

CDF Run II Silicon Upgrade





Detector Goals:

Heavy flavor tagging efficiency

B reconstruction efficiency

Increased Forward Tracking Acceptance

Improved σ_{d0} (~20 μm)

Run II Silicon:

7-8 silicon layers

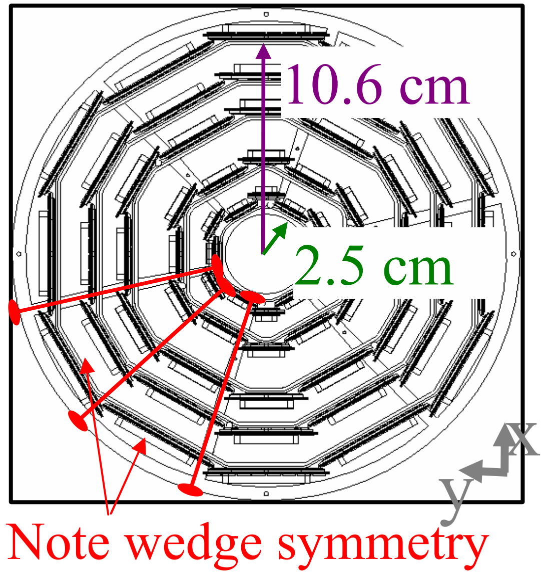
722,432 channels

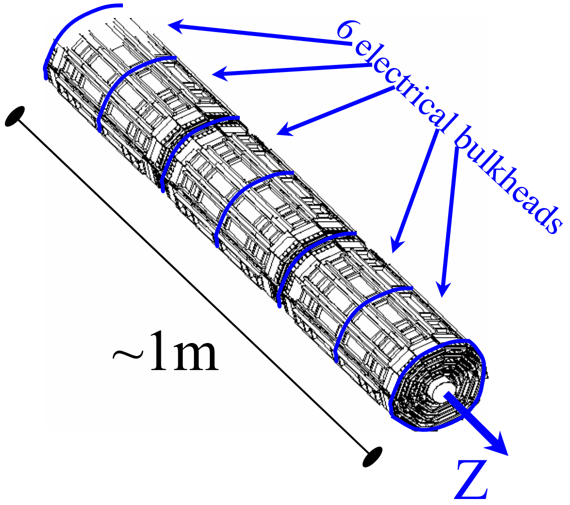
$r\phi$, rz views

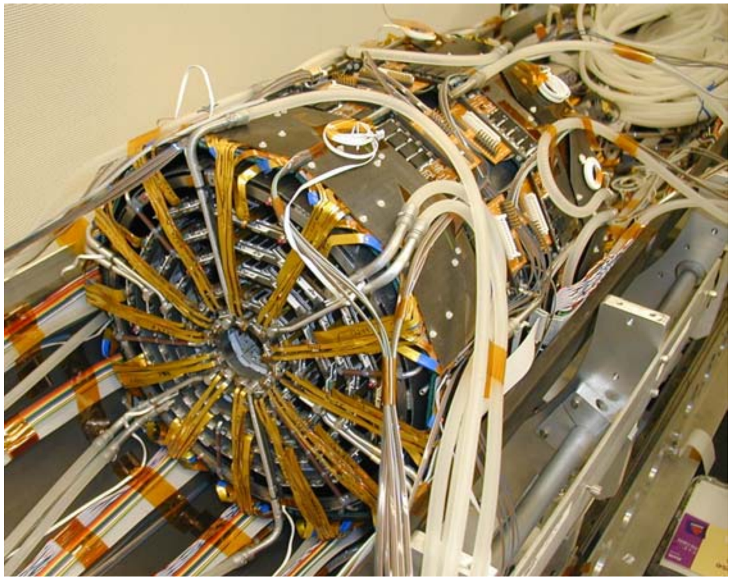
z^{max} = 45 cm, $|\eta|^{max}$ = 2

1.3 < *r* < 30 cm

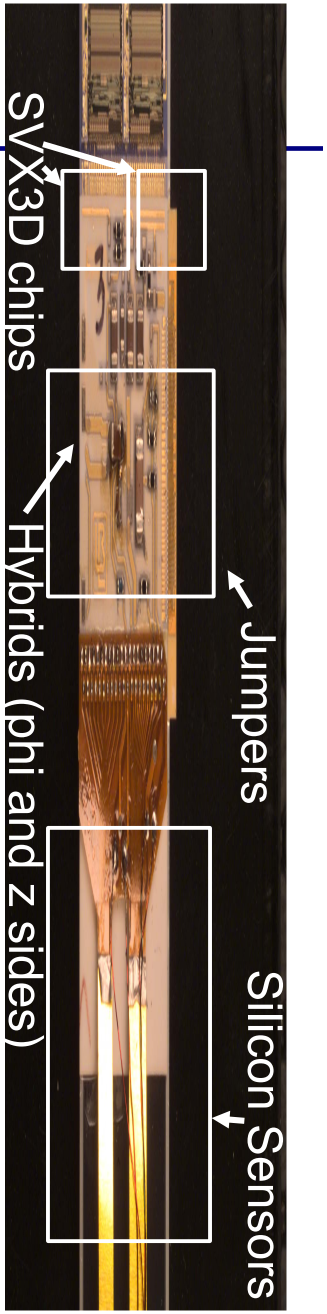
Baseline Upgrade: SVX II



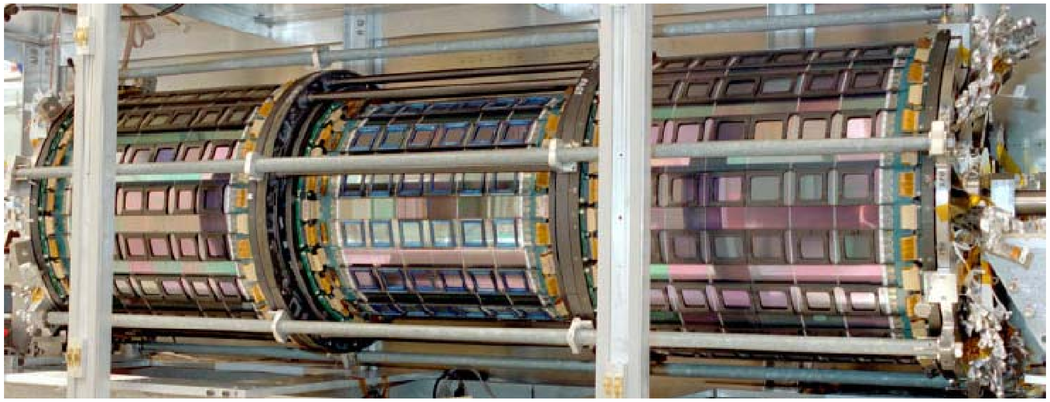


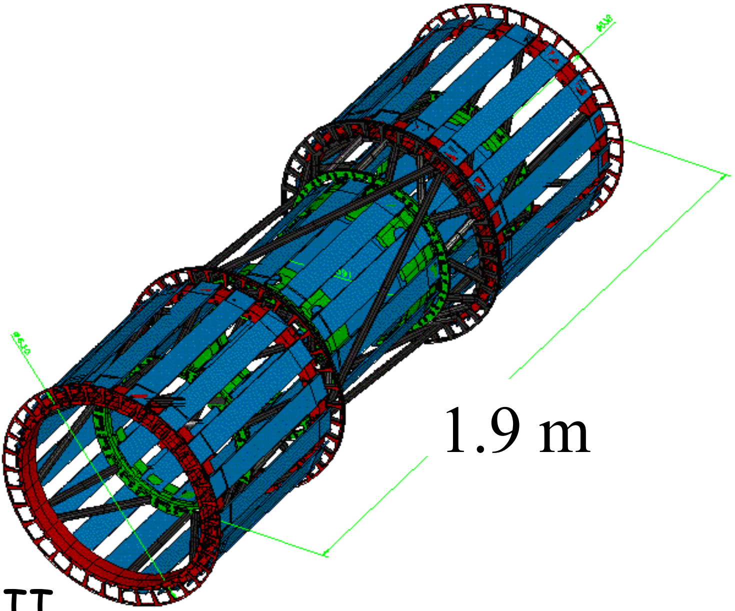


- 5 Double-sided layers
  - 5 axial, 3×90°, 2×1.2°
- Tight Alignment Tolerances
  - For displaced track trigger
- Highly Symmetric
  - 12-fold in ϕ
  - 6-fold in z

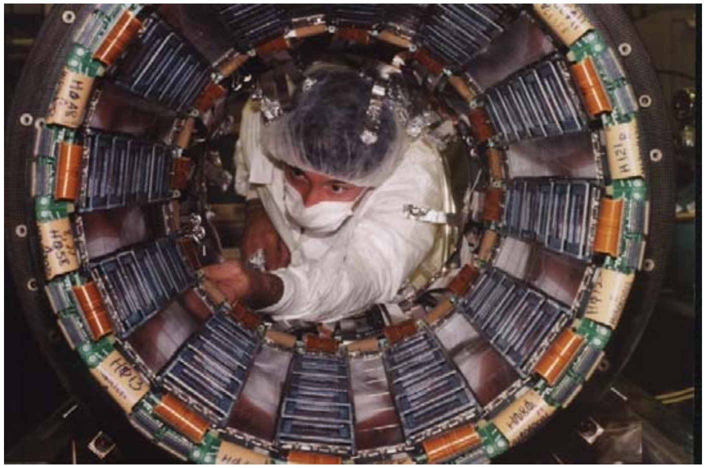


Upgrade to the Upgrade: ISL

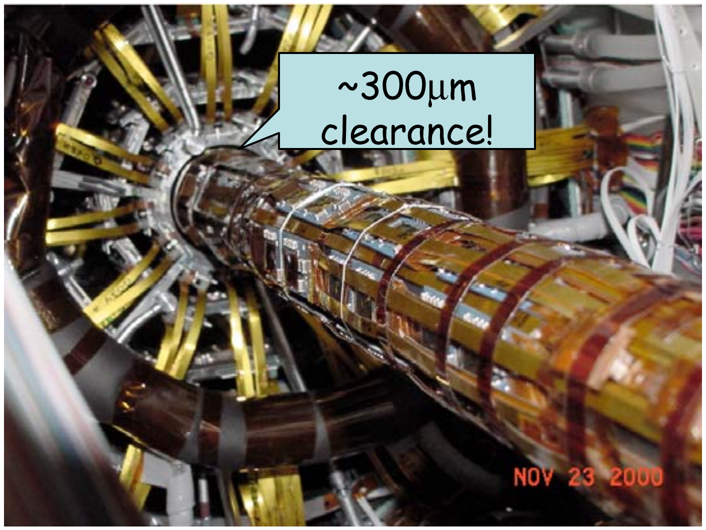


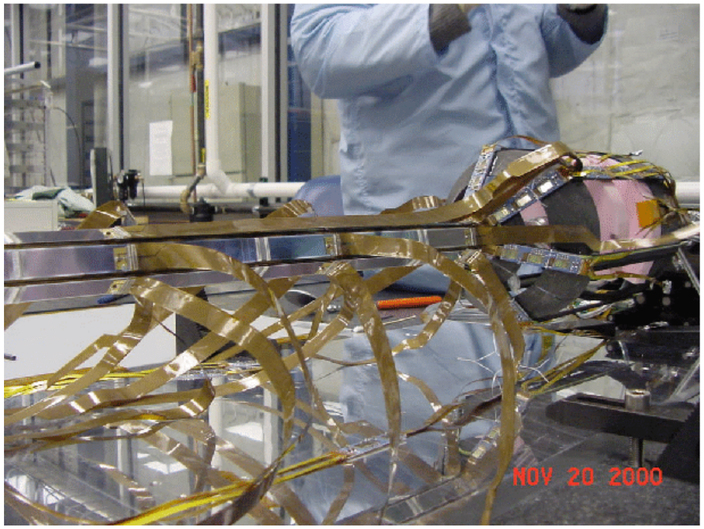


- One central layer ($|\eta| < 1$)
  - Link tracks from Drift Chamber to SVXII
- Two forward layers ($1 < |\eta| < 2$)
  - Silicon tracking in forward regions
- Simpler Design
  - Not used in trigger (less stringent alignment)
  - Hybrids mounted off silicon
  - One kind of double-sided sensor flavor

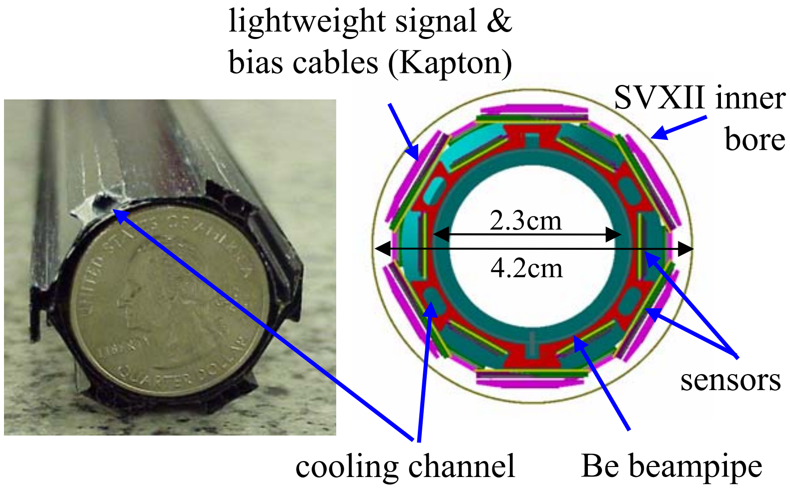


Upgrade more... L00





- Precision position measurement before scattering in dead material
- Single-sided layer mounted on beam pipe
  - 25 μm pitch; every other strip read out
  - Low material budget (0.6% - 1.0% $X_{0)}$
  - Actively cooled
  - Electronics at either end, larger radii
  - Rad hard silicon; capable of 500V bias (will outlast SVXII inner layer L0)



Operational Experience

Long commissioning period:

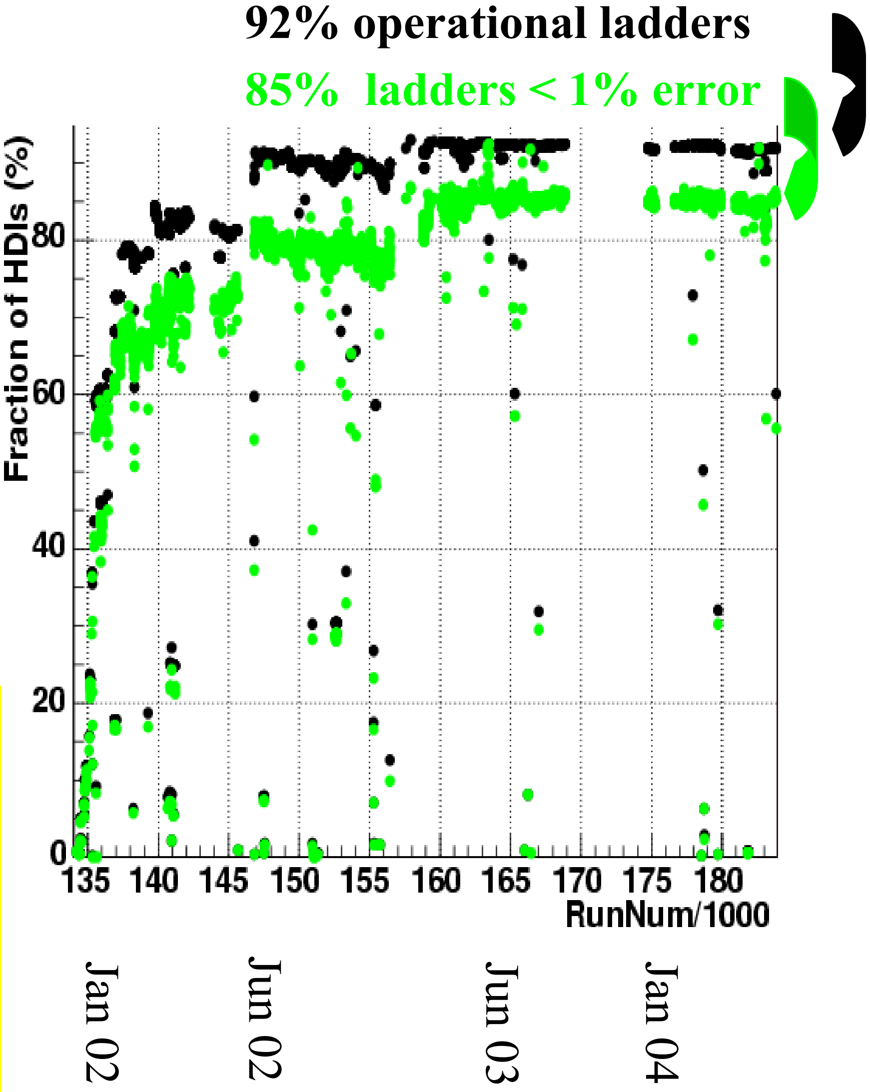
- Large scale, complex system
- Wire bond failures due to Lorentz forces which induced mechanical fatigue in non-standard trigger conditions
- Epoxy blocked cooling lines in part of ISL
- Power supply failures due to single event burnout from beam losses
- Analog pickup on cables in L00

detector in good shape now:

92% ladders operational,

85% have <1% error rate

Keeping >85% good requires a continuous effort



92% operational ladders

85% ladders < 1% error

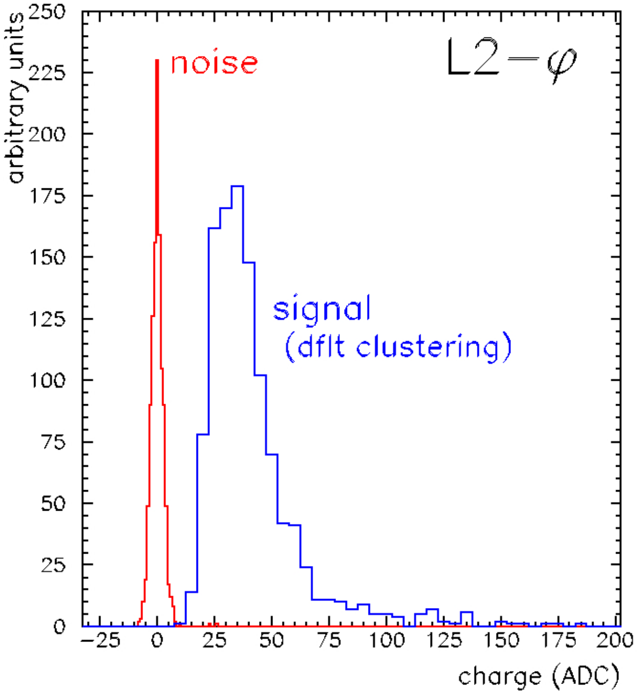
Si Performance: Charge collection

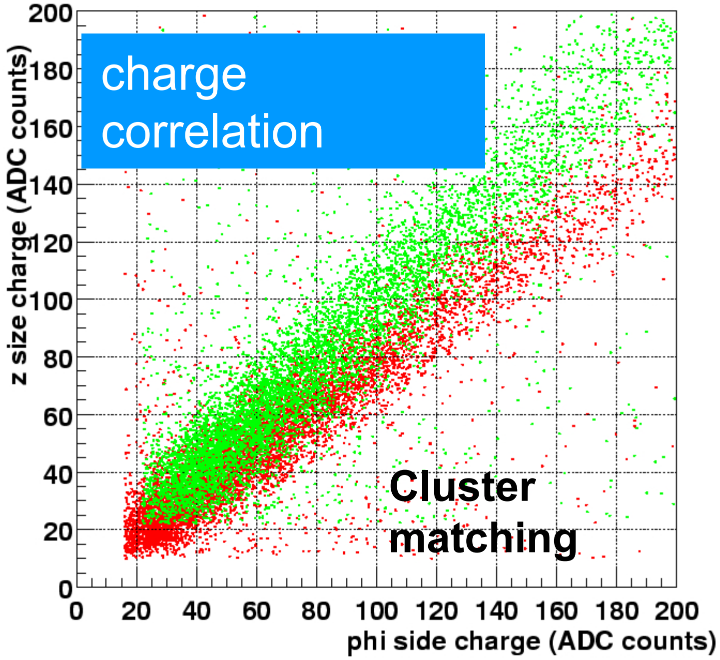
S:N	Φ	Z
L00	10:1	
SVX	14:1	12:1
ISL	12:1	12:1

S/N as designed

Charge collection efficiency > 99%

p-n side charge correlation

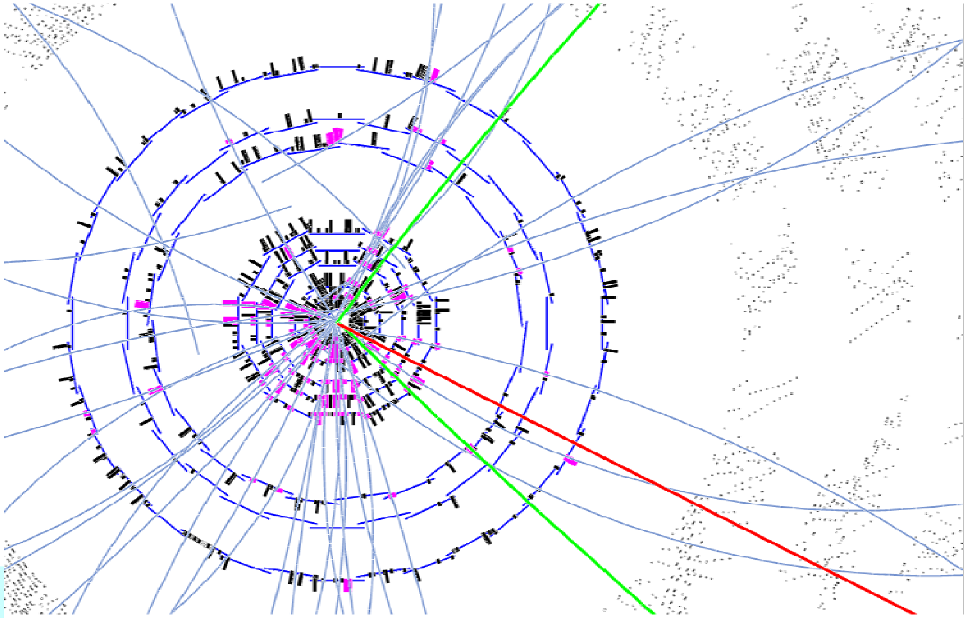




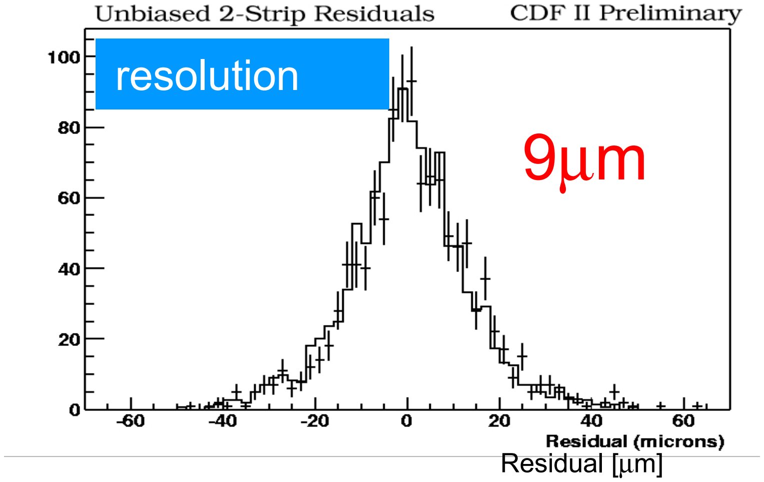
COT-Si “Outside-In” tracking

COT seeded tracking

“Progressive Road search”



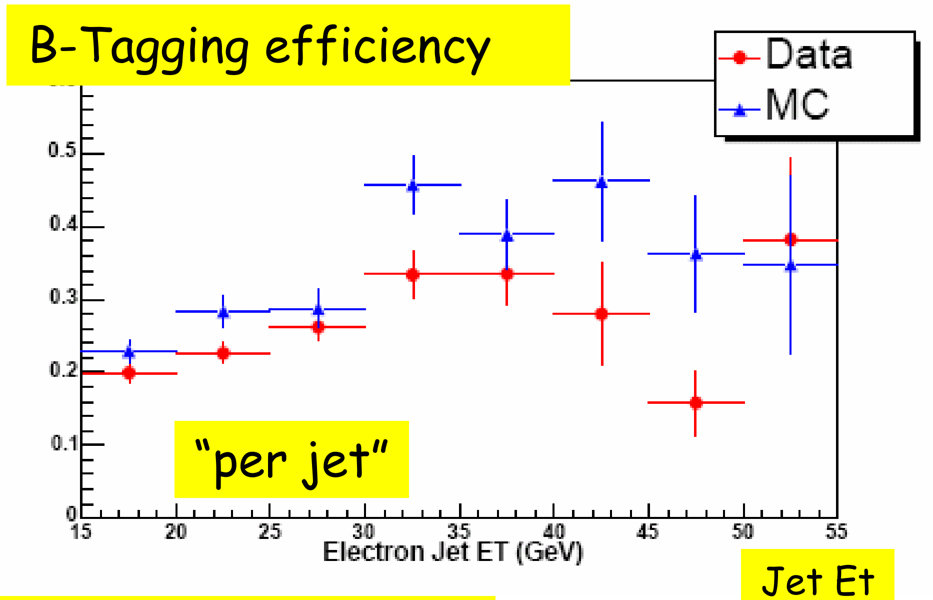
Requirement	Efficiency	Requirement	Efficiency
$N_{r\phi} \geq 3$	94%	$N_z \geq 3$	80%
$N_{r\phi} \geq 4$	90%	$N_z \geq 4$	61%
$N_{r\phi} = 5$	46%	$N_z = 5$	26%



SVX is aligned in r - Φ

Secondary Vertex Tagging

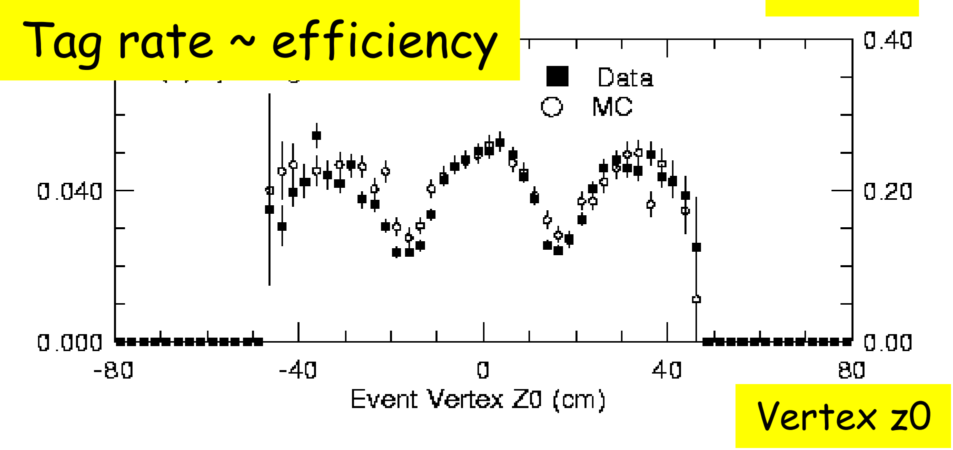
- b-tag efficiency already better than Run I
  - *e.g.* ~55% tag rate for events containing top quarks
- Tag efficiency will further increase as the full power of the detector is utilized
  - Tracks used to form vertex currently limited to $|\eta| < 1.1$
    - Forward tagging with ISL will allow tracks to $|\eta| < 2.0$
  - Visible degradation of tag rate where SVXII has gaps and/or passive material
    - This will be compensated for when L00 hits are used in tagging



B-Tagging efficiency

"per jet"

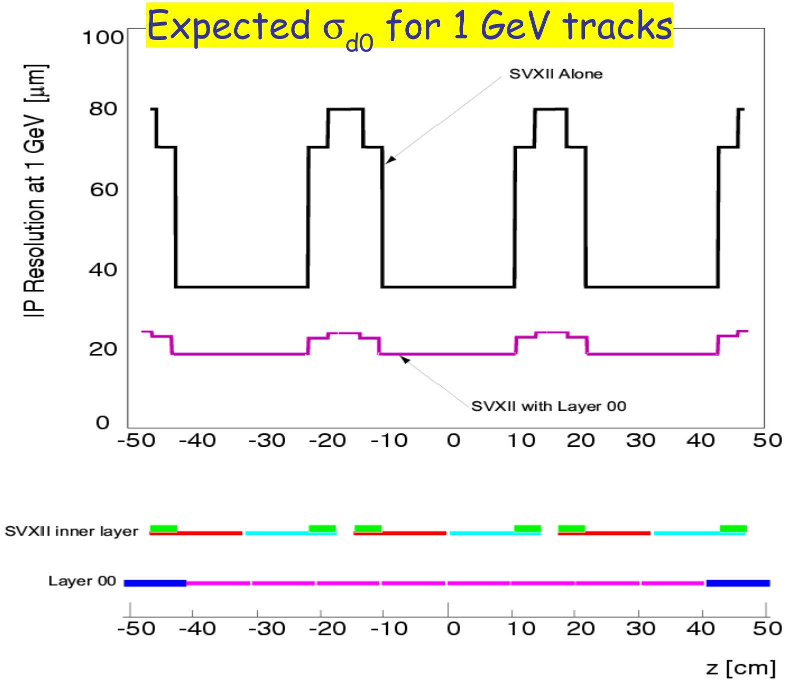
Jet Et



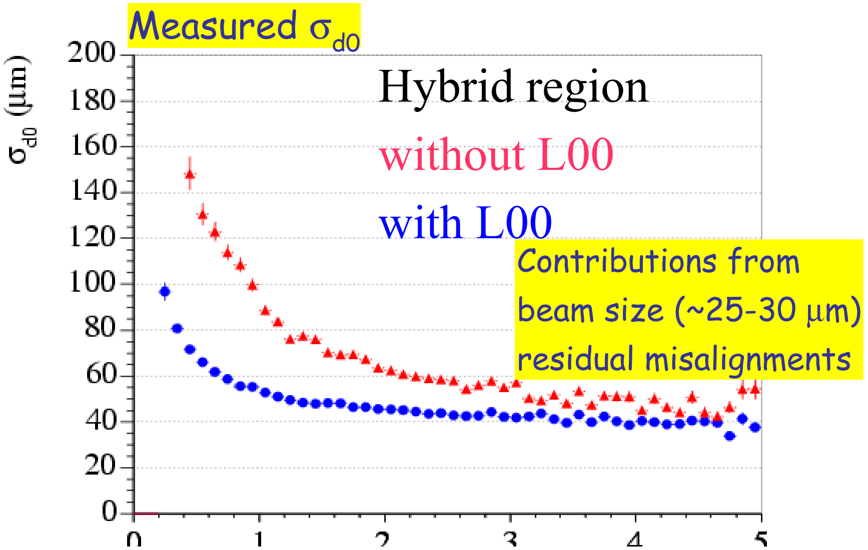
Tag rate ~ efficiency

Vertex z0

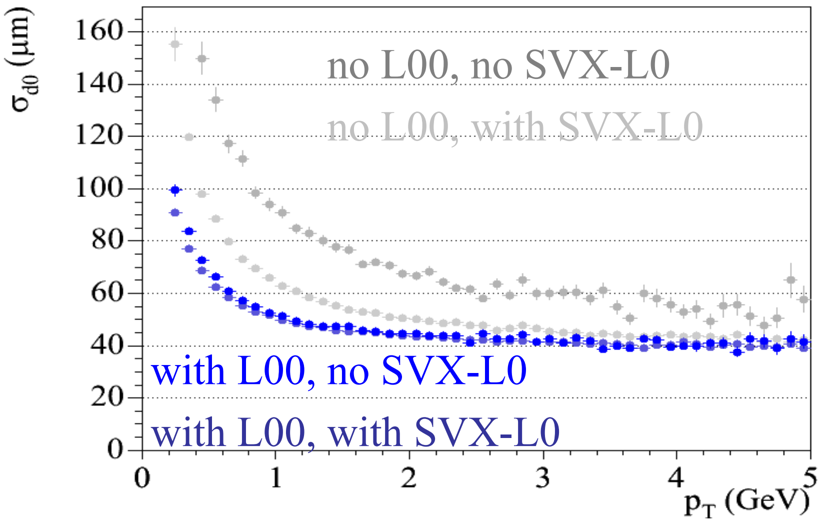
Performance: L00


Expected σ_{d0} for 1 GeV tracks

- Significant improvement at low p_T; especially for tracks in regions with more material
- Resolution is recovered for tracks without inner layer of SVX


Measured σ_{d0}

Contributions from beam size (~25-30 μm) residual misalignments



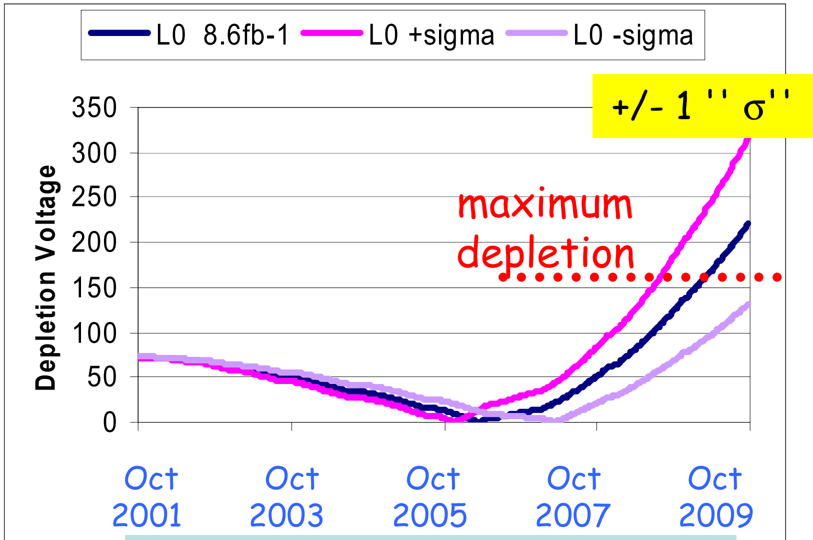
Expected Detector Lifetime

- Silicon will die either due to inability to deplete sensor or degraded Signal-to- Noise (S/N) due to high shot noise

- model calculations predict that SVX L0 sensors will have to be operated under-depleted at ~6 fb^{-1} of integrated luminosity (design goal ~ 8 fb^{-1})

BUT: Model calculations have large uncertainties

⇒ Need to monitor radiation damage via
  - Increase in leakage current
  - change of full depletion voltage V_{dep}



M.Moll RD50 parameterization compilation

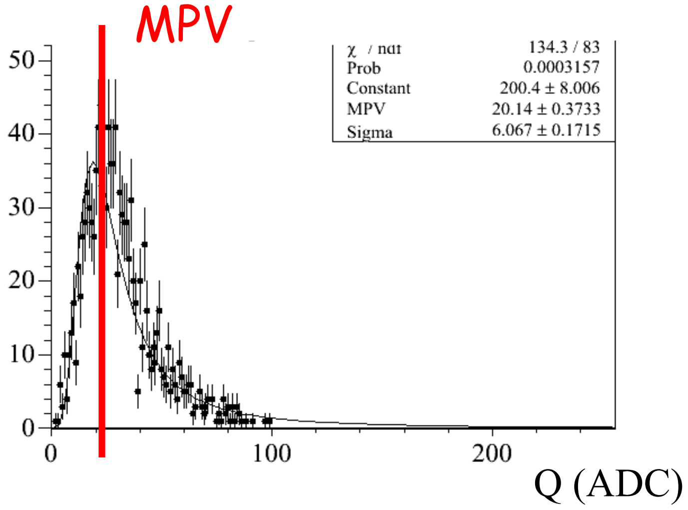
Layer	Type of Sensor	Safe Life Time fb-1	Expected Cause of Death
00	Hamamatsu	7.4	V_{dep}
00	SGS Thomp	7.4	V_{dep}
0	Hamamatsu 90	4.3(5.6)	$S/N(V_{dep})$
1	Hamamatsu 90	8.5(10.9)	$S/N(V_{dep})$
2	Micron 1.2	10.7	V_{dep}
3	Hamamatsu 90	23(30)	$S/N(V_{dep})$
4	Micron 1.2	14	V_{dep}

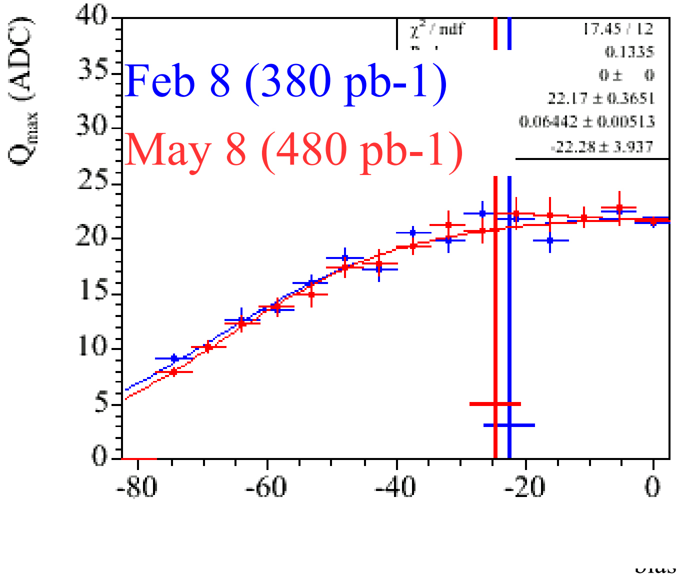
RunIIb TDR "Safe Lifetimes" prediction for RunIIa silicon detector

Ageing Studies: Depletion Voltage in L00

- Measure depletion voltage vs. delivered luminosity
  - Vary bias voltage during data taking
  - Reconstruct tracks; associate cluster
  - Fit path-length corrected charge distribution for each voltage to Landau; extract most probable value
  - Fit most probable value of Landau vs. voltage to extract depletion voltage (95% of asymptotic value)
- Average over all Hamamatsu sensors (wides) is ~ -39 ± 6 V/fb^{-1}
- No measurable change yet in SGS Thompson sensors (narrows)
- Systematic uncertainties of the method still under investigation

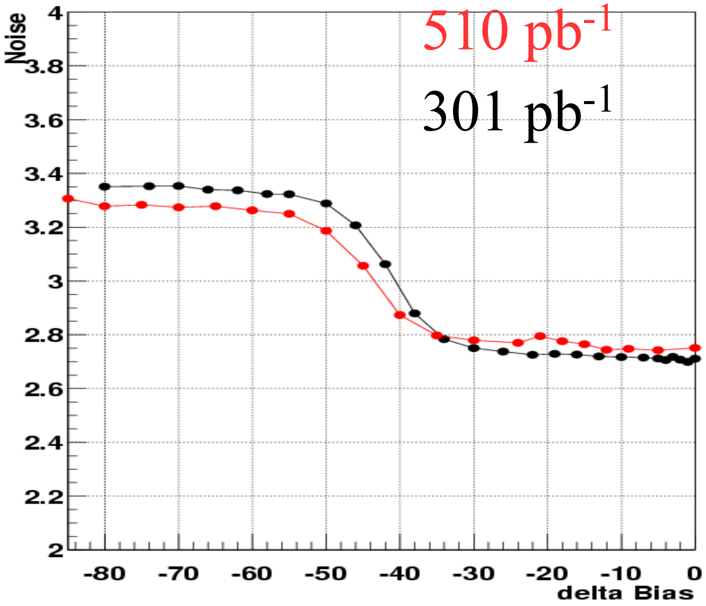
- Method works before and after type inversion
- requires substantial amount of beam time

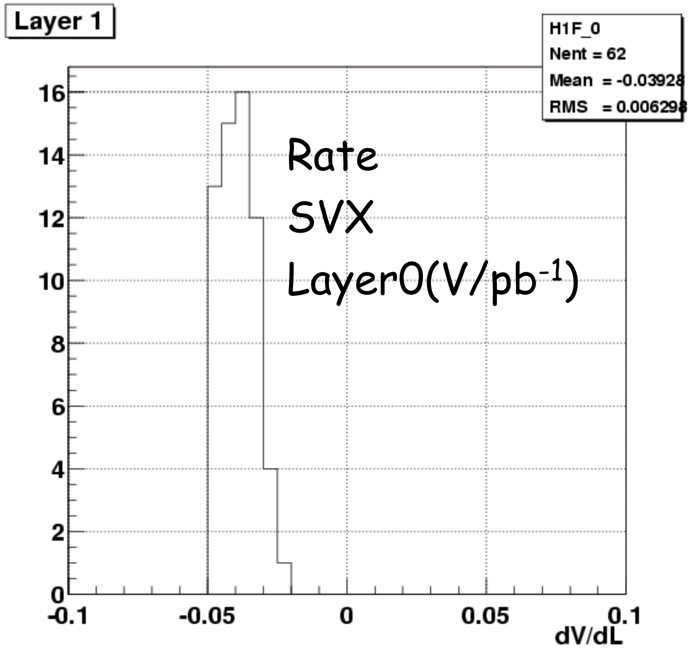




Alternative Method: Noise vs Bias Scan

- In double sided silicon sensors, noise exhibits a dip as a function of bias voltage as p-stops separate at ~V_{dep}
  - ⇒ Track V_{dep} as a function of luminosity and determine rate of change dV/dL
- Method does not require beam time
- Can't be used for L00 (single-sided)
- Won’t work after type inversion.





Rate (V/fb^{-1})

layer 0: -39.3 ± 0.7

layer 1: -26.1 ± 0.7

layer 2: -6.7 ± 0.7

layer 3: -10 ± 0.7

layer 4: 1.8 ± 0.7

layer 5: 2.5 ± 0.4

layer 6: 5.8 ± 0.5

Statistical Uncertainties only

Systematic uncertainties under investigation.

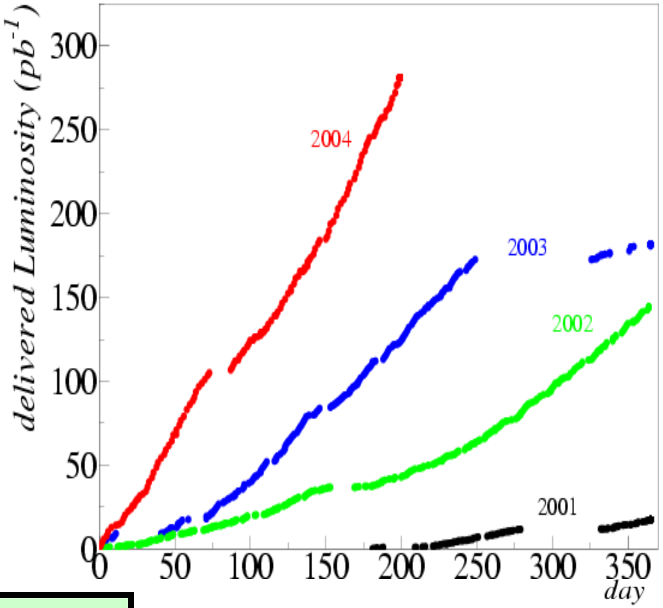
Conclusion

- Commissioning the CDF Run II Silicon detector took a longer time than expected and several challenges needed to be overcome.
- Detector is stable since ~2 years and provides high quality physics data.
- Detector performance parameters are as expected and detector potential is almost fully exploited.
- Radiation damage is visible and monitoring methods have been or are being developed. Results so far consistent with expectations.
- ***Keeping a 722k channel detector operational provides a continuous challenge to the Collaboration – there is no such thing as a free lunch.***

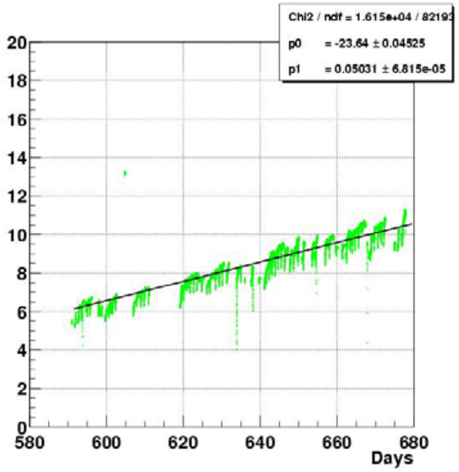
Backup Slides

Detector Lifetime: Radiation Damage

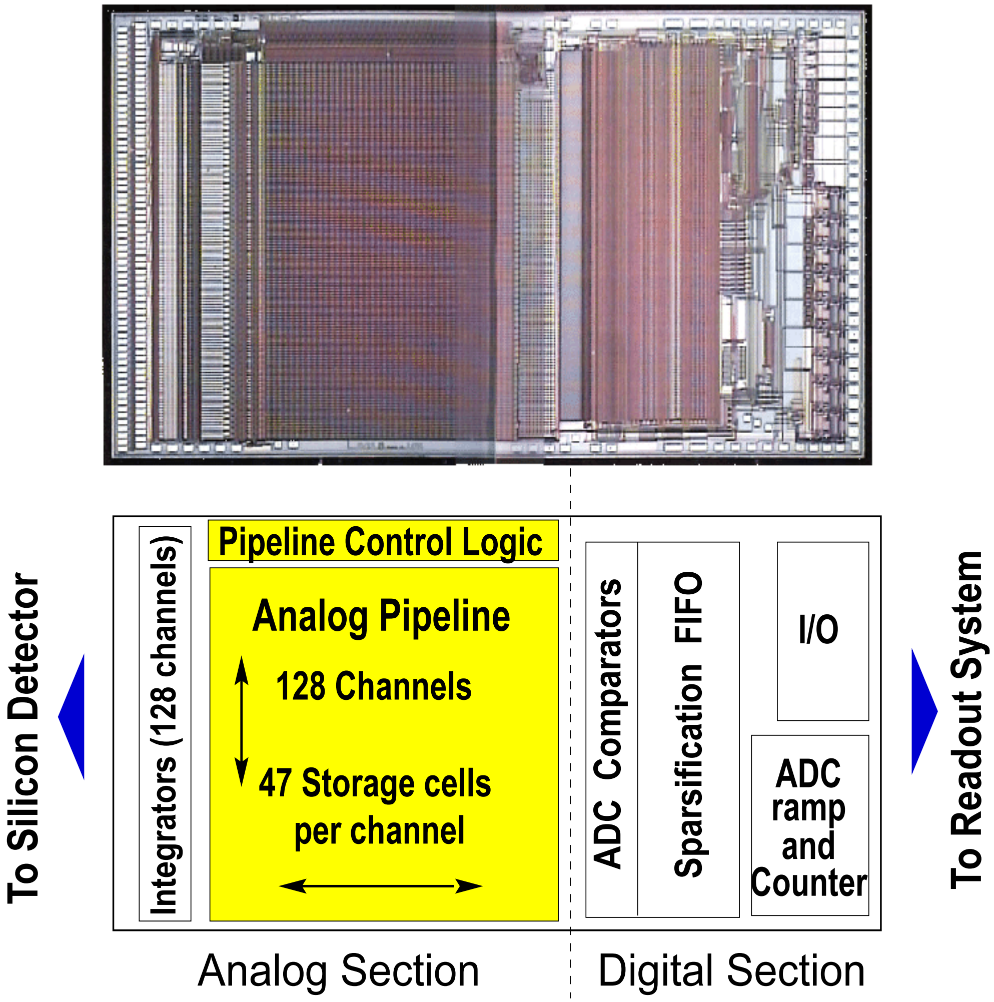
- Si Detector upgrade cancelled
- >500 pb^{-1} delivered→radiation damage measurable
  - Increase in sensor leakage current visible
- How long can current one run?



	ΔI/ ladder [μA]	RMS [μA]	Fluence 1 MeV n 1E12 $/cm^2/fb^{-1}$
Layer 00	6.47	1.93	20
Layer 0	10	1.99	9.3
Layer 1	8.1	2.00	5.1
Layer 2	5.2	2.94	2.4
Layer 3	5.88	1.60	1.8
Layer 4	4.37	2.41	1.2



The SVX3D Chip



Pipeline Control Logic

Integrators (128 channels)

Analog Pipeline

128 Channels

47 Storage cells per channel

ADC Comparators

Sparsification FIFO

I/O

ADC ramp and Counter

To Silicon Detector

To Readout System

Analog Section

Digital Section

Analog Front End (FE) and Digital Back End (BE)

FE has low noise integrator with 128 channels and 42 cell analog pipeline with 4 buffer cells

BE has comparator, ADC, and sparse readout

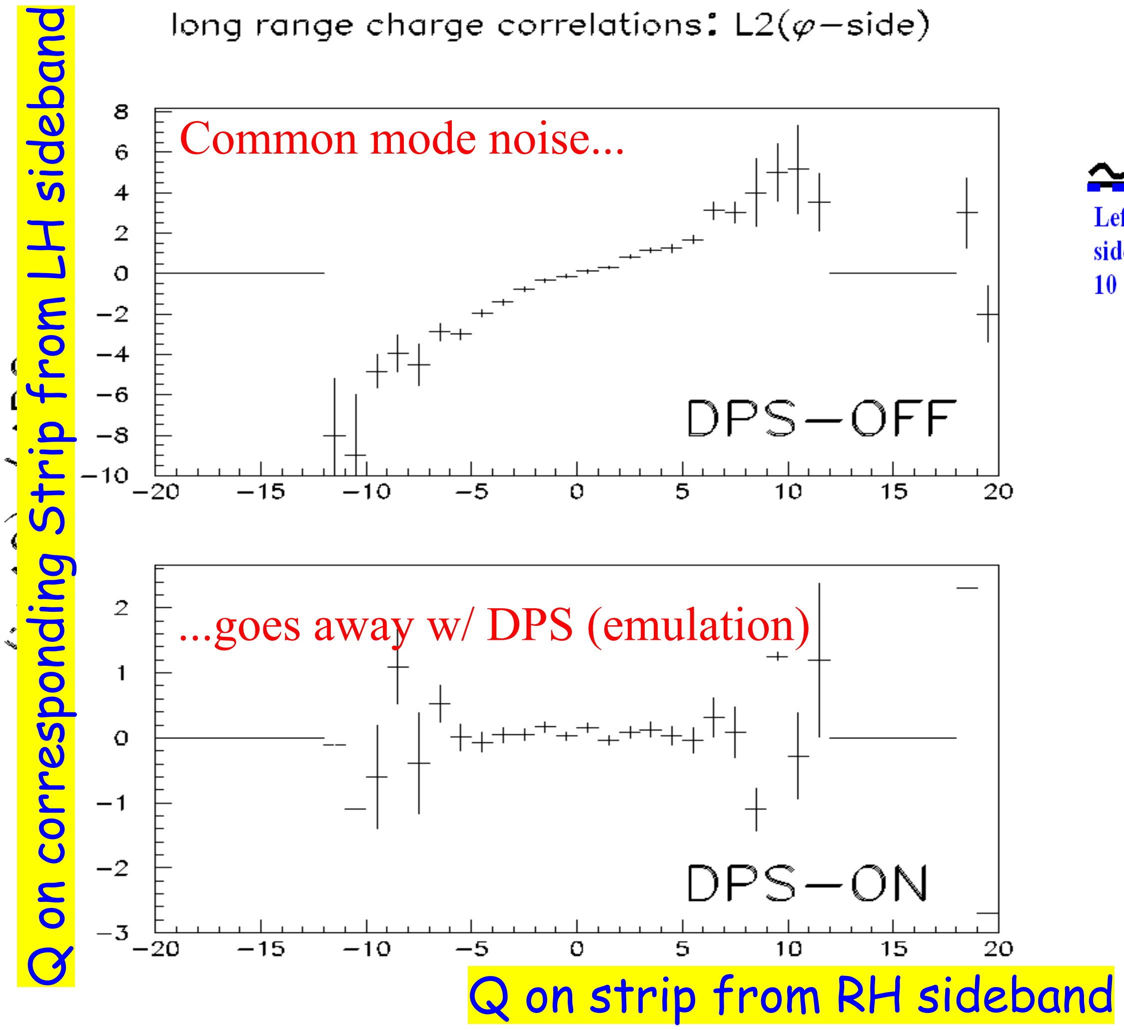
Dead-timeless:

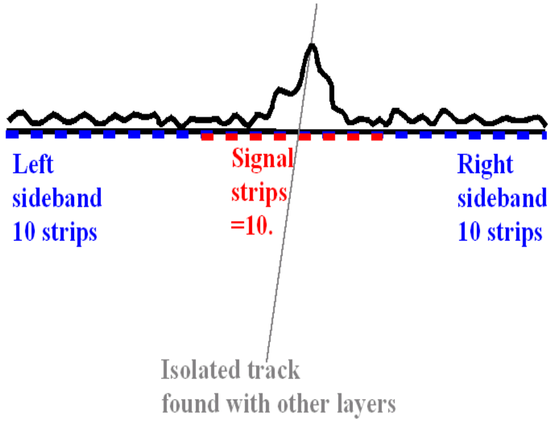
- Capable of analog operations during digitization and readout

Dynamic pedestal subtraction (DPS)

- Enables common mode noise suppression

Dynamic Common Mode Suppression

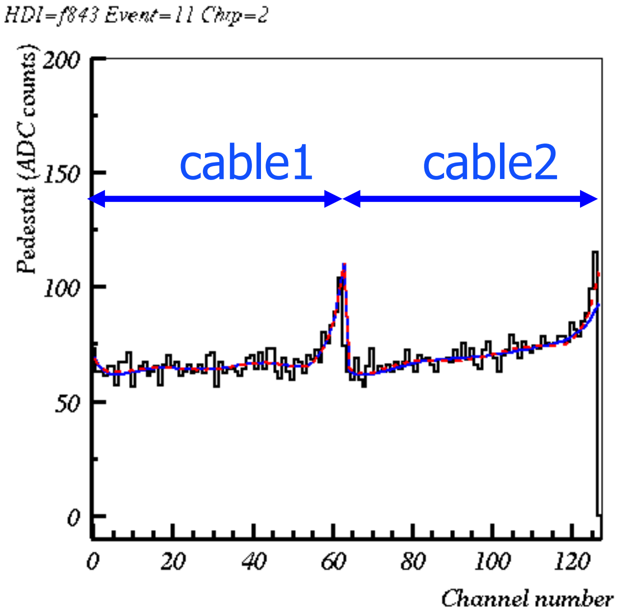


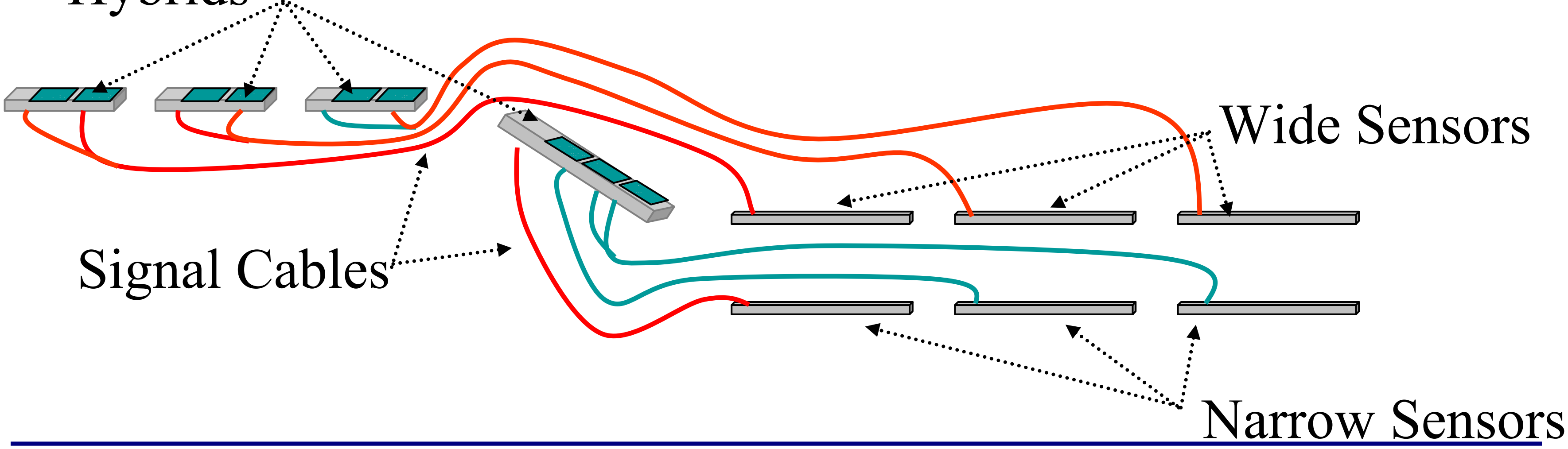


There is common mode noise on the strips, and <u>DPS suppresses it</u> efficiently.

Pickup on L00 Signal Cables

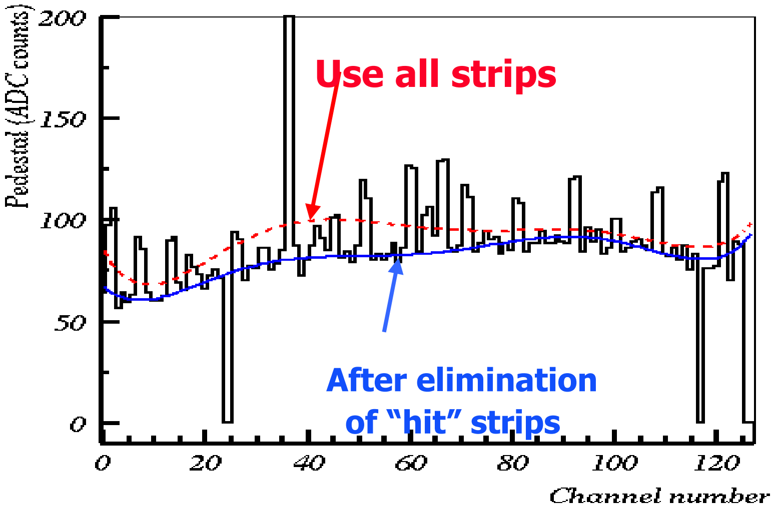
- Noise picked up by analog signal cables
  - Effects are seen at edges of cables, within one sensor
  - Both coherent and incoherent sources
    - Noise shapes
    - Pedestal shifts





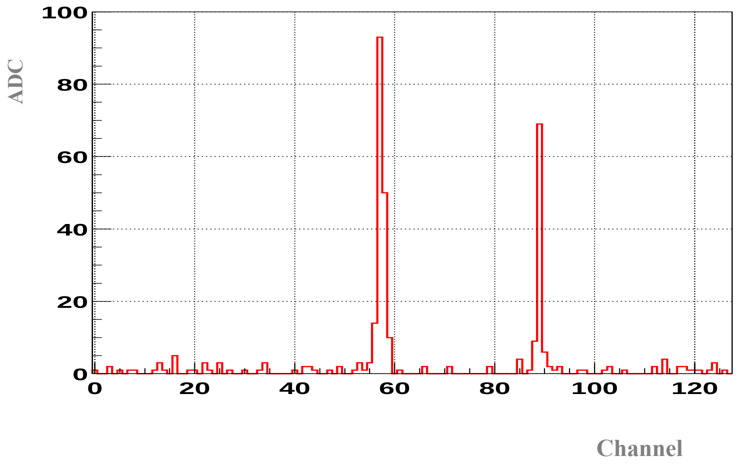
Solution: Fit for Pedestal

- Problem solved offline
  - Readout all strips in L00
  - Use this information to fit for an event-by-event pedestal
    - χ^2 fit to Chebyshev polynomials
  - Tested by embedding MC clusters in data
    - 95% efficiency with 95% purity
    - No impact on cluster size or centroid resolution
  - Implications for CDF
    - L00 can't be in online track trigger
    - Readout time may be a bottleneck

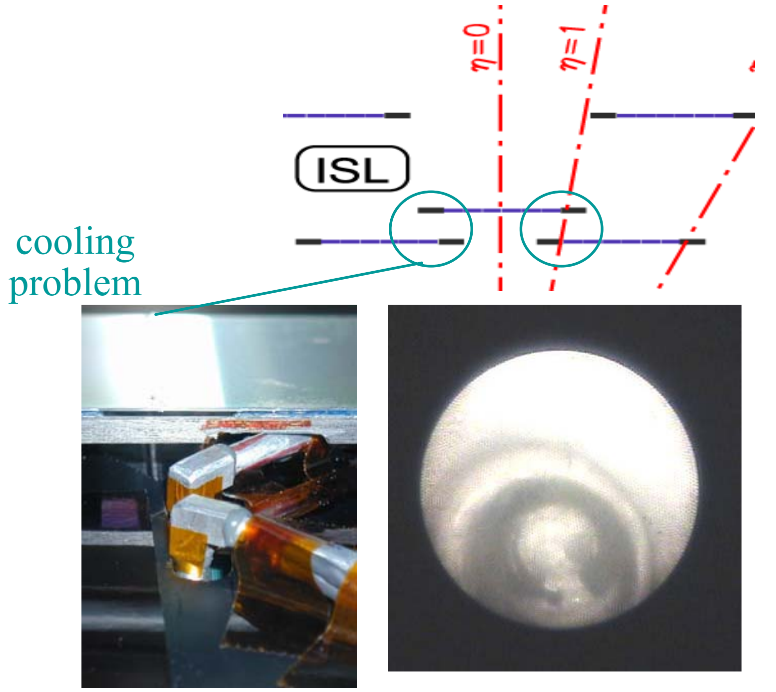


Use all strips

After elimination of "hit" strips



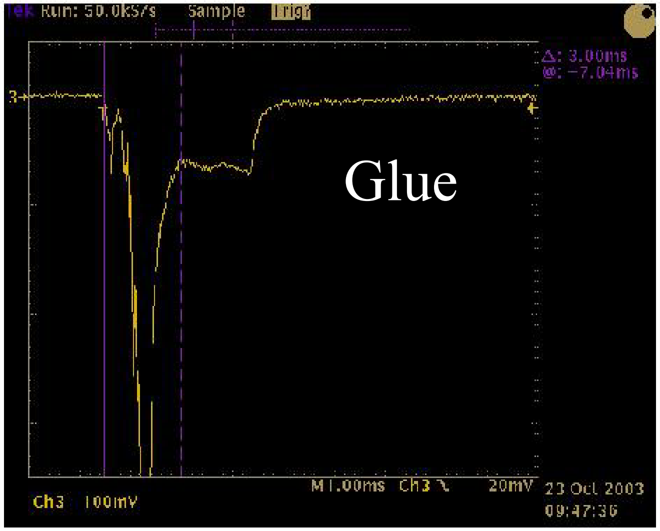
ISL Cooling Lines



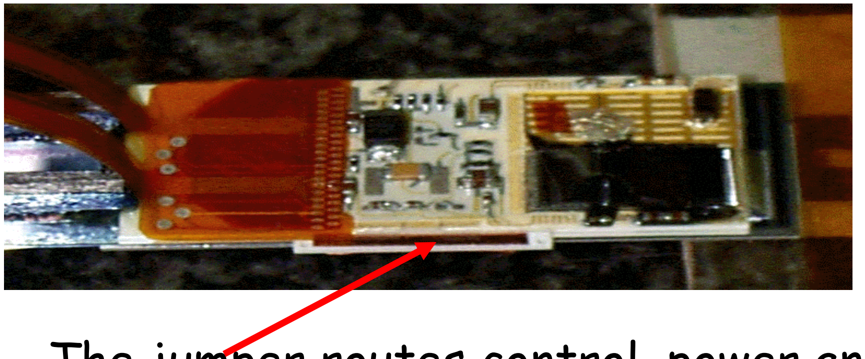
- Unable to cool central part of ISL:
- Solid blockage of Al lines experienced
- Appears at Al elbows (glue blockage seen with boroscope)
- Laser successfully opened 11/12 lines
    - PMT used for targeting to find glue

Finding the glue

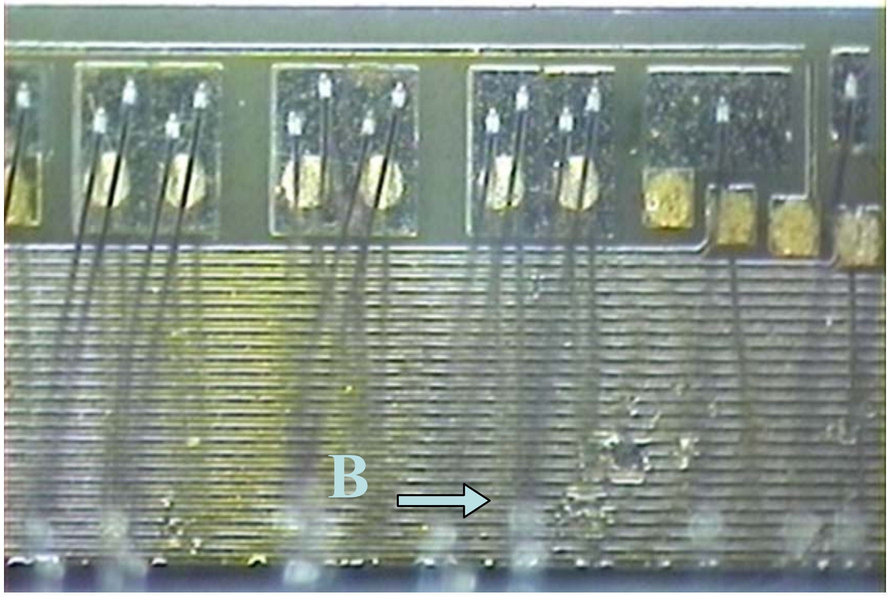
- **40W IR laser was used to find and remove the glue**
  - **Fused silica fiber optics & prisms used to direct the light**
  - **Targeted with 2 Joule pulses (determined safe for Al lines on bench)**
  - **Scattered light was observed with PMT**
    - **Glue burning had 'afterglow'**
  - **Glue was burned out with 6 Joule, 3 ms pulses**
  - **No lines were damaged**
  - **11/12 lines cleared**
    - Last line blocked by stuck prism
  - **Silicon cooled by cleared lines now takes good data**



"Jumper" Failures



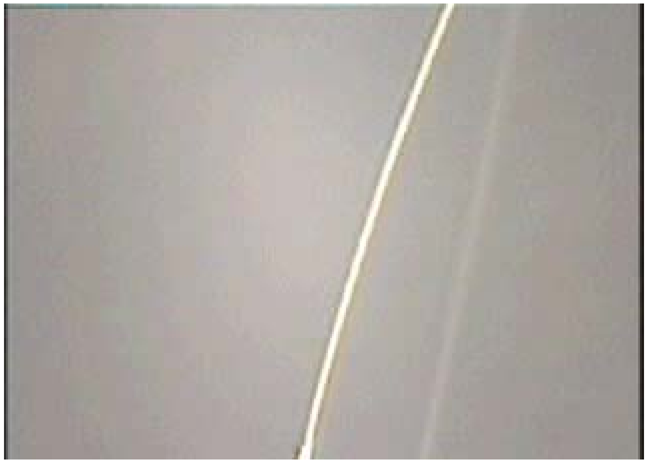
- The jumper routes control, power and data from r-φ to r-z electronics
- Loss of digital power through jumper due to:
  - Aging effects (e.g. vias) ?
    - No evidence in accelerated aging tests
  - Fusing digital wire-bonds?
    - Not reproducible in tests
    - Analog bonds carry more current
    - Power supplies and local capacitors cannot supply required energy (~100mJ)

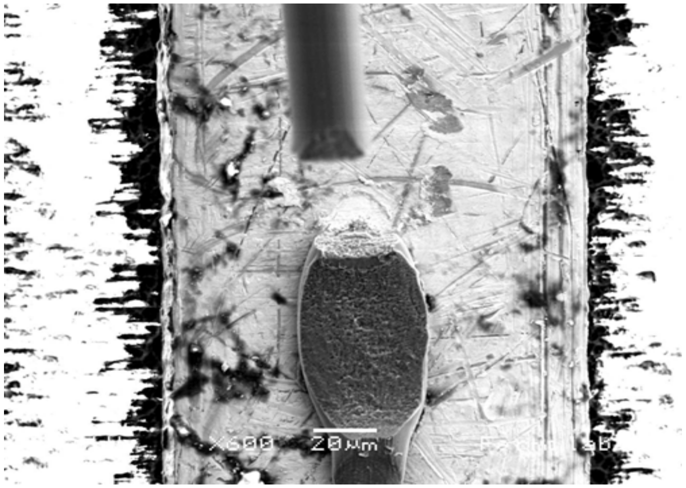


  - Mechanical damage (fatigue) to wire-bonds from Lorentz forces?
    - Jumper bonds are orthogonal to magnetic field
    - Digital bonds are unique in that current draw is dynamic
    - ΔI_{max} occurs when readout shifts from r-φ to r-z chips
      - Force applied with frequency ∝ trigger rate

Resonant Lorentz Forces

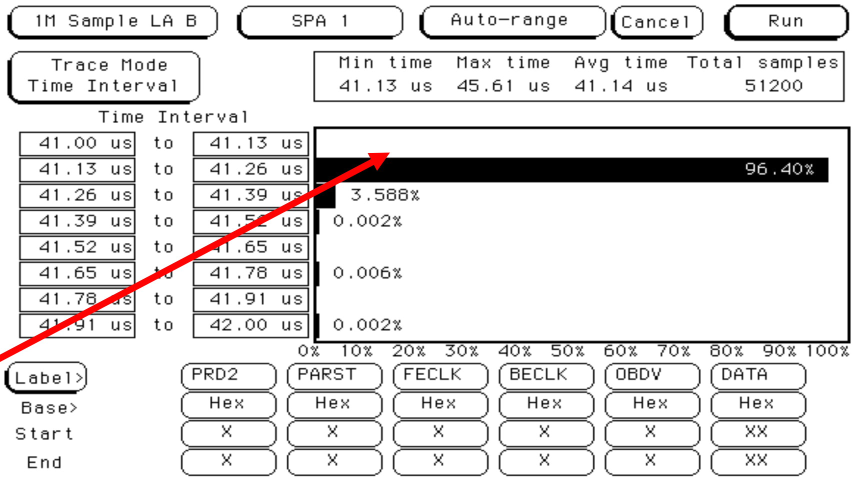
- Resonance would accelerate fatigue
  - Fundamental frequency for 2 mm AlSi bond ~ 15 kHz
- We visually searched for resonance using test bonds in 1.4T field
  - Drive w/ sinusoidal AC
  - First resonance observed
    - ~19 kHz w/100 mA
    - Bonds move several times the wire diameter (~100 um)
  - Scan current (10mA-150mA)
    - Resonance present even at 10 mA.
- After exposure to resonance for minutes-hours, bonds break
  - Break occurs at foot of bond
  - Break is due to fatigue
- Tests confirmed with real modules driven by real DAQ





Final Confirmation

- Using actual spare SVXII ladders and real CDF DAQ and real power supplies
  - Configured DAQ to readout silicon with a definite frequency
  - Scanned these frequencies, looking for resonances
  - After several days of testing … DVDD jumper bond broke!



Min time	Max time	Avg time	Total samples
41.13 us	45.61 us	41.14 us	51200

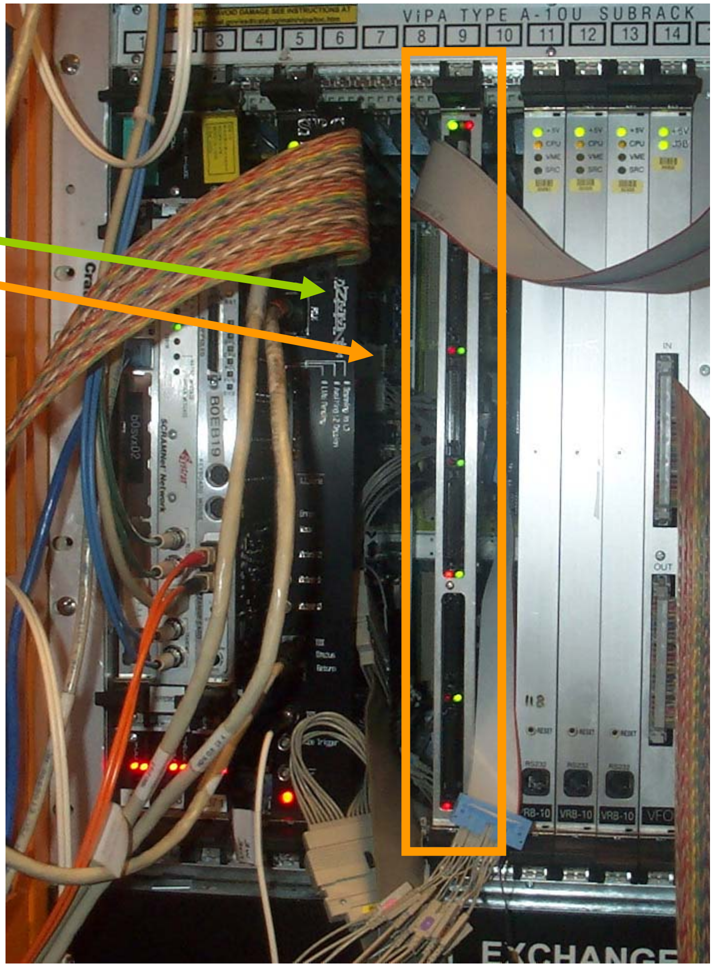
Time Interval			
41.00 us	to	41.13 us	
41.13 us	to	41.26 us	96.40%
41.26 us	to	41.39 us	3.588%
41.39 us	to	41.52 us	0.002%
41.52 us	to	41.65 us	
41.65 us	to	41.78 us	0.006%
41.78 us	to	41.91 us	
41.91 us	to	42.00 us	0.002%

Wirebond Resonance Mitigation

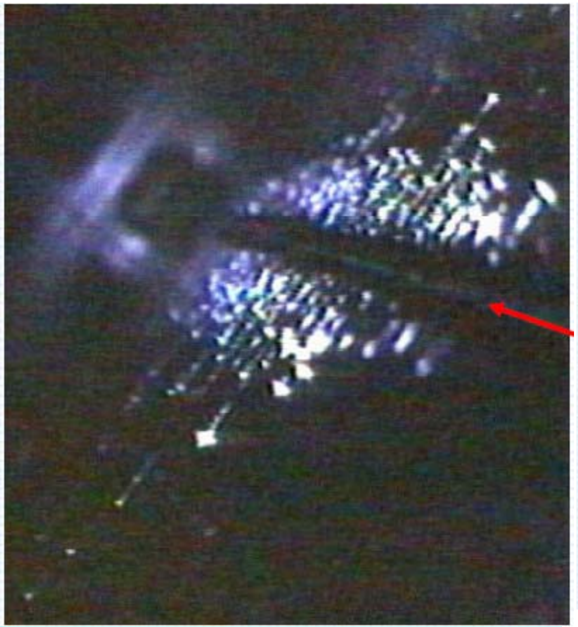
- A synchronous trigger condition detector is now operational in CDF to avoid wire bond resonances
  - Performs FFT analysis of of L1 trigger rates
  - Halts DAQ via **Silicon Readout Controller**
  - Based on dedicated **FPGA** board
  - DAQ code analyzes possible cause of synch. trigger conditions.

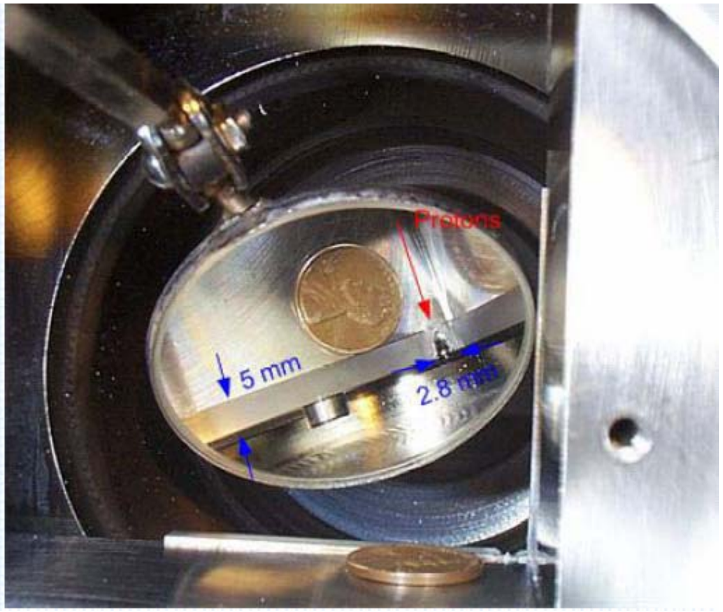
- System has been thoroughly tested – currently being migrated from prototype board to full 8 channel system

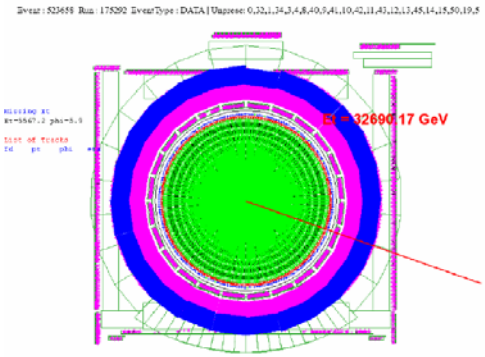
- Currently running successfully @ 25 kHz L1A rate.

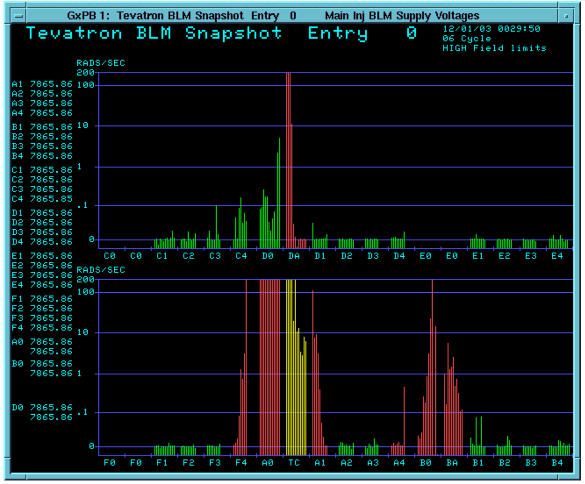


Beam Incidents

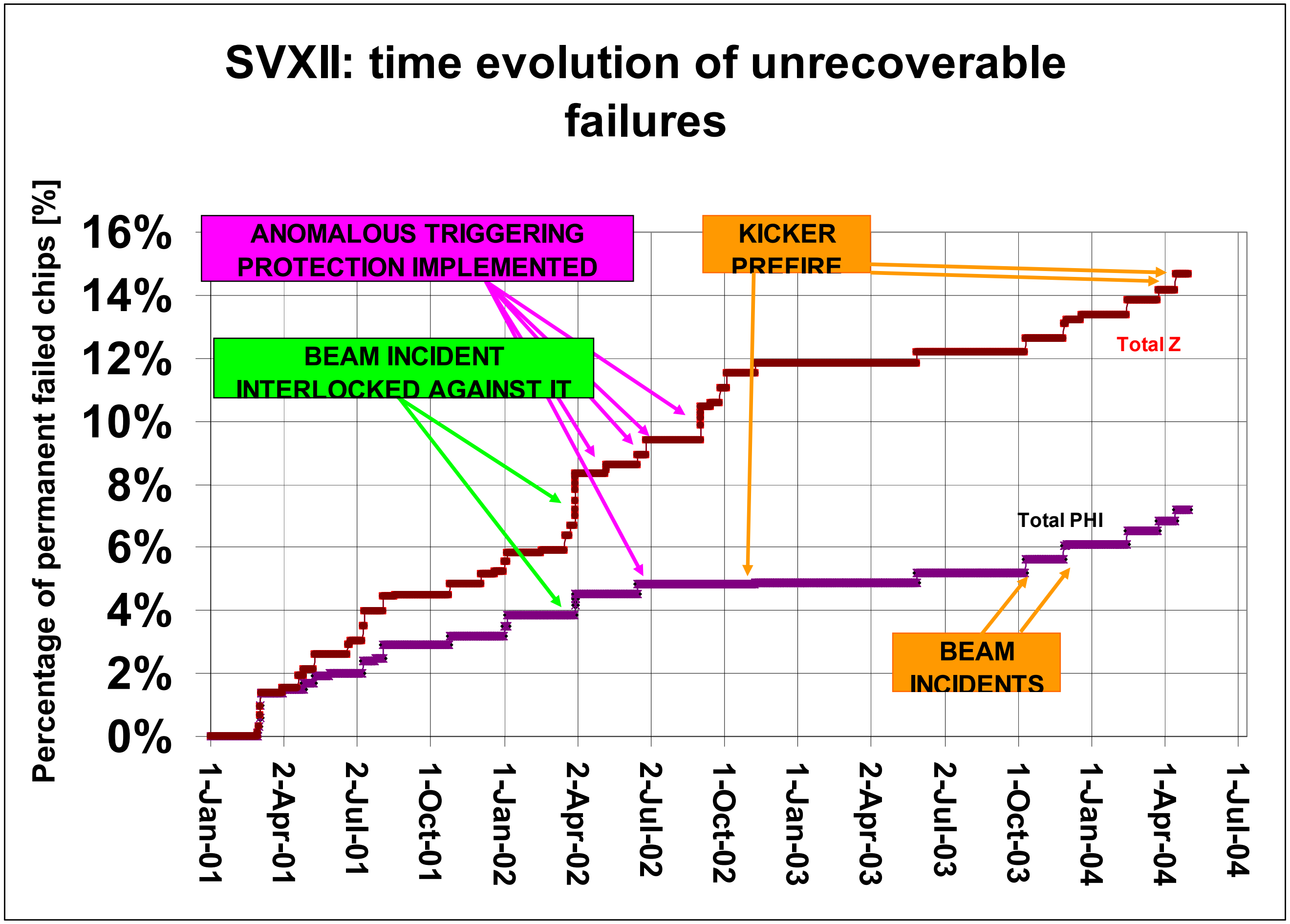








- Beam incidents are a major threat the silicon system
- Several interlock systems in place to mitigate risks – but some components of the TeV run at the limit of their specifications and occasional malfunction cannot be avoided (i.e. abort kicker prefires)


SVXII: time evolution of unrecoverable failures

Run IIb Upgrade

- Run II original plan: 15fb-1
  - Would need to upgrade inner silicon.
- Simplified design: Only two varieties of stave and hybrid (beampipe-mounted L0, "SVX")
- Only single-sided sensors
- All wirebonds encapsulated
- SVX4 chip more rad hard, included capability to remotely switch off channels
- Due to revised RunIIb luminosity, project cancelled September 2003