

ALICE Trigger and DAQ

LHC Days in Split October-2004

P.Vande Vyvre - CERN/PH

for the ALICE DAQ project (Birmingham, Budapest, CERN, Mexico, Split, Zagreb)



Outline

- ALICE DAQ
 - Trigger/DAQ logical model Requirements
 - Trigger/DAQ at LHC
 - ALICE Trigger/DAQ Architecture
- Hardware components
- Software packages
- Towards the final ALICE
- Conclusions



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	DAC LHC Beam	Event Size (Byte)	LHC Readou (HLT inp (Events/s.)	ıt ut) (GB/s)
ALICE	Pb-Pb	4x10 ⁷	2x10 ³	25
ATLAS	рр	10 ⁶	2x10 ³	10
CMS	рр	10 ⁶	10 ⁵	100
LHCb	рр	2x10 ⁵	40x10⁴	4

	Mas	ss S	tora	ge @ L	HC
ALICE			R (Mas) (Event)	ecording s Storage) s/s.) (MB/s)	Data archived Total/year (PBytes)
ALICE	Reference of the second s	Pb-Pb	200	1250	2.3
ATLAS	Aur mar in an	рр	100	100	6.0
CMS		рр	100	100	3.0
LHCb		рр	200	40	1.0





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Trigger Control Software

⊕ X VME ↓ X ↓ X ↓ ↓ ↓	crate 🔲 🖬 🖻		X							
statuncs			X 0XA00000:				(_	
CTP_Emulator	stdfuncs	cmd				start	quit	kill	Log:	None
Configuration		PID	2407 Tmain called							
Testing	InpSelTiming	pcsr	:1() 9011017							
Monitoring			V avataooo							
SimpleTests	sendL1L2		A 0x810000;				1	1	_	
SLM		cmd				start	quit	kill	Log:	None
MasterTest	primitives	PID LTUC	2404 code:56 serial#:3f	VME ver:a3 LTUf	ipga:a4					4
011	it	BC_S	STATUS: 2							
4.										
👻 🕂 🔍 🗆	IP emulator						+ (X	Input s		×
5	Sequence:	LO	.seq							
	oad sequence		8	equencer editor			Countin	ig:	Uno	
	ouu sequence					4	Trig	ger src:	Disabl	ed III
		Em	ors enabled				-		🗢 🕂	
		_	10 Hz				requenc	y:	♦ L1A	0
er	ror signal rate:		JIOTIZ				В	C delay: 9 VME OK		2
Error generation a	ulowed for: LO L2	a					L1A	FIFO emp	↑ L1A	3
Pre-nulse	0 [11]	11 Message	11811 Massana	12a Messare	12r Word		LIA	FIFO not	♦ VME	
error er	ror error	error	error	error	error	L	1A FIFO:	C	🔷 Ran	dom
	Generate 1 'Start signal' Automatic START not selector								◆ Calil ◆ Disa	bration abled
		5	S	ignal selection:		-	:	set CSR1		
Start emu	Ilation	Break	emulation	Quit emu	lation			quit		



Detector Data Links

- Standard and stable interface detector/DAQ
- Point-to-point full-duplex digital data link
- Massive parallelism (100's)
- Integrated with SDD, TPC, TRD, TOF, Muon, HMPID



Link performance

- HEP development based on commodity components:
 - Fiber Channel or Gig. Ethernet: 2.125 Gb/s
 - Optical transceiver 850 nm VCSEL
 - Flash-based FPGA (Radiation tolerant)

200 MB/s sustained Lots of bw available. Major fraction available to end application.





Links Adapters

AT CHEST

- Adapter for 1 or a few links to PC I/O bus
- A few-to-one multiplexer
- Massive parallelism (100's)





Link and adapter performance

- Currently PCI and PCI-X busses. PCI-XP (PCI Express) in the future.
- No large local memory. Fast transfer to PC memory
- PCI interface
 - IP core (VHDL code synthesized in FPGA)
 - PCI 64 bit 66 MHz. Master enabled.

200 MB/s sustained

Total PCI load: 92 % Data transfer PCI load: 83 %

Lots of bw available. Major fraction available to end application



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Subevent & event buffer

- Baseline:
 - Fast dual-port memories
 - Electronics racks are over Extensive use of dual-CPUs PCs
- Key parameters:
 - Cost/performance
 - Performance: I/O and memory bandwidth





Readout System Performance

- Supermicro server motherboard with dual Xeon CPUs @ 2.4 GHz
 - In the future: multicore CPUs from Intel and AMD
- Six PCI-X slots, 4 bus segments (3+1+1+1)
- Linux OS
- ALICE Data-Acquisition software (DATE)



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Performance: 6 D-RORCs

- Testing the fully populated PC using data source internal to PCI interface
 - Interoperability test
 - Measure the maximal input bandwidth

t 2	#4	PCI #6						1 Ch	1 Ch		
- 1	#3	PCI #5					1 Ch	1 Ch	1 Ch		
	#2	PCI #4				1 Ch	1 Ch	1 Ch	1 Ch		
ller #'	Segment #1	PCI #3			1 Ch				1 Ch		
ontro		ment	ment	PCI #2		1 Ch	1 Ch				1 Ch
0		PCI #1	1 Ch	1 Ch	1 Ch	1 Ch	1Ch	1 Ch	1 Ch		
	Ban	dwidth [MB/s]	264	464	424	528	792	1045	840		
Normalized Bandwidth [MB/s/Ch]			264	232	141.3	264	264	261.3	140		



Event Building Network

- Baseline:
 - Adopt broadly exploited standards Switched Ethernet and TCP/IP
- Motivations for switched Ethernet:
 - Performance of Gigabit Ethernet switches already adequate: 2 Tbit/s of aggregate bandwidth
 - Use of commodity items: network switches and interfaces
 - Easy (re)configuration and reallocation of resources
- Network Interface Card (NIC)
 - TCP/IP Offload Engine (TOE) Dedicated processor to execute IP stack
 - 10 Gbit Ethernet in the PCs



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~80 CPU servers 2 x 2.4 GHz Xeon, 1 GB RAM, Intel 8254EM Gigabit in PCI-X 133 (Intel PRO/1000), CERN Linux 7.3.3

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ADC V Trunking



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Mass Storage System

- Logical model: distributed file-system
- Software implementation
 - CASTOR system developed by CERN/IT
 - Accessibility via the GRID
- Baseline hardware implementation
 - Transient Data Storage
 - Located at the experimental area
 - Capacity: a few hours of autonomous data taking
 - Before archiving to tertiary storage, if any
 - Permanent Data Storage
 - Located in the computing centre
 - Infinite capacity, very low cost
 - Single write and a few read
 - Sufficient performance to achieve performances with reasonable number of parallel streams and media operations
 - ◆ 1 GByte/s: 40 active streams at ~30 MB/s
 - 1 media operation every 2'30" with 200 GB/volume
 - Open to new implementations thanks to software model

Possible Transient Storage







Transient Data Storage

- Transient data storage at the experimental area
- Baseline
 - Storage arrays of commodity disks
 - Box attachment: Fibre Channel
 - Disk attachment: IDE or serial-ATA
 - RAID-level
- Partnering with industry for test of equipment
- Key selection criteria:
 - Cost/performance
 - Bandwidth/box
 - Robustness



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Storage Arrays

dotHILL SANnet II 200 FC

- 12 fiber channel disk slots
- 1 GB cache
- 1 x 2Gbit fiber host channel
- Infortrend IFT-6330
 - 12 IDE drive slots
 - 128 MB cache
 - 2 x 2Gbit fiber host channels





 Infortrend EonStor A16F-G1A2 (INFN CASPUR Storage Lab)

- 16 SATA drive slots
- IGB cache
- 2 x 2Gbit fiber host channel

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Storage Arrays Performance

- Aggregate throughput measured for
 - Set of 5 disks configured as RAID 5
 - Filesizes of 100, 300, 1024 and 2048 MB
 - Recl=8 kB, 32 kB, 128 kB, 512 kB, 2 MB, 8 MB, 32 MB and 128 MB





Permanent Data Storage (1)

- Permanent data storage in the computing centre
- Baseline solution
 - Magnetic tape
- Critical areas
 - High Energy Physics peculiar use of tapes
 - Infrastructure hidden by a hierarchical storage management sw
 - Limited market, different application
 - Limited competition
 - No demonstrated alternative yet
- Demonstrated solution for LHC
 - 15 parallel streams









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DAQ Software Framework

- DAQ Software Framework
 - Common interfaces for detector-dependant applications
 - Address all configurations and all development phases
- DAQ Software
 - Complete ALICE DAQ software framework in 3 packages:
 - DATE:
 - Data-flow: detector readout, event building
 - System configuration, control (1000's of programs to start, stop, synchronize)
 - AFFAIR: Performance monitoring
 - MOOD: Data quality monitoring
 - Production-quality releases
 - Evolving with requirements and technology ⇒ home-development

Key issues

- Scalability (1 to 1000, demonstrate it)
- Support and documentation



Data Flow - DATE

RUN Control		SD 1						
<u>File View Options Windows</u>	-	LDC status display						
		LDC name	tbed0001ldc	tbed0013ldc	tbed0030ldc	tbed0037ldc		
DAQ = Rup Control	പ	Event rate	13	13	14	13		
	7 T	Bytes recorded rate	40.182 M	41.203 M	41.938 M	40.163 M		
		Bytes in buffer	C 1192% M 1195%	C 1188% M 11939	C 1192% M 1194	% C 1187% M 119		
DOMAIN+ divia23073	Number of events	10453	10462	10457	10450			
		Events recorded	9816	9825	9820	9813		
		Bytes injected	31'031'205'136	31'057'922'896	31'043'079'696	31'022'299'216		
$\begin{array}{c c c c c c c c c c c c c c c c c c c $	Data Taking	Bytes recorded	29'141'863'284	29'175'752'364	29'154'396'136	29'140'480'912		
Define Start run	Stop run	Readout SOR/EOR phases	0	0	0	0		
Show 📕 Run AutoStart	Pause trigger	Recorder SOR/EOR phases	0	0	0	0		
Autoset GDC	Abort run					\square		
📕 Recording Enabled 🖃			GDC stat	us disp	lay			
📕 AFFAIR 📕 EDM		GDC name	tbed0003c	dc tbed0004	gdc tbed001	4qdc tbed001		
I ALIMDC I HLT		Events received	4924	5170	5438	3505		
DIN NUMPER : 1705 DAG Lagia Engine Status : DUNNING		Events recorded	622	639	673	432		
KON NOMBER : 1785 DHQ LOGIC Engine Status : KONNING		Bytes received	14'588'026'9	44 15'347'910'	144 16'167'256	896 10'428'860		
Into: Kun 1785 running		Bytes recorded	14'392'096'2	56 15'175'728'	576 15'983'200	832 10'259'64:		
Trace Fri 13 11:07 Run 1785 running		Event builder SOR/EOR ph	ases 0	0	0	0		
Clear Fri 13 11:07 Run number saved on ruade siderad/configuradon files/run number.com	'g	Status	FULL	FULL	FULL			
Debug Fri 13 11:07 * Message from tbed0029gdc: TRACE STOP_PROCESS: EVB 3223 has	s been killed as r							
Fri 13 11:07 * Message from tbed0029gdc: ACTION End of run requested with error Pause Fri 13 99:10 * Management the 109 40 days ERD OR file Materia from the 109 40 days	r Duna ak uwakilawa		FDM stat	us disn	lau			
Fri 13 05:10 * Message from deduodsido: ERROR hie /date/runcontrol/Linux/check	Proc.sn problem	EDM name		ed0015edm	209			
Fri 13 08:05 Run number saved on /dateSiteAdc/configurationFiles/runNumber.confi	ig	wakeUpId received (nbln	Run:10442)					
Smaller	∇	maxWakeUpId (nbin	Run:10442)					
roou@upeaooor:~		lastThresholdSent (nbln	Run:10454)					
11:21am up 78 days, 22:29, 1 user, load average: 1.73, 1.69, 1.62 90 processes: 87 sleeping, 3 running, 0 zombie, 0 stopped	11 86	lastUpperBoundSent (nbln	Run:10464)					
CPU0 states: 2.0% user, 50.5% system, 1.2% nice, 46.1% idle	CPU	edmMask [0]:00	040000 [1]:00000100)				
Men: 384356K av, 374564K used, 9792K free, 3020K shrd, 1475401	K buff Her	Excluded 3.4.1	4 26 29 41 50 51 64	65 74 75 96 97		-		
Swap: 1044184K av, 26364K used, 101/820K free 1524561	K cached Swa	<u> </u>						
PID USER PRI NI SIZE RSS SHARE STAT XCPU XMEM TIME COMMAND 15208 nobody 14 5 4080 4080 3644 N 9.9 1.0 13:09 recorder 1334 root 9 0 2332 2284 1592 5 0.5 0.5 21:39 sshd 1574 root 9 0 1060 1060 820 R 0.3 0.2 30:05 top 3 root 9 0 2368 2364 1856 R 0.1 0.6 3:17 xterm 5070 nobody 8 0 4004 3976 1468 0.1 1.0 10:00 rcserver 1 root 9 0 0 SWN 0.0 0.0 10:00 keventd 4 root 19 0 0 SWN 0.0 0.0	LCPU0 157 41 LCPU0 157 42 LCPU1 184	PID USER PRI NI 330 nobody 14 5 363 alicemdc 13 5 701 root 14 0 3 root 19 19 31 root 9 0 196 root 9 0 195 root 9 0 196 root 9 0 197 root 14 0 2 root 8 0 4 root 19 19 5 root 9 0 6 root 9 0 7 root 9 0 8 root 9 0	SIZE RSS SHARE 187M 187M 187M 188M 188M 187M 188M 188M 187M 192 948 748 1052 1052 00 0 0 0 2176 1724 1495 1924 1924 1732 1935 1080 964 488 440 424 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	STAT ZCPU XM R N 43.5 50 S 1.9 0 R V 23.5 50 S 1.9 0 R V 23.5 50 S 1.7 0 R V R 0.7 0 R 0.3 0 0 S 0.3 0 0 S 0.1 0 0 S 0.0 0 S S 0.0 0 0 S 0.0 0 S S 0.0 0 S S 0.0 0 S S 0.0 0 S S 0.0 0 S	TIME COMMU. 0 5:23 ever 1 3:47 writ .2 1:56 top .2 1:56 top .0 2:116 ksof .1 0:00 slee .5 0:14 ntpo .2 0:55 xloa .1 0:20 inti .0 0:00 keve .0 21:13 ksof .0 1:38 ksua .0 0:00 kere .0 0:00 kere .0 0:00 kere	IAND tBuilder eCastor_v3 tirqd_CPU0 p ind intd tirqd_CPU1 pd ilaimd ush lated		

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Control - DATE





DATE Scalability in ADC V

-	ADCV_CONTROLS::ALLDETECTORS_CONTROL_			SMI Status			
File Yiew	/ Options Windows	GDC (91)					
	BAQ – Run Control HI running on tbed0001.cern.ch with PID 29758 RC running on tbed0001.cern.ch	NOT RUNNING STARTING ALIMDC STARTING_EVB RUNNING RUNNING_ERR STOPPING_ALIMDC WAIT_STOPPED OTOPPED					
Disconr Configu Define Show	connected > Ready to start Data Take ration Run Parameters Start processes Start Define Recording Enabled Abort GDC ON ALIMDC EDM	LDC (71) NOT PERMING SYNCHRONOUS STARTING STARTING EDM STARTING HETA	C DRDER GENT				
		STARTING_EDM	DOUT				
RUN NUM	BER : 5443 Run Control Status : RUNNING	RUNNING					
Trace Clear Debug Pause	Tue 26 15:42:46 (RC) Run number saved on /dateSiteAdc/configurationFiles/ALLDETECTORS/ru Tue 26 15:42:45 (HI) Run Options loaded from : /dateSiteAdc/configurationFiles/ALLDETECTORS/ru Tue 26 15:42:45 (HI) Start processes time : 32 seconds Tue 26 15:42:13 (RC) Starting run 5443 Tue 26 15:42:13 (RC) Run Options loaded from : /dateSiteAdc/configurationFiles/ALLDETECTOR Te 26 15:42:13 (RC) Run Options loaded from : /dateSiteAdc/configurationFiles/ALLDETECTOR	STOPPING_REAL STOPPING_EDM STOPPING_HLTT STOPPING_RECT STOPPING_EDM STOPPED	AGENT AGENT ORDER C				
	Tue 26 15:42:13 (HI) RC options saved as : /dateSiteAdc/configurationFiles/ALLDETECTORS/AD			SD		ाती	
Bigger	Tue 26 15:41:58 (HI) Connection time 34 seconds		LDC at a	tuo dion	lau		
Smaller	Tue 26 15:41:29 (RC) Starting Logic Engines at 26 Aug 2003 15:41:28 (Wait)		LDC Sta	itus arsp	тау		
	Tue 26 15:41:24 (RC) Connecting to thed0082ldc	LDC name	tbed00011dc	tbed0002ldc	tbed0003ldc	tbed0004ldc	
	Tue 26 15:41:24 (RC) Connecting to the d00801ac	Event rate	3//	311	297	330	
	Tue 26 15:41:24 (RC) Connecting to thed0079ldc	Bytes recorded rate	38.453 M	31.852 M	30.443 M	33.814 M	
	Tue 26 15:41:24 (RC) Connecting to tbed0078ldc	Bytes in buffer	C 40% M 40% 6	38 C 39% M 39% 623	C 39% M 39% 62	0 C 40% M 40% 6	
	Tue 26 15:41:24 (RC) Connecting to thed0077/dc	Number of events	8645	7/61	7580	8533	
	Tue 26 15:41:24 (RC) Connecting to tbed0075ldc	Events recorded	8008	7126	6944	7896	
	Tue 26 15:41:24 (RC) Connecting to tbed0074ldc	Bytes injected	886056720	795453792	776902740	8/45//616	
	Tue 26 15:41:24 (RC) Connecting to thed0073ldc	Bytes recorded	822185216	/3310//96	714808848	811135200	
	Tue 26 15:41:24 (RC) connecting to thed0072ldc	Readoul SOR/EOR phases				0	
	Tue 26 15:41:24 (RC) Connecting to thed0070ldc	Recorder SON/EON priases		U	lo.		
	Tue 26 15:41:24 (RC) Connecting to thed0069ldc						
	Tue 26 15:41:24 (RC) connecting to the double of the doubl		GDC Sta	itus disp	Tay		
	Tue 26 15:41:24 (RC) Connecting to thed0066ldc	GDC name	tbed000	1gdc tbed0002	ydc tbed000:	<mark>3gdc tbed000</mark>	
	Tue 26 15:41:24 (RC) Connecting to tbed0065ldc	Events received	5007	4872	4726	4658	
	Tue 26 15:41:24 (RC) Connecting to thed0064ldc Tue 26 15:41:24 (RC) Connecting to thed0063ldc	Events recorded	145	3	2	2	
	Tue 26 15:41:24 (RC) Connecting to tbed0062ldc	Bytes received	563359168	560661364	542728828	53371316(
-		Bytes recorded	65782276	64823208	43215472	43215472	
<u> </u>		Event builder SOR/EOR ph	ases 0	0	0	0	
		Status					
		1					



DAQ Configuration Database

- DATE Configuration Database
 - Operator console
 - State machines
- Home-made development based on free software (MySQL)

Alice Data Base	Roles	
Detectors Partitions	Name a1 Roles list Role Detector New a1 ID 111 a3 a4 Hostname ID	•
Memory banks Event building rules	Add AloneLdc Top level Image: Construction Add DetOne Active Image: Construction Suppression DetOneLdc2 Tree structure ->	•
Event building patterns Variables	Triggers -> Commit Rollback Qu	iit
Quit		

Web access to Configuration Database

Mozilla

	<u>F</u> ile	<u>E</u> dit	<u>V</u> iew	<u>G</u> o	<u>B</u> ookma	rks <u>T</u> oo	ls <u>W</u> indow <u>H</u> elp	
•	ack	•	Forward	Ŧ	3. Reload	Stop	🗼 http://localhost/date/dumpconfig.php	-
•	🚮 Hor	ne 🔤	🐠 Bookm	narks				

Connected successfully to DATE database

Roles

Name	Hostname	Description	Role	Id	Toplevel	Madeof	
gdc1	host8	GDC #1	GDC	1	1	1	Undefined
gdc2	host9	GDC #2	GDC	2	1	1	Undefined
DetOneLdc1	host1	DetOne LDC #1	LDC	1	0	1	Undefined
DetOneLdc2	host2	DetOne LDC #2	LDC	2	0	1	Undefined
DetOneLdc3	host3	DetOne LDC #3	LDC	3	0	1	Undefined
DetTwoLdc1	pcald37	DetTwo LDC #1	LDC	10	0	1	Undefined
DetTwoLdc2	host5	DetTwo LDC #2	LDC	11	0	1	Undefined
AloneLdc	host7	Single LDC	LDC	30	1	1	Undefined
DetThreeLdc	host6	DetThree LDC	LDC	160	0	1	Undefined
DetOne		Detector 1	Detector	1	1	1	Subdetector
DetTwo		Detector 2	Detector	2	1	1	LDC
 .	1			_			:

Performance Monitoring - AFFAIR





Data quality monitoring - MOOD

- MOOD framework
 - Interfaces to detector code
 - Software development in all institutes
- Applications:
 - Raw data integrity
 - Detector performance





Data quality monitoring - MOOD

Event: "377" Timebin: 0-1000





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Combined ITS test beam





DAQ for ITS Test Beam



Control for ITS Test Beam



File

0



Simulation

- Complete model of the ALICE TRG/DAQ
- See next 2 talks:
 - Tome Anticic
 ALICE Trigger and DAQ Simulation
 - Linda Vickovic
 - **ALICE Mass Storage System Simulation**



Conclusions

- ALICE TRG DAQ system
 - All major hw and sw components released
 - Production phase
- Towards the final system
 - Integrated with most major detectors
 - First combined test beam
 - Simulation
- System evolution
 - New technology: PCI-XP, multicore CPU, 10 Gbit Eth
 - Isolate from technology obsolescence by logical interfaces (DDL or Mass Storage System)
- Start installation 1Q 2005. Startup 1Q 2007