Radhard Electronics for LHC Experiments

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The context

- LHC is at the convergence of two phenomena:
  - First generation of accelerators with significant radioactivity problem for detector and electronics (and of course for the machine itself)
  - Detectors are so large that they can be technically, functionally and economically instrumented only through custom designed components
- Microelectronics has been enthusiastically embraced by the physicists and engineers building detectors
- The community of experimentalists has jumped in the design of several dozens ASICs with a relatively little previous practical background
- Successes and mistakes have taught us valuable lessons
  - Technical
  - Organizational
- Meanwhile Industry is progressing still at exponential growing rate…

The Issues

- Experiments have heavily invested in custom ASICs
- LHC experiments can not exist without custom electronics
- From here:
  - Can this model be extended ?
  - What needs to be designed next and how ?
  - What are the benefits ?
  - What are the costs ?
  - Where does it make sense ?
  - Which mistakes should be avoided (i.e. from what should other people learn)
  - What organization is necessary to design ASICs successfully ?

Outline

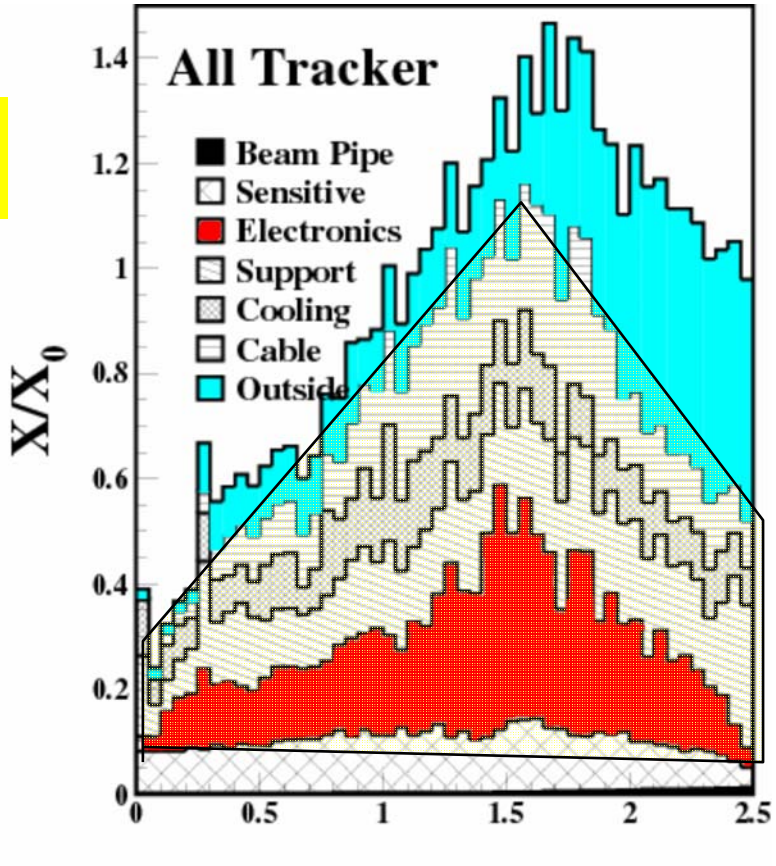
- Understand where we stand
  - Enabling tricks in ¼ micron CMOS
  - What has been done for LHC experiments
    - Illustration: One practical system implemented by using 5 new ASICs
- Where is industry going
  - Input from microelectronics developments in non-HEP areas
- Next generation: 130 nm and beyond
- What problems are coming next
  - Technical
  - Costs
- Summary

Why ?

What is the motivation for designing ASICs for experiments ?

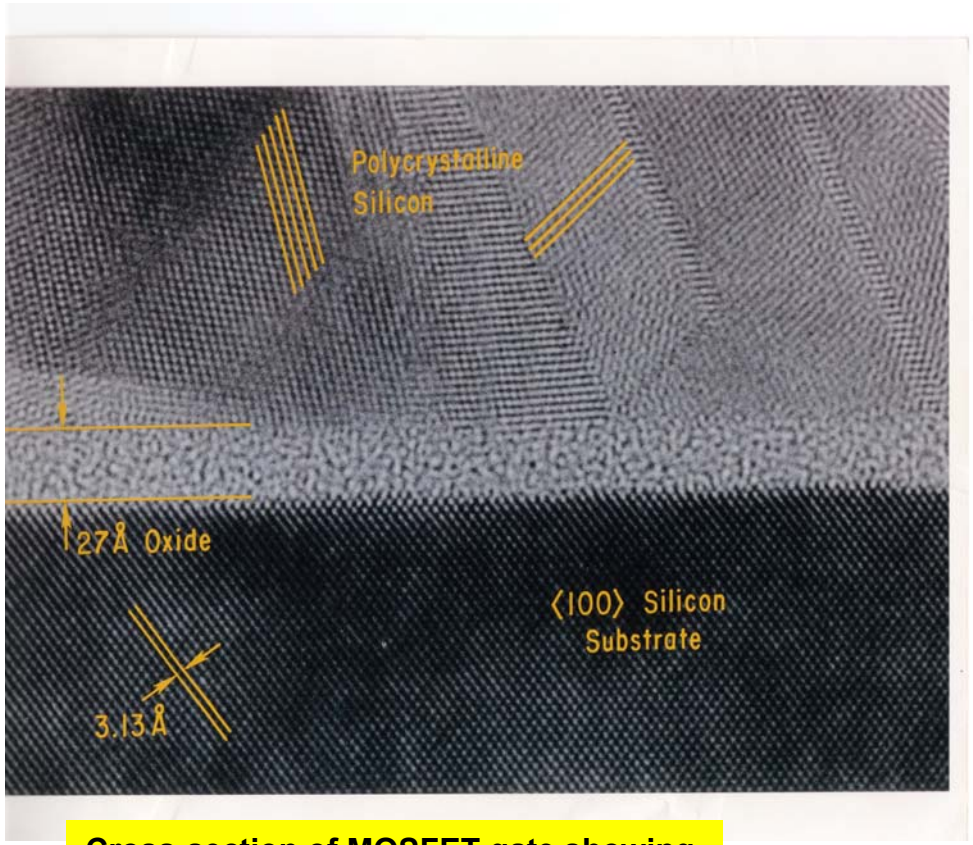
Why do we need better microelectronics ?

Material budget in CMS Silicon tracker

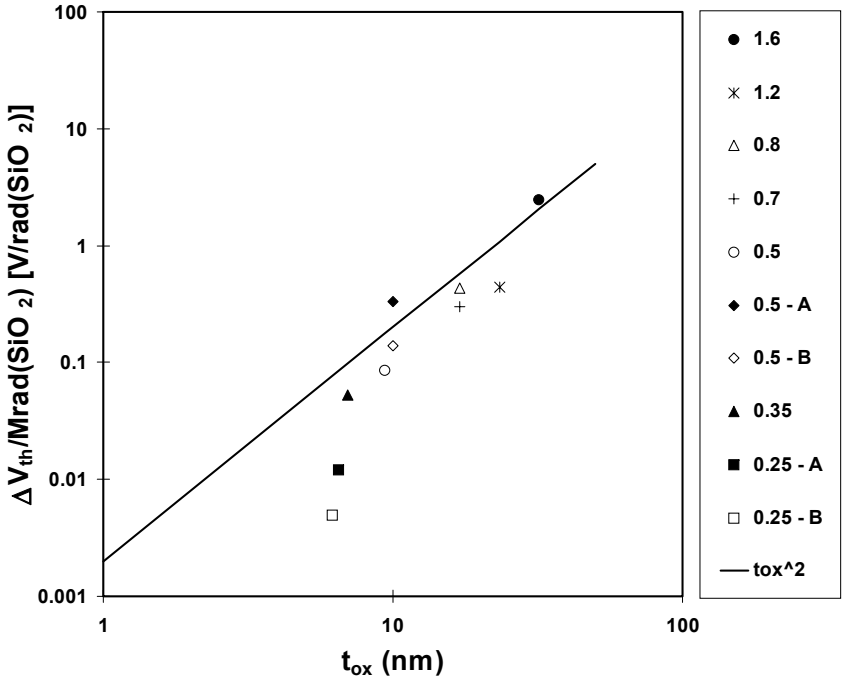


Enabling Technologies

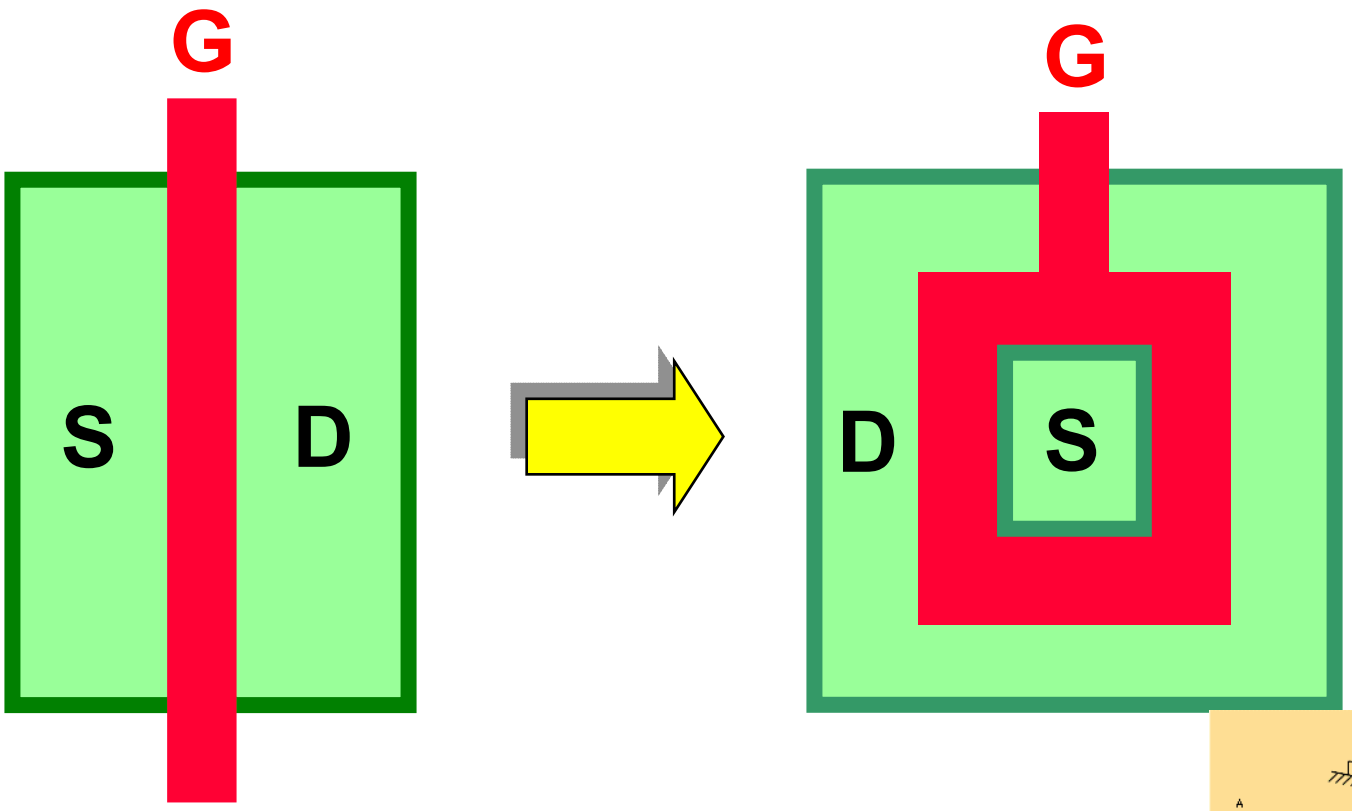
Progressing technology +

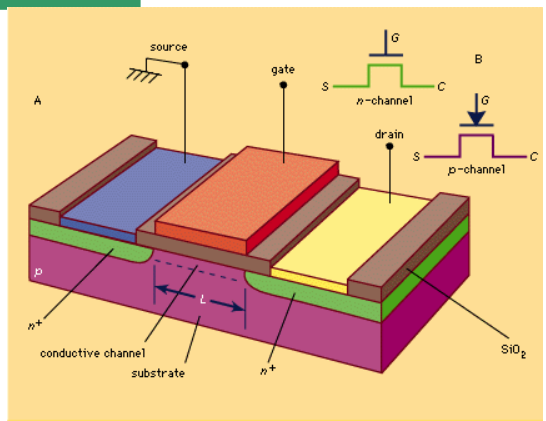


Cross-section of MOSFET gate showing thin isolation layer of SiO2

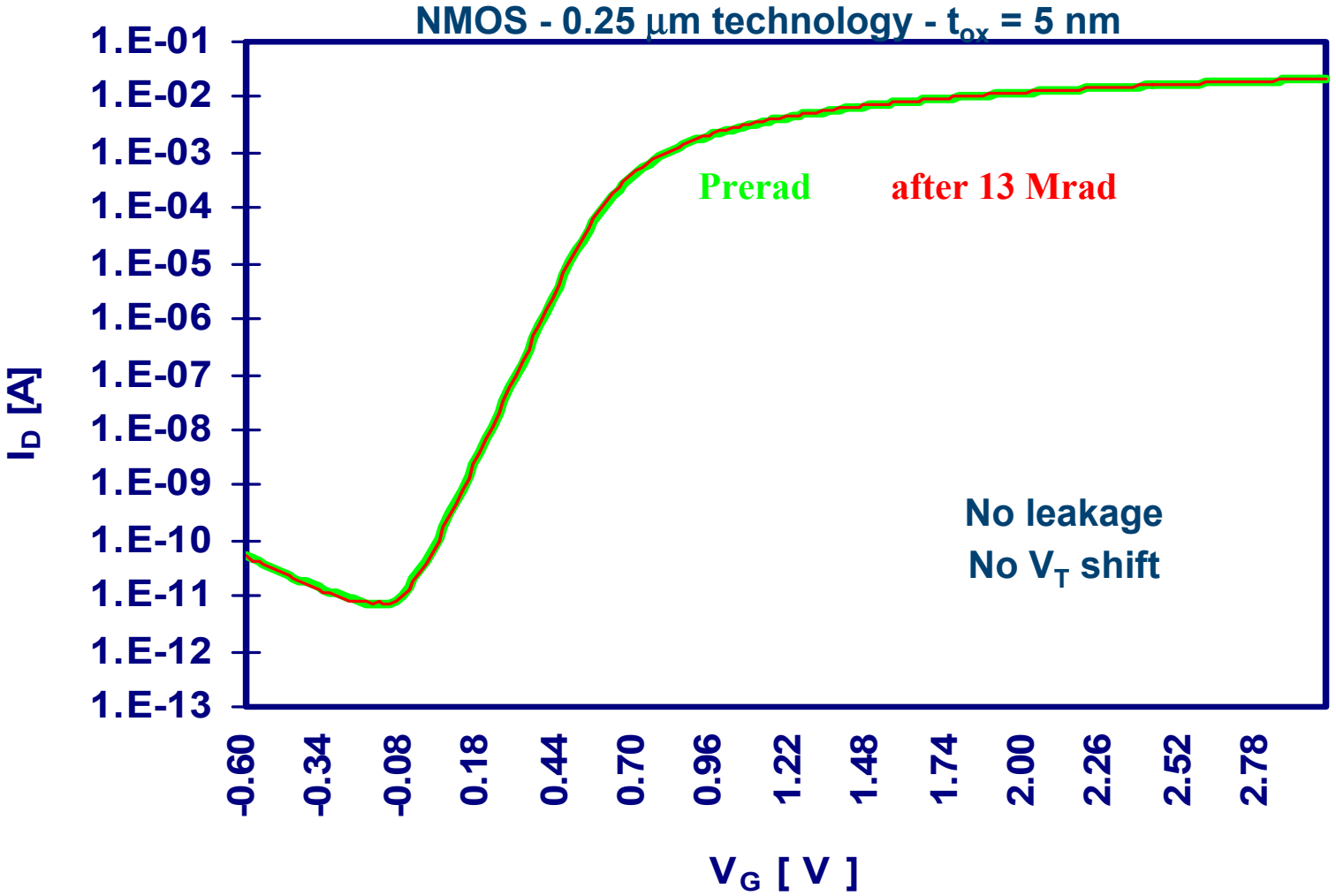


+ Design trick

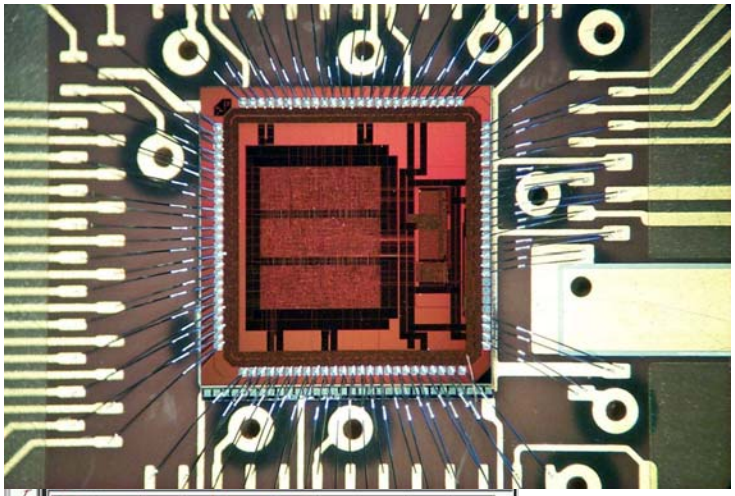


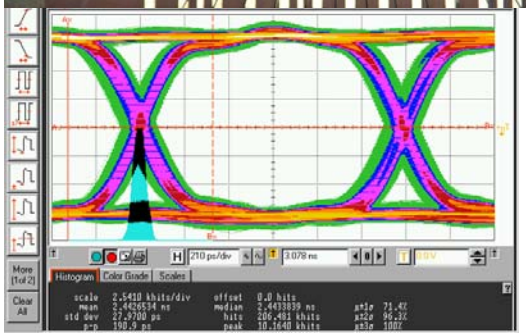


= Excellent result

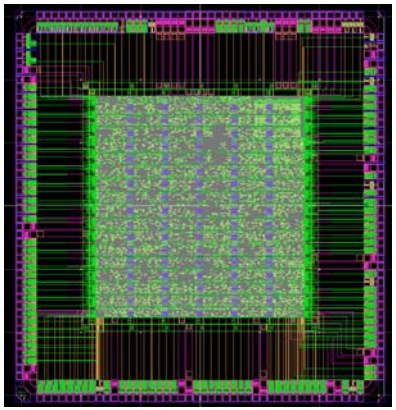


Design examples

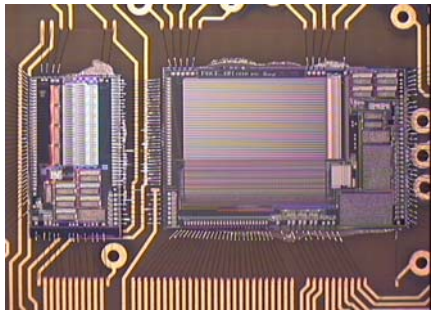




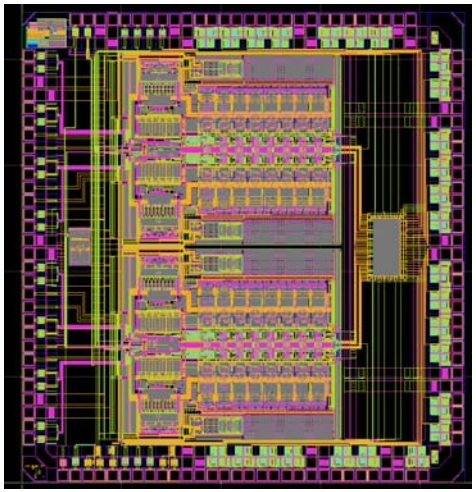
0.8-1.6 Gb/s serializer



Control chip for CMS Tracker and Ecal



FE for CMS preshower



Quad-12 bit 40 MS/s ADC

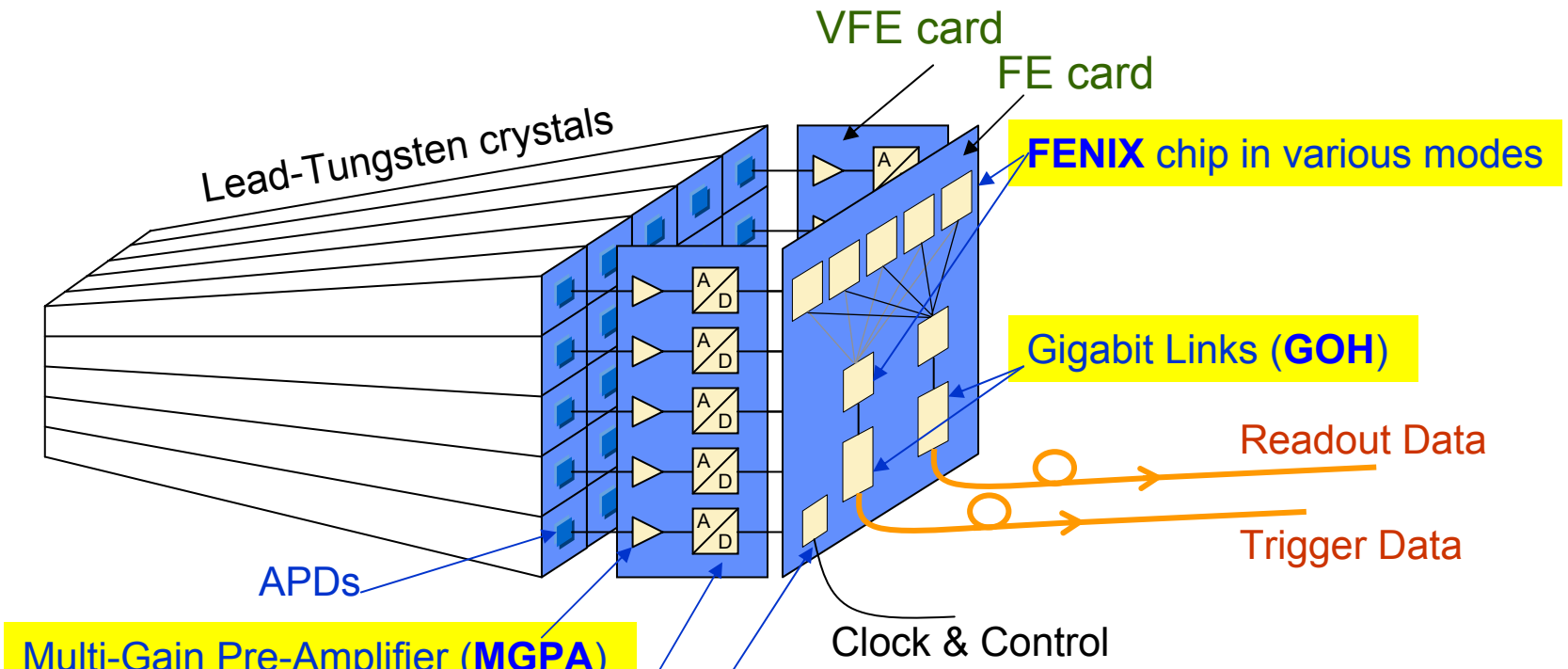
Summary of ASIC utilization in LHC

- **DMILL**
  - 0.8 μm BiCMOS "special" technology
  - some 1,000 6" wafers produced
  - < 5 major designs
- **CMOS6**
  - ¼ μm CMOS commercial technology
  - some 2,000 8" wafers produced
  - > 15 major designs
  - >> 100 prototype designs

Case Study: CMS Ecal (1/4)

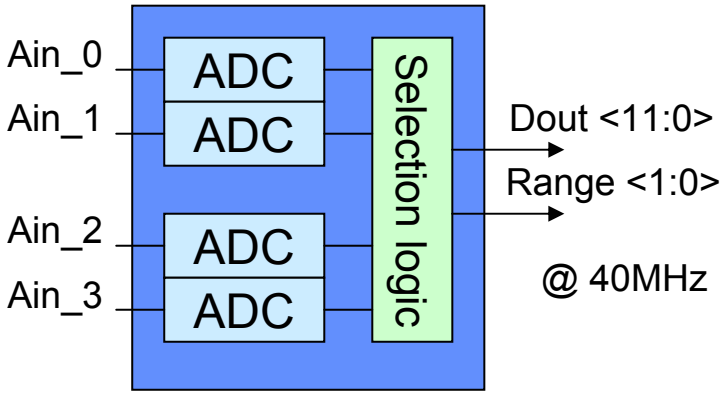
- 80,000 channels
- Requirements for Crystals readout:
  - 12 bit precision on a 16 bit dynamic range
  - Low power
  - 40 Ms/sec
- Optoelectronics dominates system cost if not used wisely
  - Avoid usage of fast links to send unreduced data
- Message: cost of ASICs << cost of opto

Case Study: CMS Ecal (2/4)



- **Key Features**
  - Single Power Supply 2.5V
  - All FE ASICS in CMOS 0.25 µm Rad-Tol process

Case Study: custom ADC (3/4)

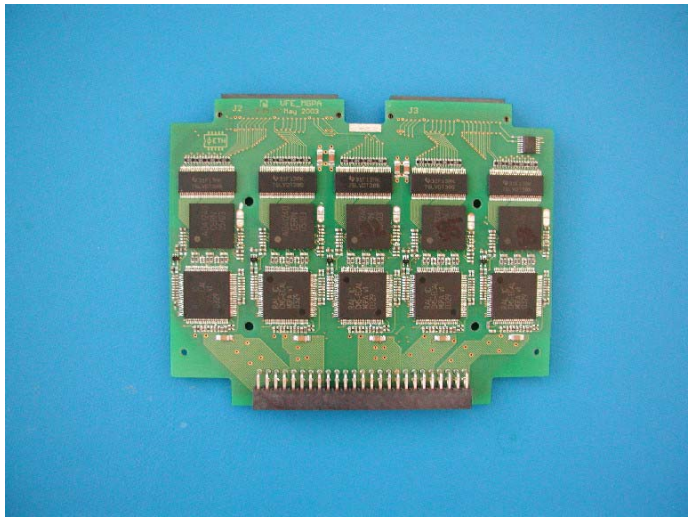


Mode	Bus speed [MW/sec]	#buses/ BusWidth
0 – Quad ADC	80 DDR	2/12
1 – Ecal Direct	40	1/14
2 – Ecal with Hysteresis	40	1/14
3 – Ecal Direct	80 DDR	1/7
4 – Ecal with Hysteresis	80 DDR	1/7
5 – Transparent (0-1 ch)	40	2/12
6 – Transparent (2-3 ch)	40	2/12

"Single ADC" mode for ECAL Crystals

- **Key features**
  - Quad channel Pipelined ADC
  - Conversion latency: 6 clock cycles
  - Resolution: 12bit
  - High Speed: 40MSPS
  - Low power: 412 mW @ 2.5V, 40MHz
  - CMOS 0.25 µm Rad Tol commercial process
  - Output bus: Multiple modes of operation
- **Developed by**
  - ChipIdea Microelectronica & CERN

Case Study: CMS Ecal (4/4)



- VFE Card
  - 5 MGPA
  - 5 AD41240
  - 1 DCU (Detector Control Unit)
- FE Card
  - Serves 5 VFE (25 Channels)
  - 5 Strip Sum FENIX
  - 1 Data FENIX
  - 1 TPG FENIX
  - Control chips (CCU/DCU/LVDSMUX/QPLL/PLL)

Using ASICs is great, but … where is industry going ?

Different growth models

- **Industry**
  - 2x every 18 months since 30 years
    - Essentially an "evolutionary growth model"
  - Well predicted, modulated by market demand
  - Microelectronics is the Primary Tool, enabling new applications to be defined:
    - Gigantic engineering effort are behind many high volume popular products (PCs, mobile phones, Wi-Fi Internet, MP3-HiFi consumer etc.)
- **HEP**
  - Quantum step every ~ 20 years
  - > 10 years construction
    - many unknowns
    - ROI difficult to predict
  - Technology is not always perceived as important (detectors and physics are first objectives, microelectronics is just "another tool")

The luckiest paper ever written

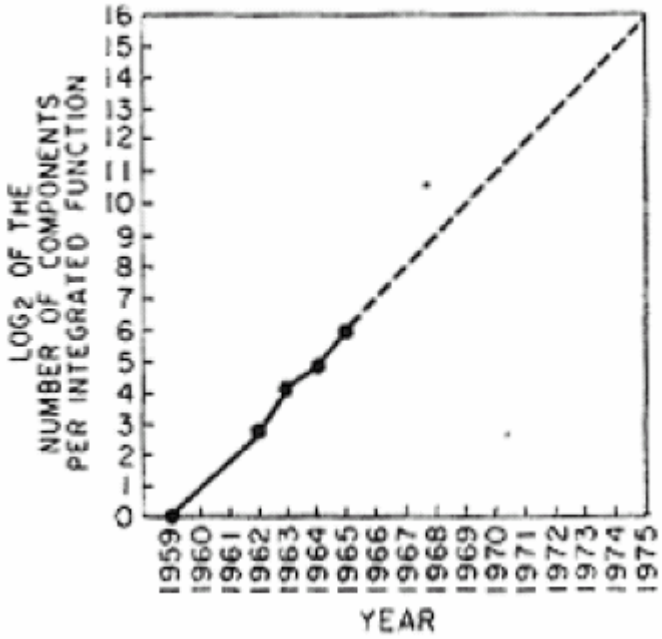
Cramming more components onto integrated circuits

With unit cost falling as the number of components per circuit rises, by 1975 economics may dictate squeezing as many as 65,000 components on a single silicon chip

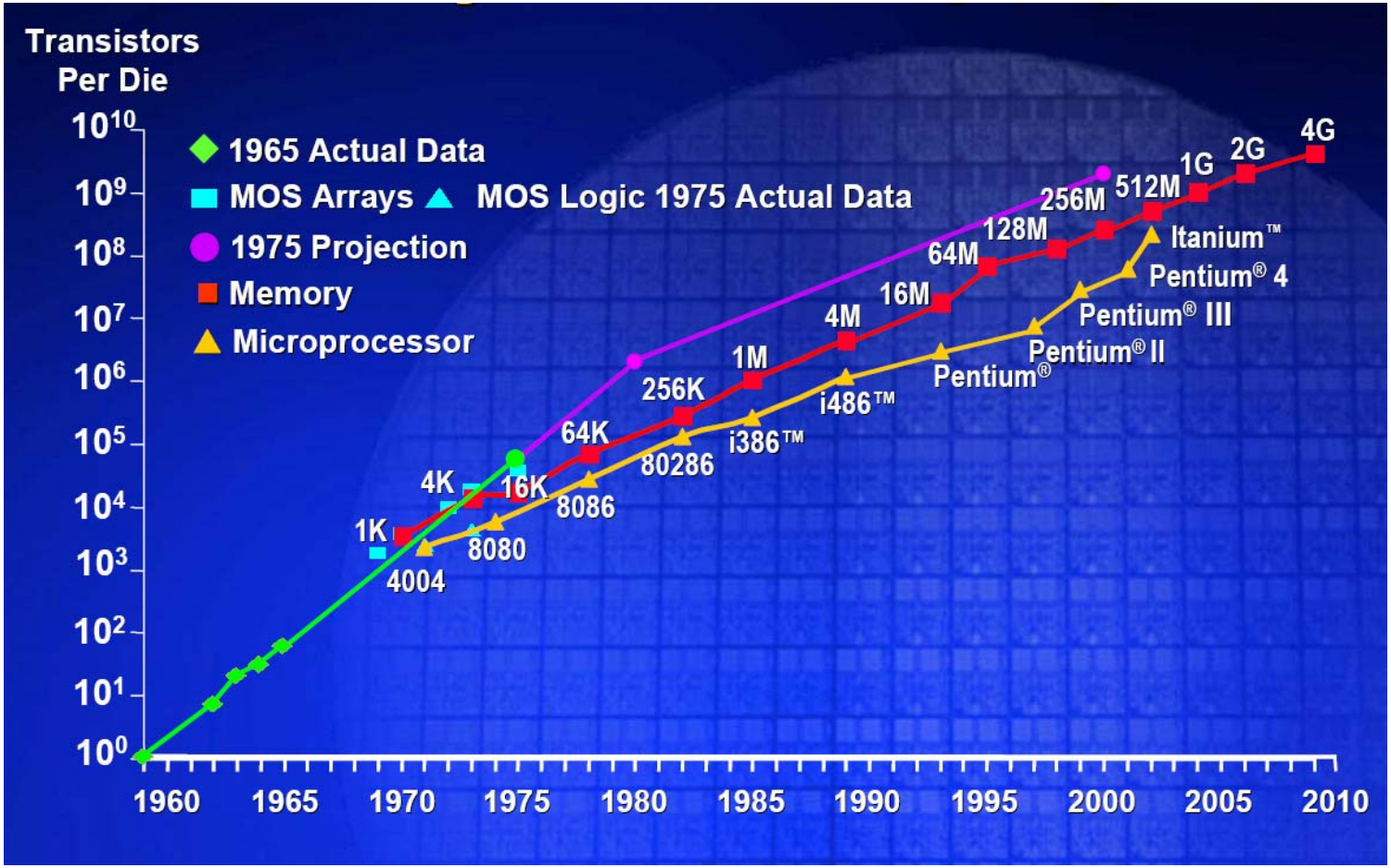
By Gordon E. Moore

Director, Research and Development Laboratories, Fairchild Semiconductor division of Fairchild Camera and Instrument Corp.

Electronics, Volume 38, Number 8, April 19, 1965



Scaling continues



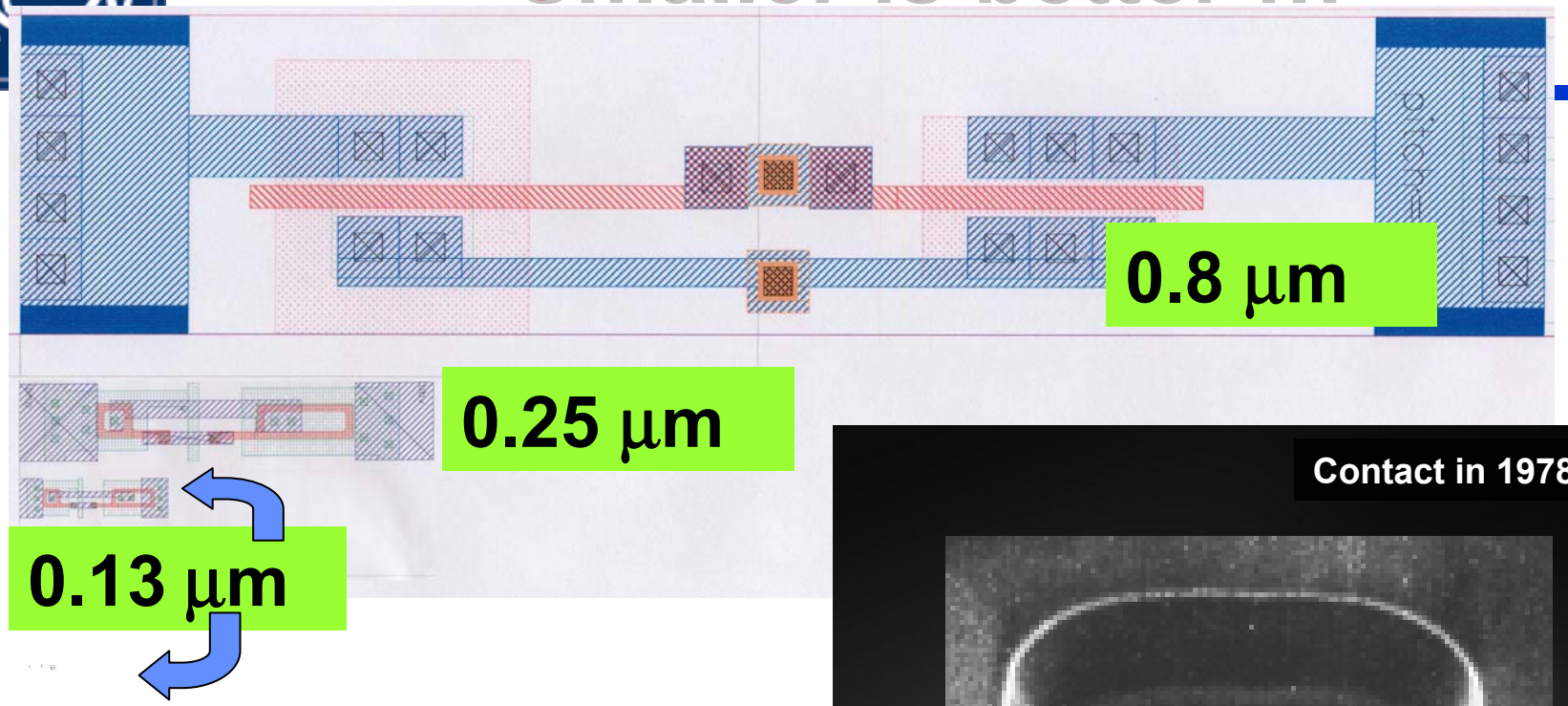
Source: Intel

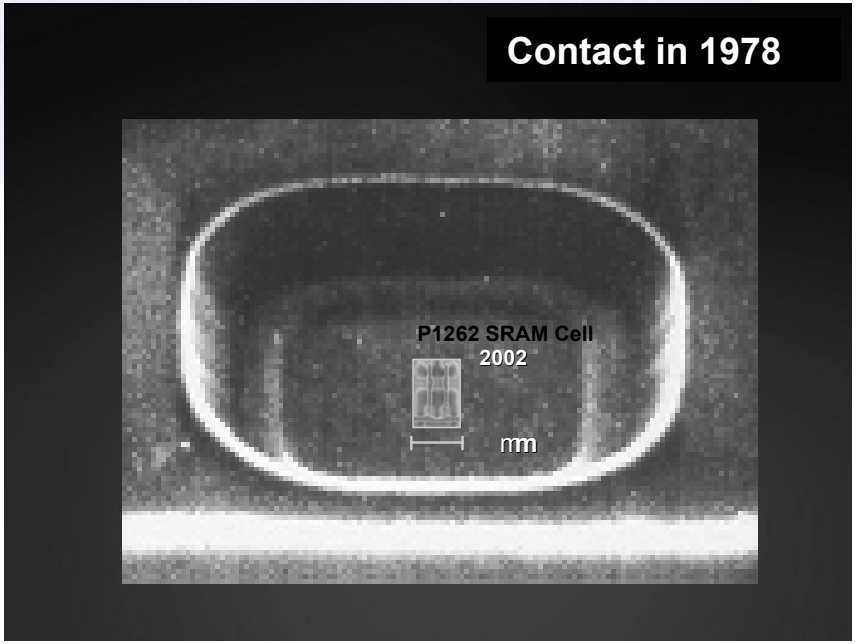
Who is using what

	0.25 µm	0.18 µm	0.13 µm	0.09 µm
Micros [Session 3,18]	1	4	6	3
Memories [Session 11,27]	0	1	7	6
SerDes [Session 9,13,22,26]	2	7	10	6
A/D [Session 14,25]	2	8	4	1
RF [Session 15,21]	4	2	3	0

Number of papers at ISSCC2004 in selected areas

Smaller is better …





Power consumption:
0.25 um: Inverter @ 100 MHz: 5.5 uW
0.13 um: Inverter @ 100 MHz: 0.58 uW

What's in it for us

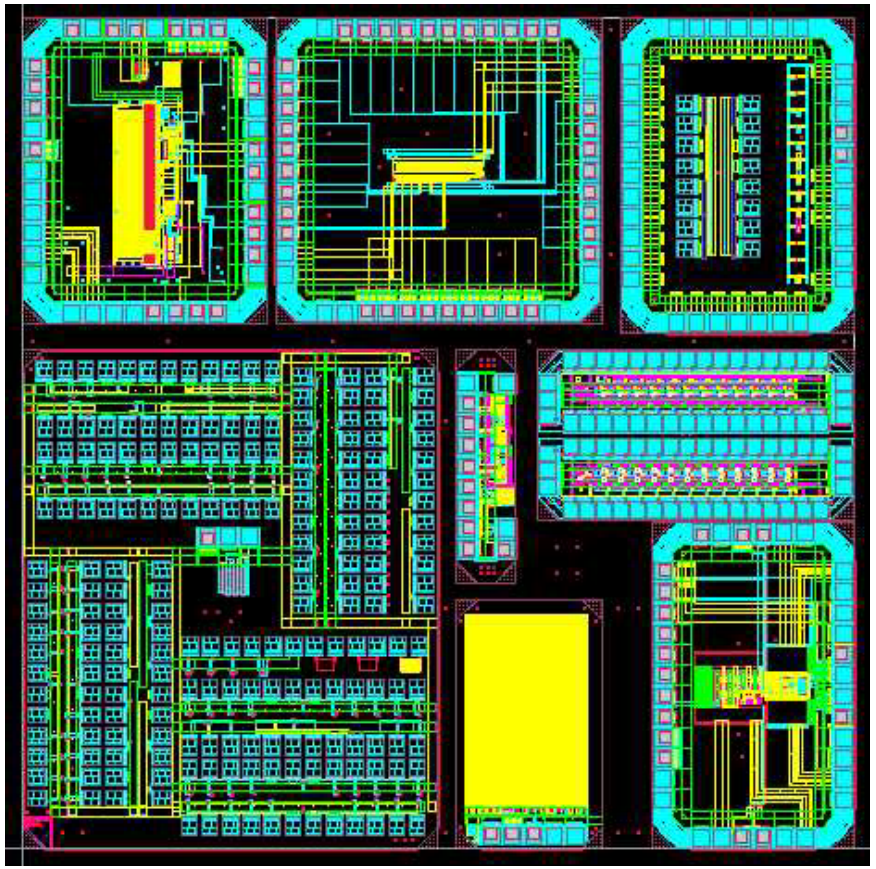
- **Much higher integration capabilities**
  - Better instrumentation and better data
  - More reliable equipment
  - Microelectronics can reduce dramatically system cost
    - Only if integrated early and fully in system design
  - Future higher integration can open the way to solutions just un-thinkable today
    - Think of how transistor on non-silicon substrates has revolutionized the market of displays
    - Think of how flash memory technology is changing the market of consumer portable HiFi devices
    - Think of how microelectronics technology combined with huge advances in coding theory has revolutionized the telecom world
      - Several MB/s and more on a 3 KHz BW phone line
      - 10 MB/s and more on radio links at very low cost

Can we follow ?

Early irradiation results with 130 nm

2003 Test run

- **Run options:**
  - 6 levels of metal (4 thin; 2 thick)
  - Mimcap
  - Op resistors
  - All transistors:
    - all Vts
    - all oxide thicknesses
  - Designs with linear or Enclosed transistors



Contact author or F. Faccio /PH for detailed results

130 nm Preliminary Results

- **TID**
  - Enclosed transistors are very good
  - Linear transistors also look very promising with minor weaknesses
  - No guard-ring needed
  - Thick Ox gates (IO devices) are sensitive: use carefully!

- **SEEs**
  - Sensitive charge smaller, higher SEU sensitivity
  - NB: without enclosed transistors, error rates can be considerably higher than for present 0.25μm designs
  - SEL not observed and not expected to be a crucial issue for our applications (careful: design-dependent sensitivity)

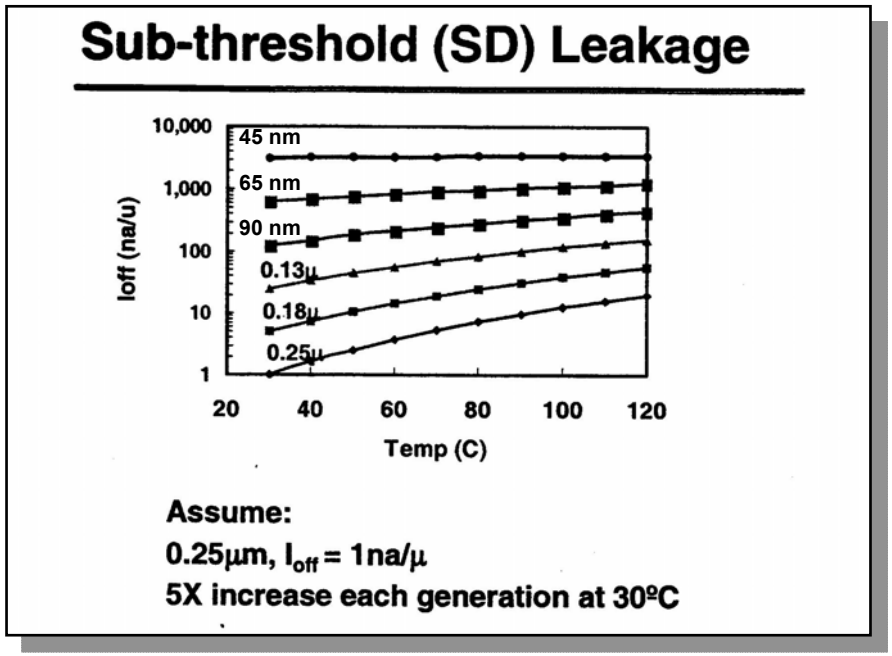
If we embark beyond 130 nm, what are the difficulties ?

The bad news!

- **Technical**
  - Some CMOS advantages are disappearing
  - Complex modeling
  - Analog becoming more and more painful
  - Digital and wiring complexities
  - 12" vs. 8" wafers (instrumentation cost)
- **Cost**
  - Much Higher NRE
  - Business for HEP is exponentially $_{\text{decreasing}}$ for modern fabs

Problems with DSM

- New high K dielectric are needed to cope with gate leakage problem
  - leakage current increases very fast
- New simulation models
  - "Good-bye to old MOS devices, gate current must be included"

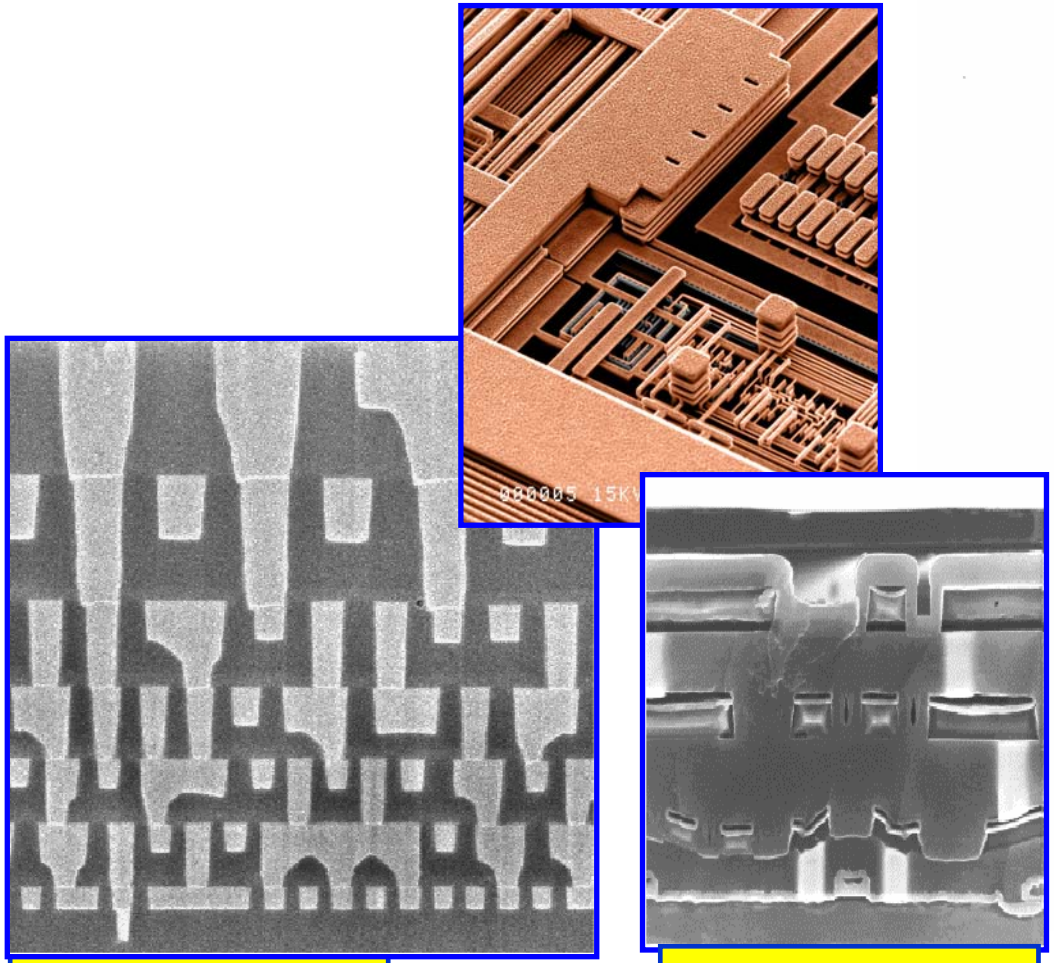


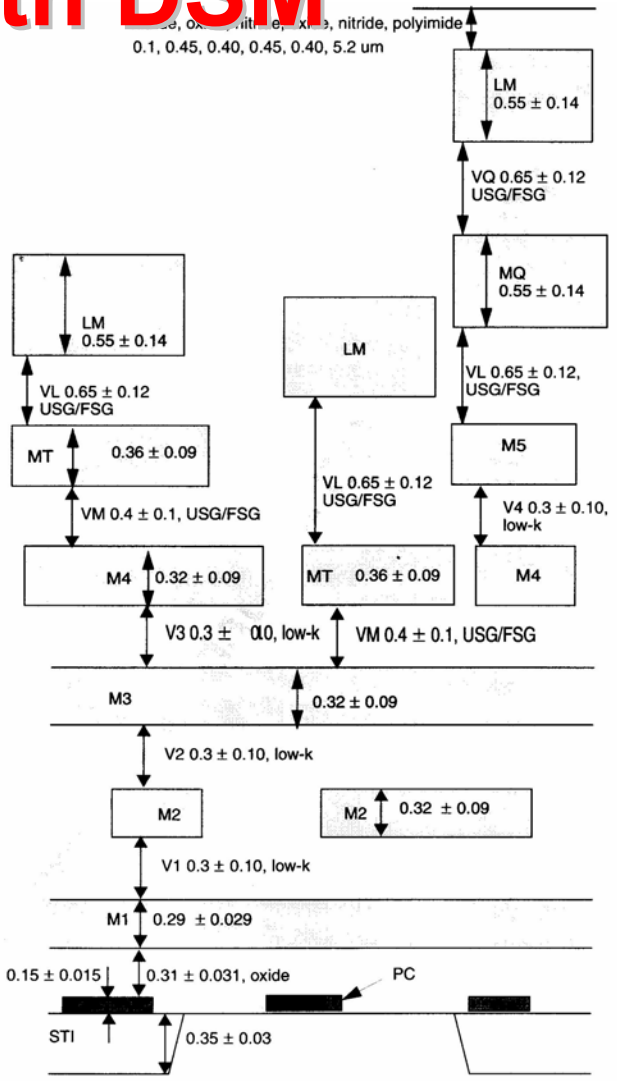
Problems with DSM

	Tech	Speed	Area / # devices	Power	Comments
Power5 IBM	.13 μm SOI	1.5 GHz	389 mm^2 276 M	160 W	10% of power in leakage
Sparc Sun	.13 um	1.2 GHz	206 mm^2	23 W	
X86 Intel	90 nm	4 GHz	112 mm^2		
Power 970 IBM	90 nm SOI	2.0 GHz	62 mm^2 58 M	50 W	

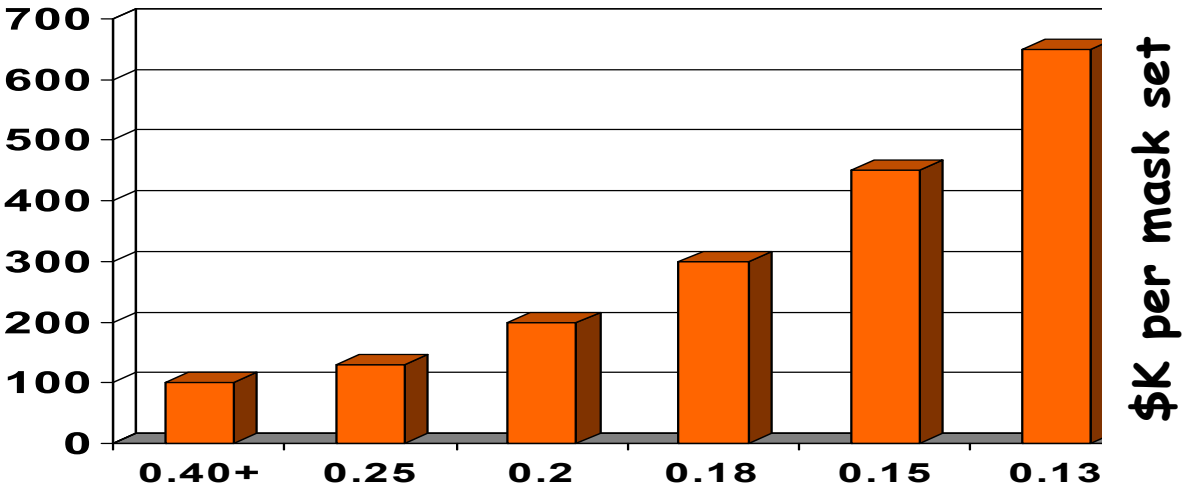
Microprocessors presented at ISSCC2004

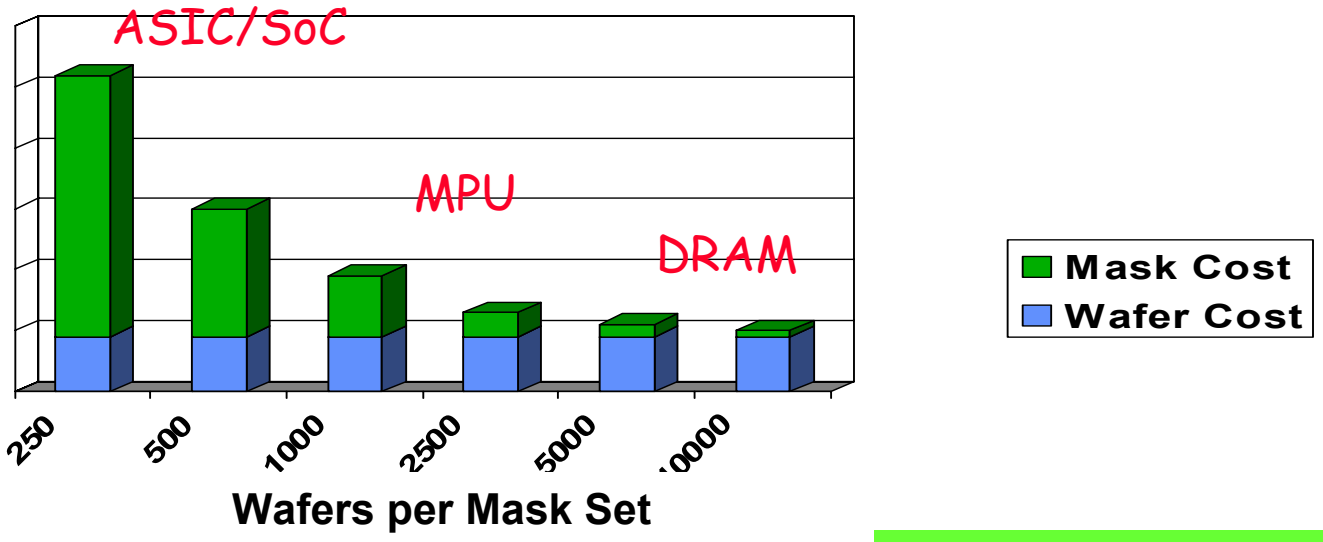
Problems with DSM





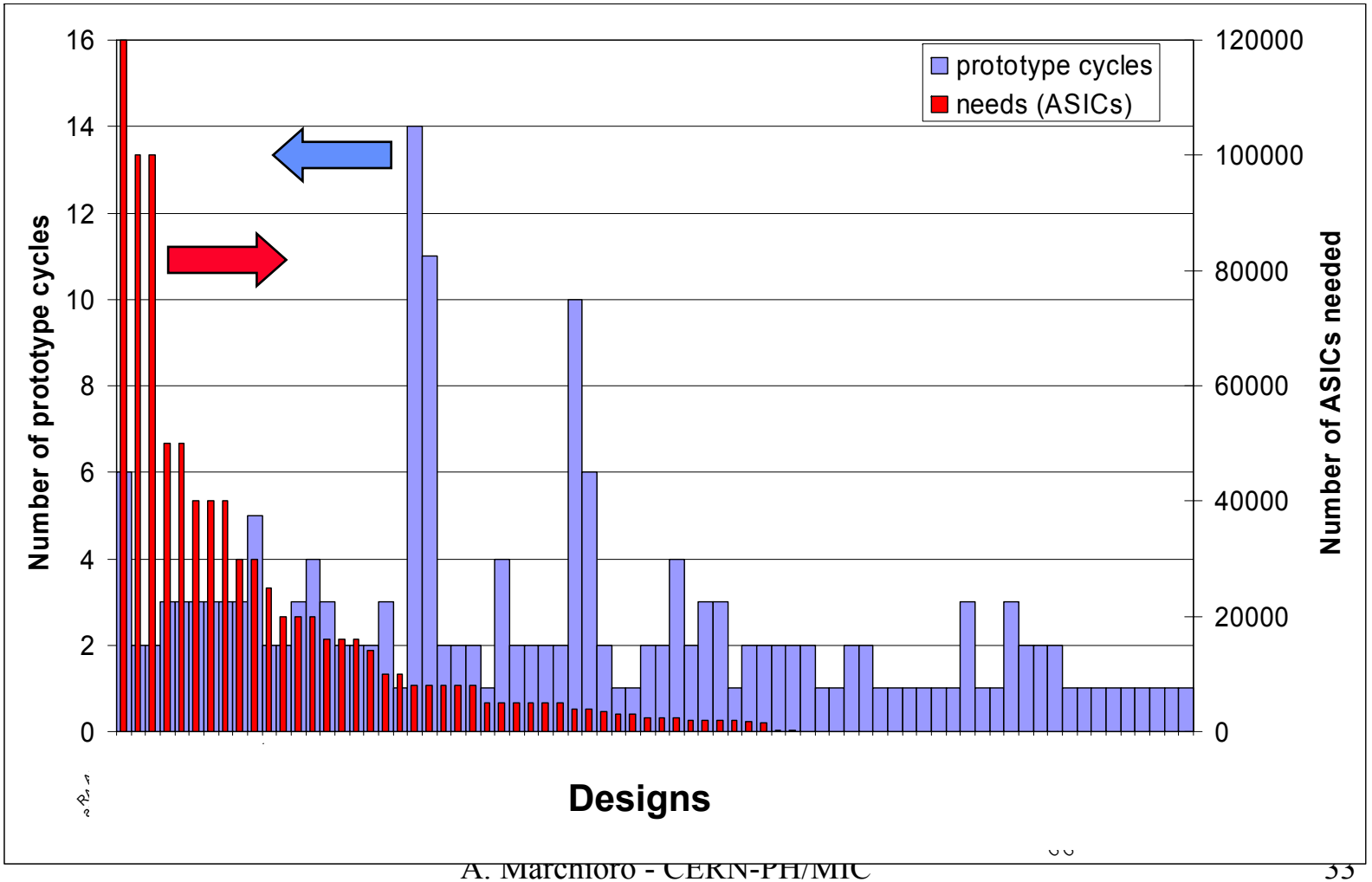
Cost comparison



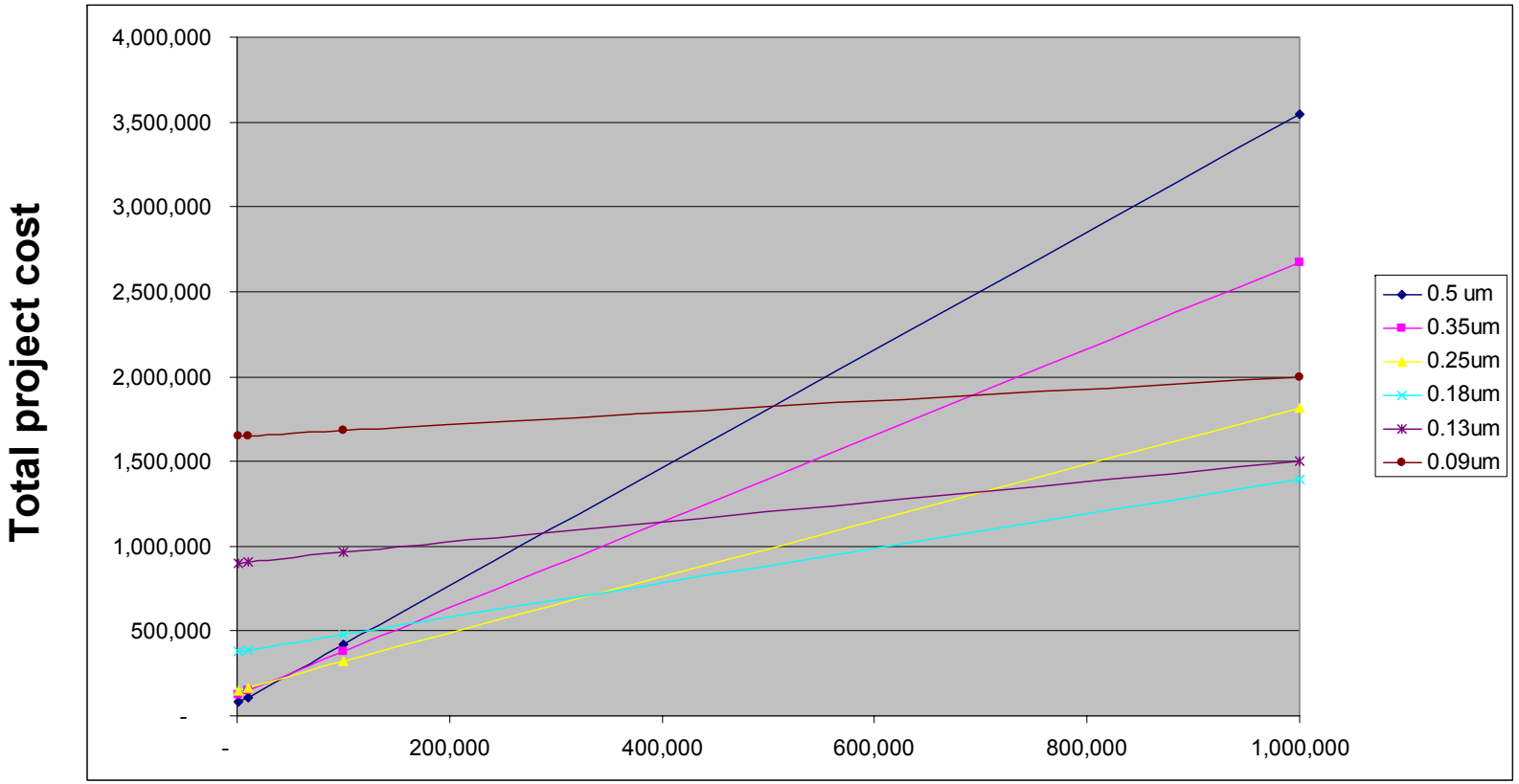


Kind permission from: M. Rieger, Avant Corp.

Production vs. design



Cost model (take with a grain of salt)



…and don't forget

- Design cost is roughly same as wafer cost for up to 100K parts in 0.25 μm
- Investment for becoming "proficient" is very high and should be accounted fairly
  - ASIC designer should NOT be recycled to other electronics jobs
- Packaging can be as expensive as silicon
- Testing takes always 5x more than foreseen
- Users tend to neglect issue of spare parts

Key areas

- Given the increasing costs of ASICs fabrication, we may have to limit the future developments to only those parts with really high volume
  - Trackers
  - Calorimeters
  - Timing systems
  - Any high volume component in machine ?
- Too many low volume designs performed in our community
- Investment in "generic" ASICs (remember the 74xx or LMxx series?) should be gratified and rewarded by the community !

Conclusions

- Microelectronics is for HEP of the future what photographic emulsions and bubble chambers have been in the past
- Technology will unquestionably be ready and available to offer another quantum step in instrumentation for physics
  - Huge opportunities are open to creative people
- Success will depend on our capability to:
  - Master technology
  - Manage risks and costs
  - Manage our own organization