TAB bonding

Tape Automatic Bonding (TAB) offers an elegant solution not only for a flexible and compact interconnection between the readout ASICs and the sensors but also for ASIC selection and testing prior to the assembly of the detector and their associated readout electronics. Our group has explored that road in close collaboration with the Kharkhov Space Institute in Ukraine. The microcables investigated use 12 μm thick aluminum traces on a 12 μm thick polyamide flex. The minimum trace separation, 100 μm, were just enough for the 140 μm pitch of the ASIC pads. Nevertheless, first positive results have already been obtained with a trace separation of 50 μm.

A silicon module prototype has been built using this technology and tabbed. The module was made with a 500 μm thick silicon pad detector with 8x32, 1.4x1.4 mm pads which were readout by two VATAGP ASICs. The TAB of the module consists of three different tape desings: one for the silicon sensor, one for the readout chip, Figure 1, and another one for the hybrid circuit. Each tape is tabbed to the respective component (dectector, chip or hybrid) and then assembled together as shown in Figure 2.

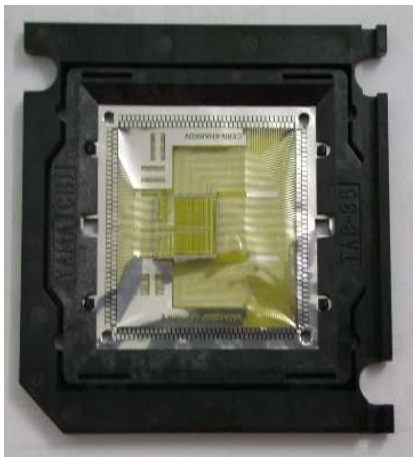

Figure 1. Tabbed chip in the testing frame.

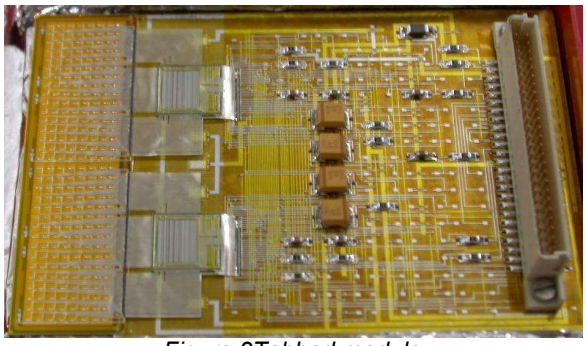

Figure 2Tabbed module

Before assemblying the 3 parts, a chip quality selection was made testing several tabbed chips in a dedicated test system. The system consisted of a clamp board, see Figure 3, holding the ASIC frame shown in Figure 1. The clamp was housed in an intermediate board in charge of the distribution of acquisition signals and data (Figure 4). The setup allowed to test most of the ASIC features comprising both the analogue and the digital circutries.

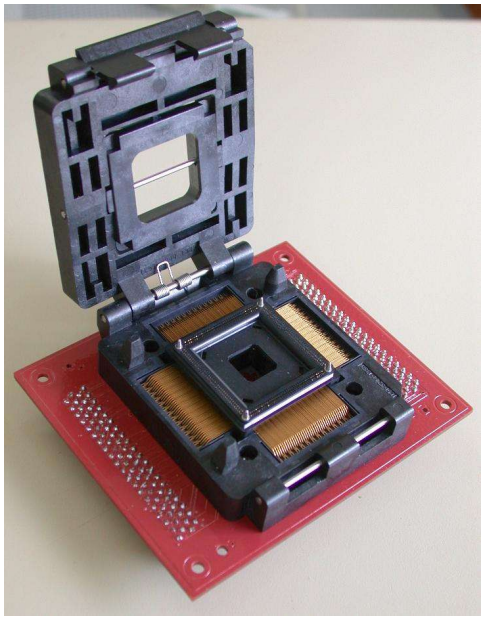

Figure 3. Device to hold the frame with the tabbed chip

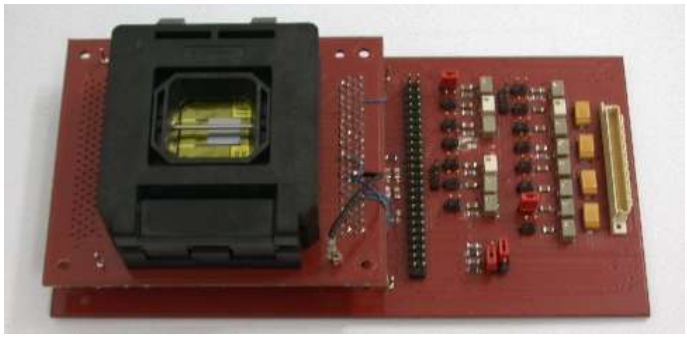

Figure 4. The chip frame and the clamp board are connected to a board that will distribute the DAQ signals.

Once the ASICs where selected the module was assembled and tested using an ^{241}Am source. Although some of the trigger lines could not be addressed and the data was taken with the wrong timing, however the readout of the

tabbed module worked successfully. First estimates obtained after unfolding the data for the timing problem show a slight increase of the noise due to, presumably, a non-optimized trace length and capacitance.

Future work will, therefore, be focused on an optimized design of the microcables trying to minimize the stray capacitances. Also intended for next developments is to reduce the minimum trace separation down to 50 μm in order to cope with the smaller pitch of the new versions of the ASICs.