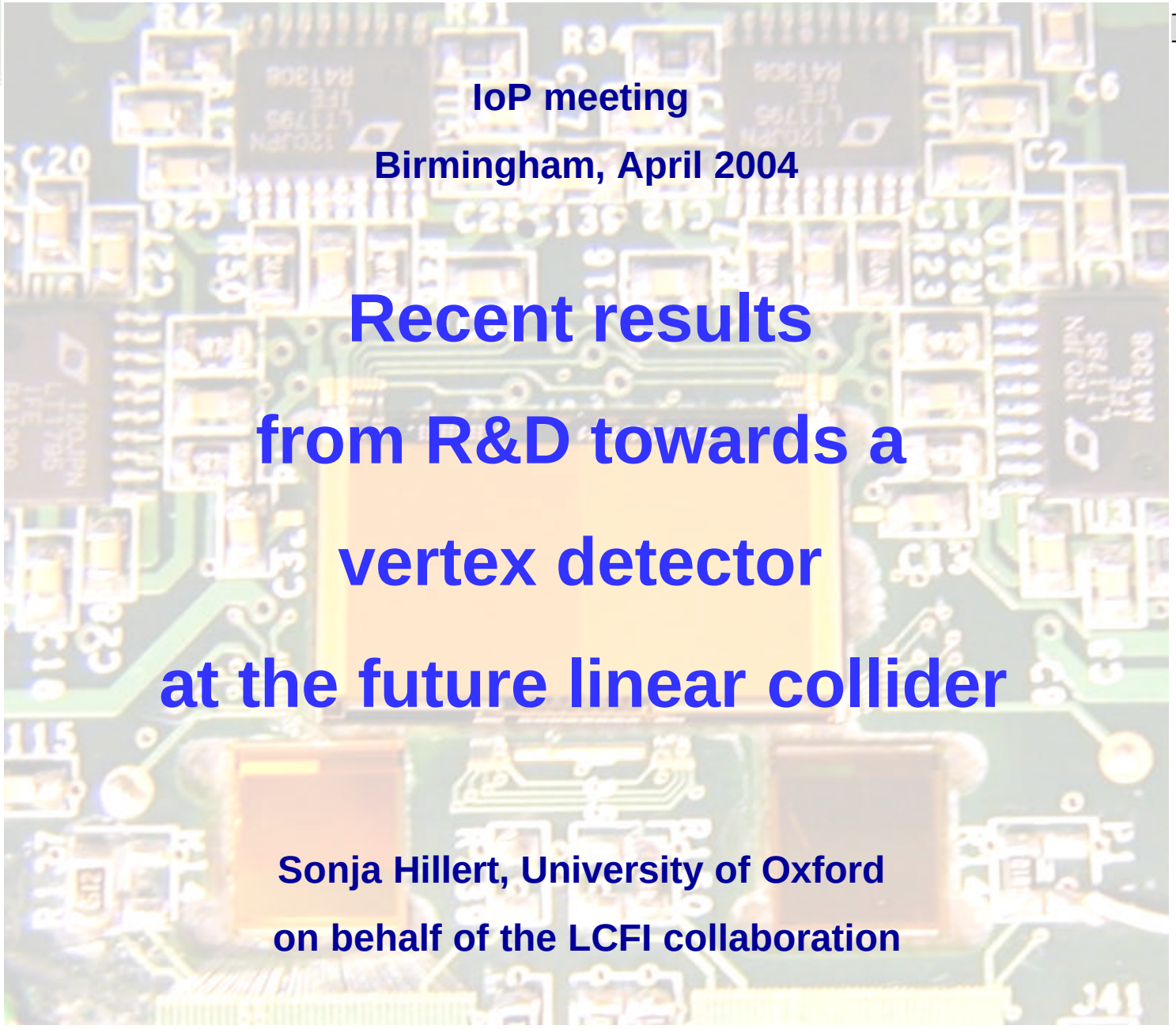


IoP meeting

Birmingham, April 2004

Recent results from R&D towards a vertex detector at the future linear collider

Sonja Hillert, University of Oxford

on behalf of the LCFI collaboration

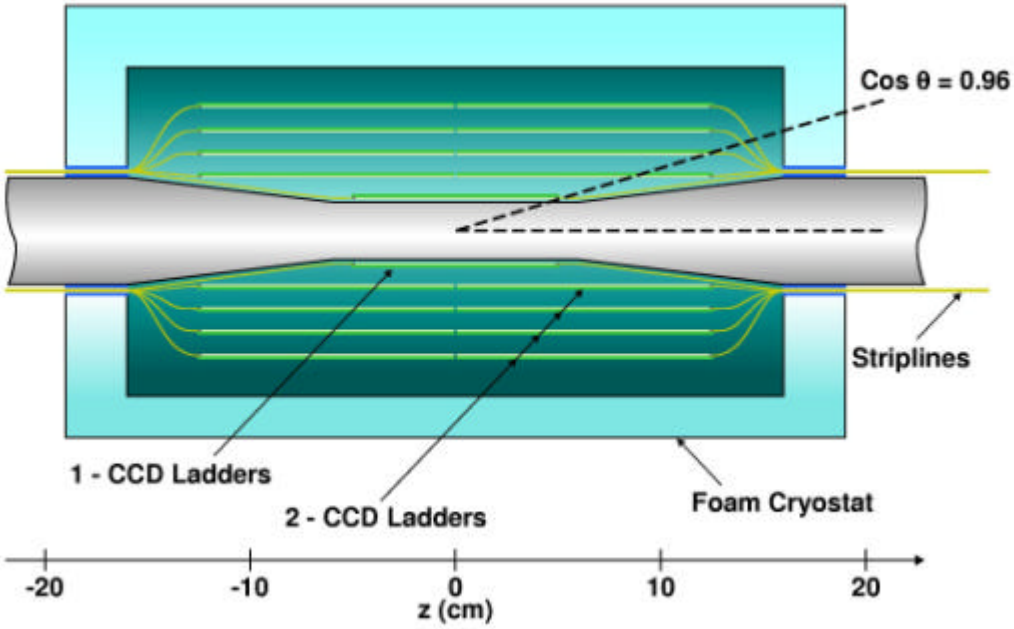
A vertex detector for the future LC

Precision measurements require:

- Good angular coverage (cos q = 0.96)
- Proximity to IP, large lever arm:

  5 layers, radii from 15 mm to 60 mm
- Minimal layer thickness (< 0.1% X_0)

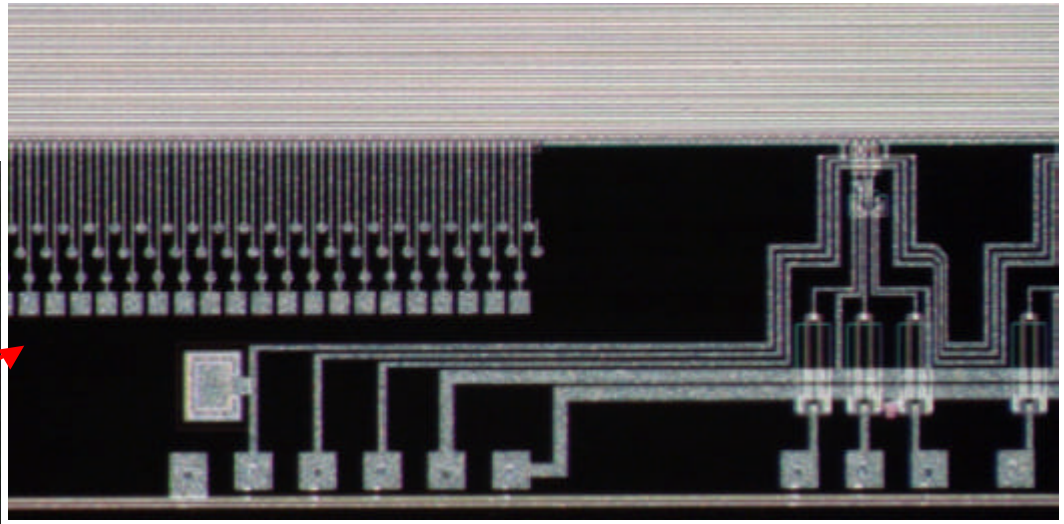
  to minimise multiple scattering
- Mechanically stable, low mass support
- Low power consumption



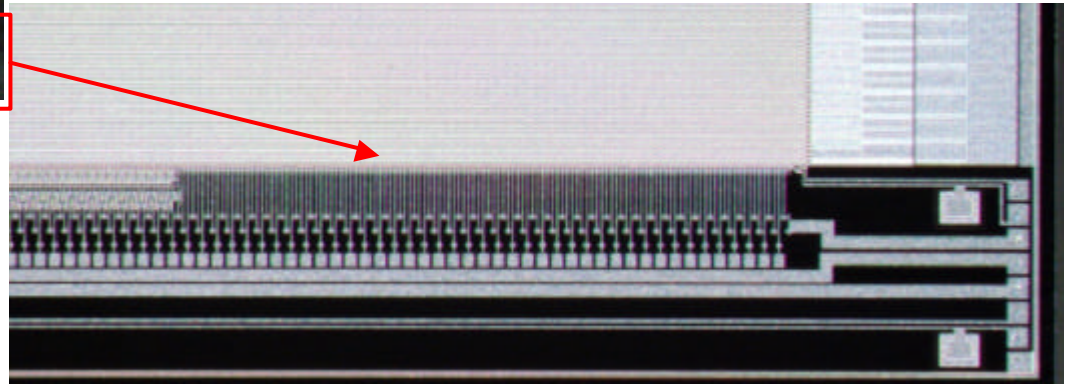
High hit density near interaction point requires:

- Small pixel size: 20 mm ´ 20 mm
- Fast readout: to be achieved with Column-Parallel CCDs
  - 8ms for NLC/GLC (read between bunch trains)
  - 50 ms for TESLA (read 20 times during trains)

Our first Column-parallel CCD



Direct connections and 2-stage source followers



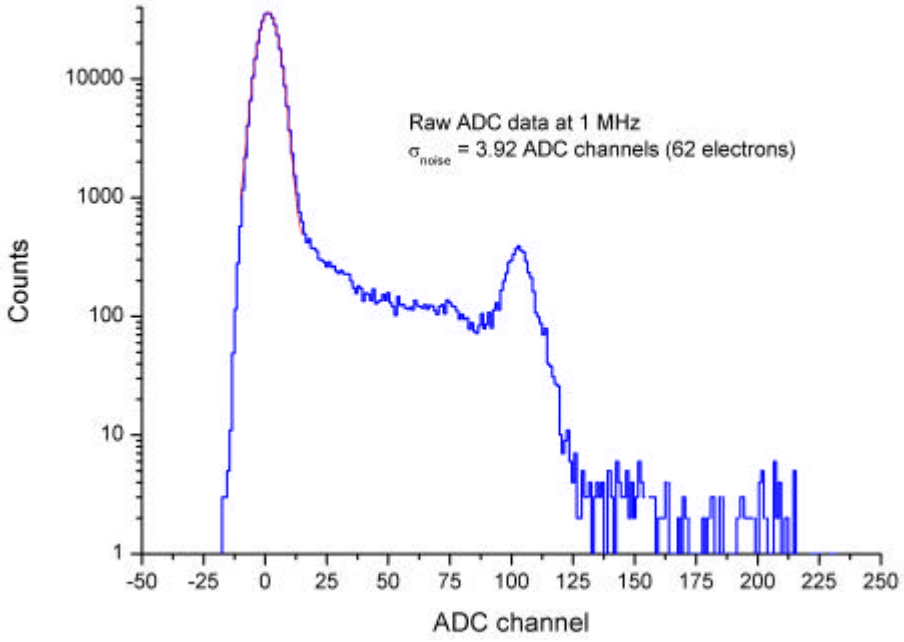
1-stage source followers and direct connections on 20 µm pitch

- Two phase, pixel size 20 µm ´ 20 µm;
- 400 (V) ´ 750 (H) pixels;
- Two charge transport regions;
- Wire and bump bond connection pads to readout chip and external electronics.

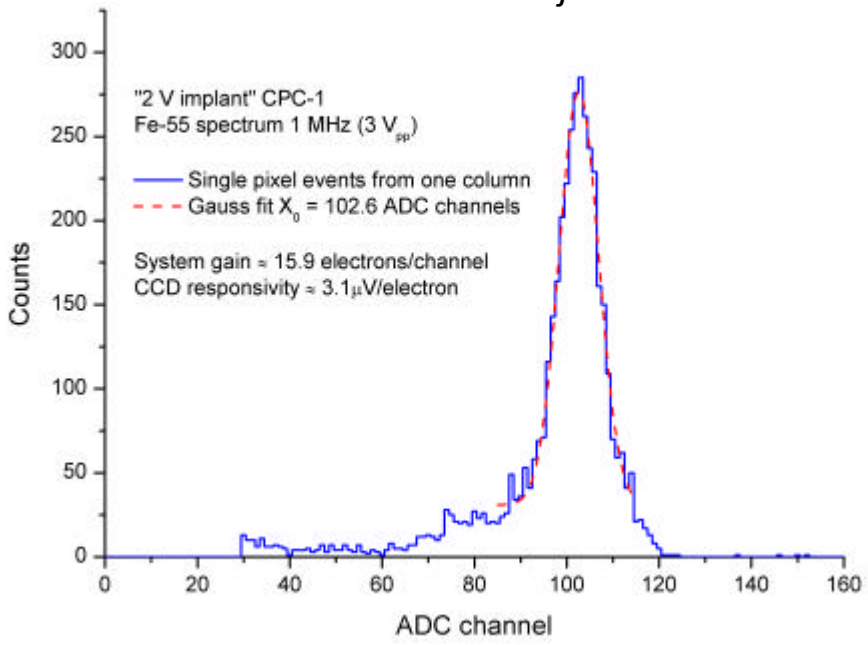
Stand-alone CCD tests

tested CCD with 5.9 keV X-rays from ^{55}Fe source, external VME-ADC at 1 MHz:

- **CCD sensitivity » 3.1 µV/electron;**
- **Gain spread between channels £ 6% - allows easy data analysis;**
- **Noise » 60 electrons with 3 MHz low-pass filter.**

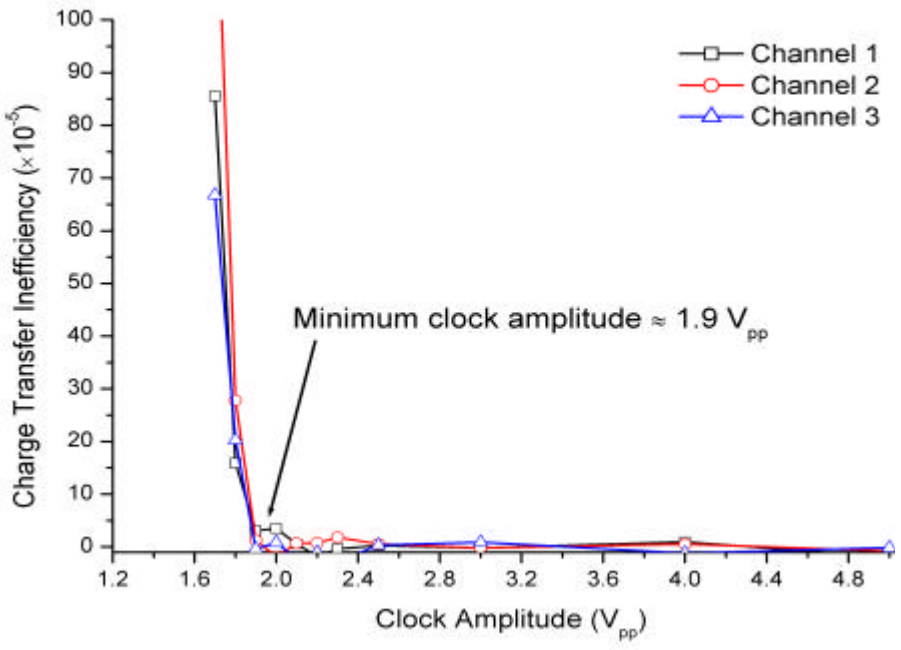


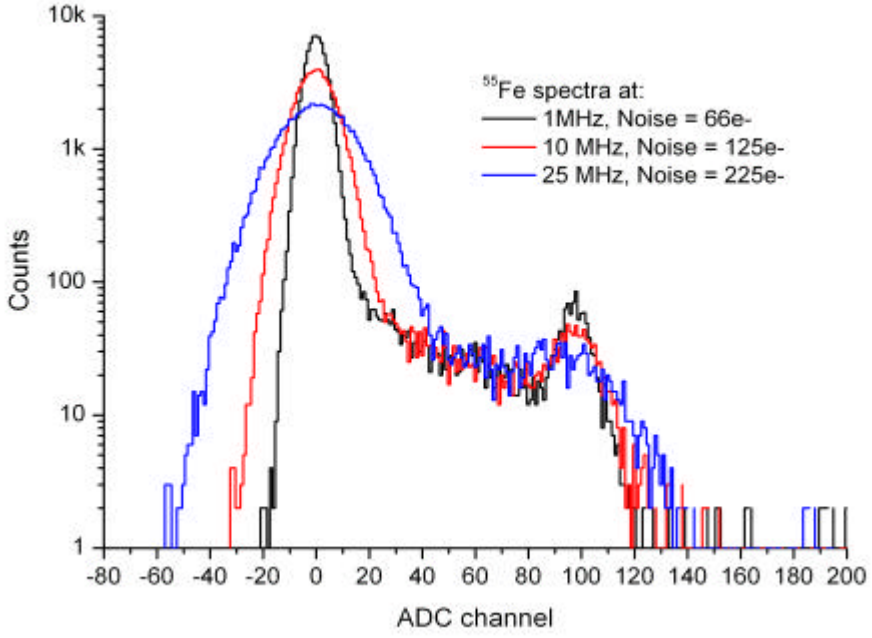
Single pixel hits spectrum using information from 3 adjacent columns



Characterising the Performance

Clock amplitudes down to 2 V_{pp} and clock frequencies up to 25 MHz reached

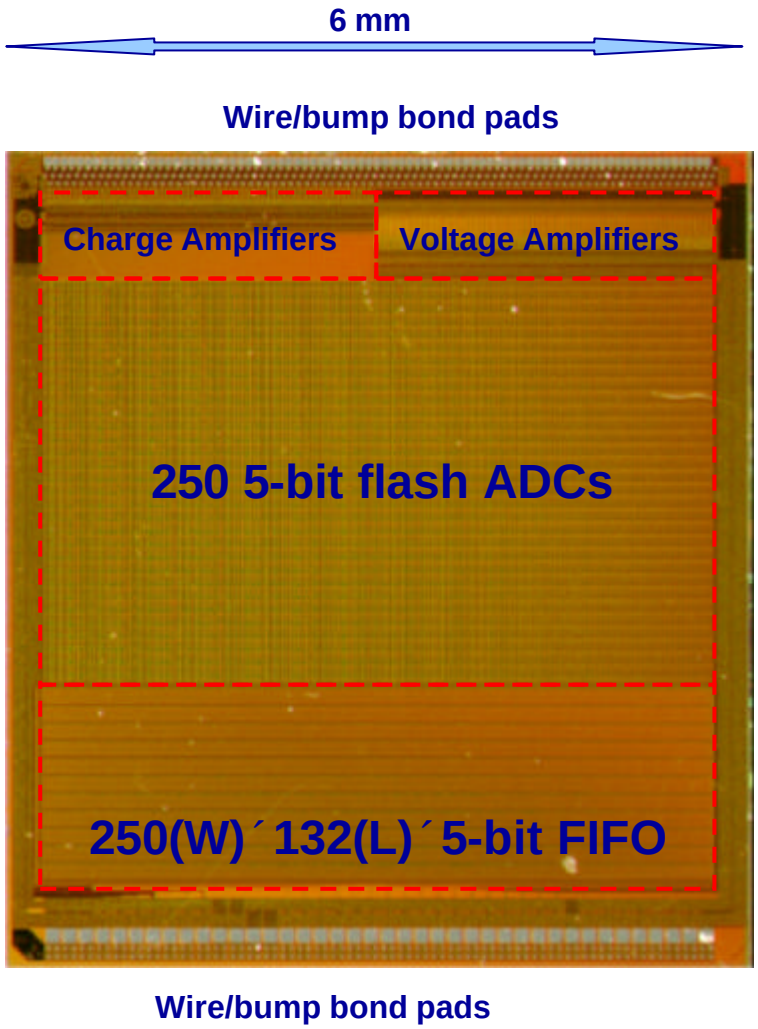




➢**Minimum clock amplitude 1.9 V_{pp} for optimised inter-gate barrier and field–enhancement (i.e. smaller charge storage region)**

➢**At high frequency: increased clock feedthrough and noise, under further investigation**

Readout Chip CPR1

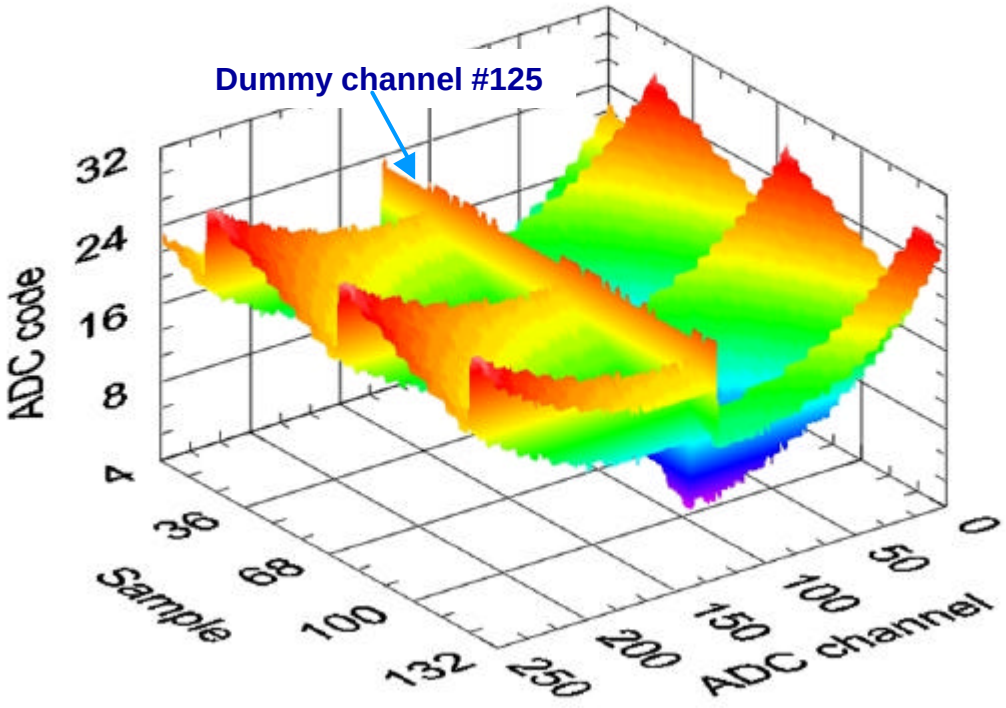


ASIC for CPC-1 readout

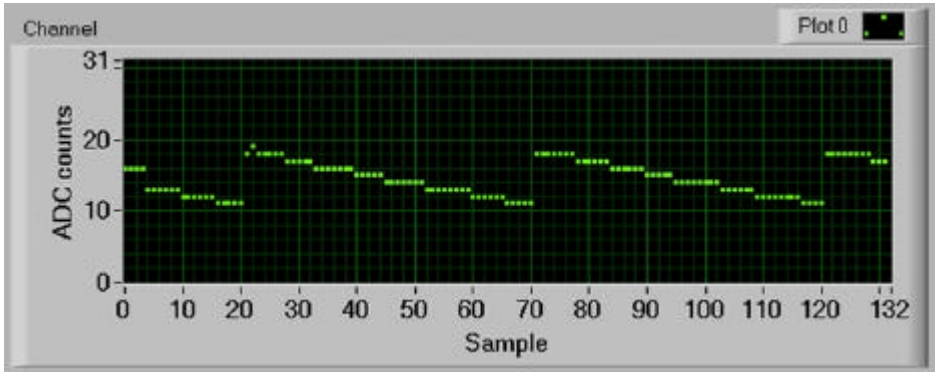
- Design: RAL Microelectronics Group;
- Voltage amplifiers for 1-stage SF outputs;
- Charge amplifiers for direct outputs;
- 20 µm pitch, 0.25 µm CMOS process;
- Wire- and bump-bondable;
- Scalable and designed to work at 50 MHz.

Stand-alone CPR1 tests

- test signal applied directly to ADC section: all 250 channels work fine;
- Non-uniform response: chip centre yields 150 mV lower output.

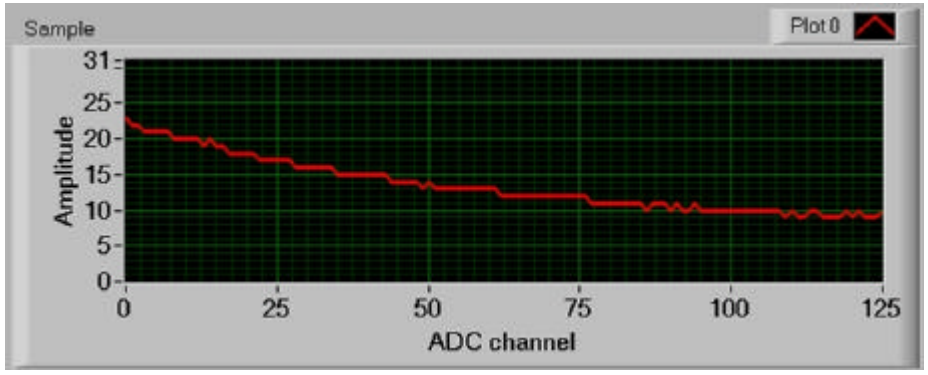


Slice along the the ADC array



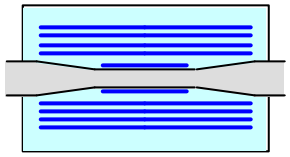
Time

Slice across the ADC array

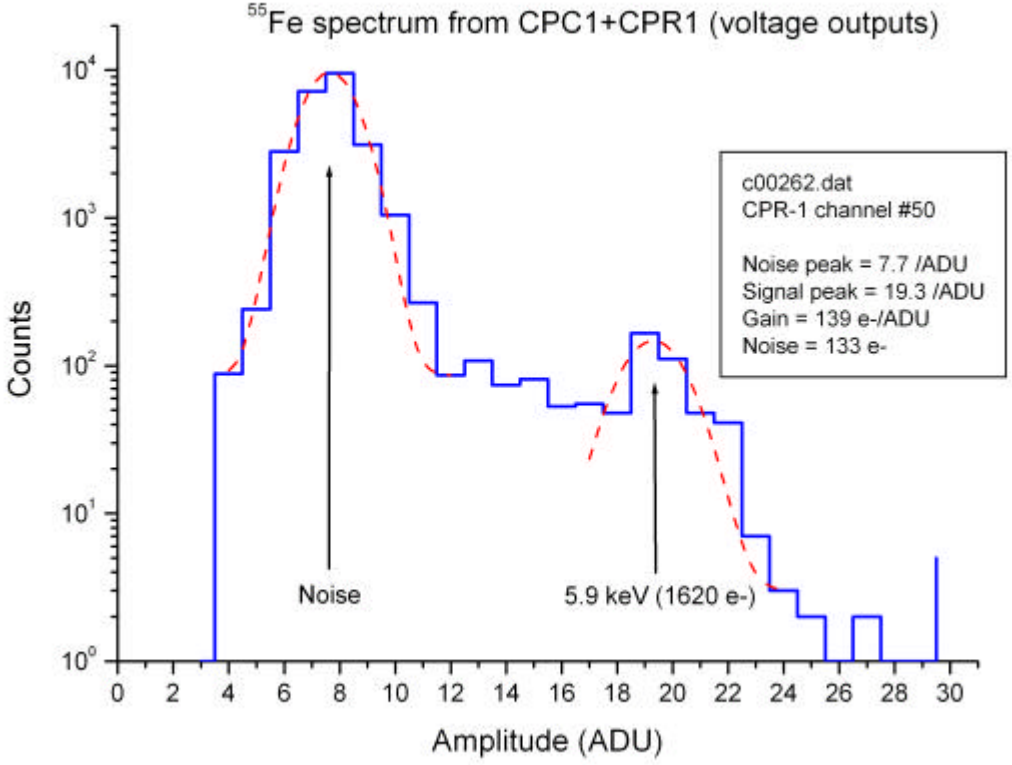


ADC channel

Testing CCD & CPR1 wire-bonded



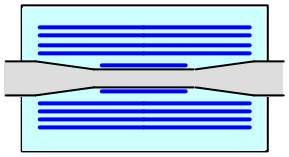
X-ray signals generated in CPC-1, amplified and digitised in CPR-1



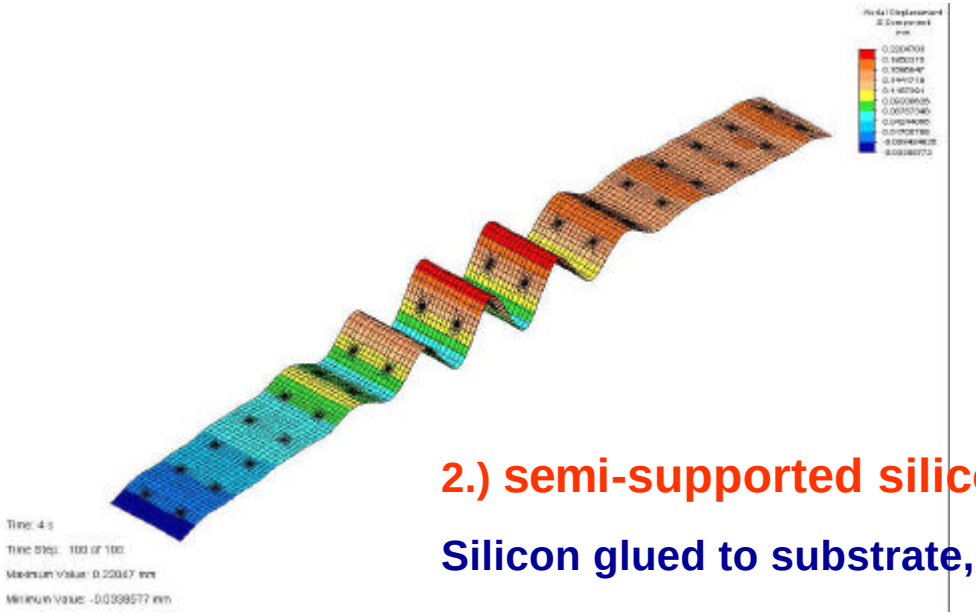
- **Several 1-stage SFs on CPC-1 bonded to voltage amplifier channels on CPR-1;**
- **1 MHz CCD clock and sampling frequency;**
- **Noise performance as expected;**
- **Capacitors on CPR-1 withstand >20 V – robust.**

Major milestone reached!

Thin-ladder development



Multiple scattering impairs physics performance – How thin can ladders be made?



Ideas:

1.) Unsupported silicon under tension:

Stiff in longitudinal direction, but laterally instable → not believed to be promising

2.) semi-supported silicon, thinned to epitaxial layer (> 20 μm):

Silicon glued to substrate, e.g. Beryllium, composites, ceramics, foams;

30 μm Si, 250 μm Be, 200 μm glue pillars (Nusil):

Measurement on physical models: about 150 μm ripples at – 35 C

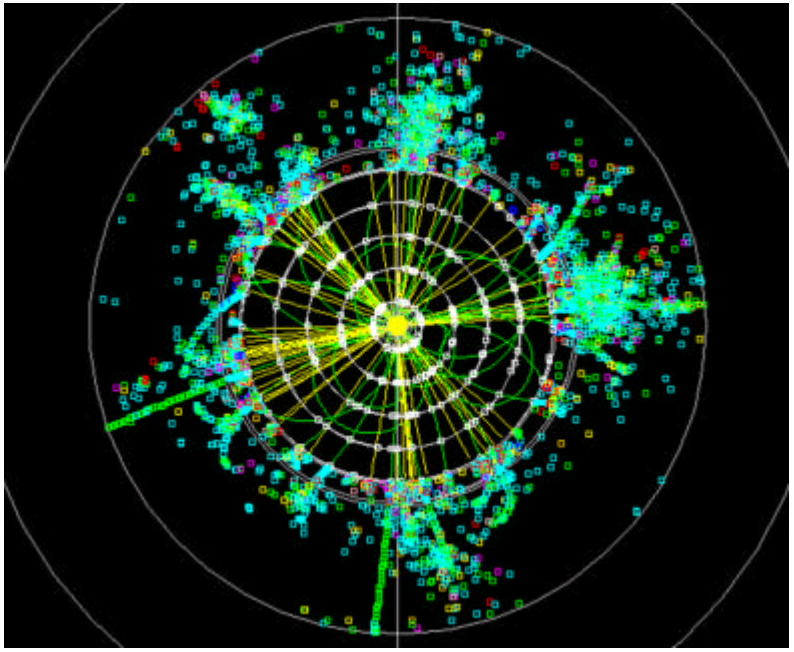
FEA-analysis (plot): about 160 μm ripples at – 60 C – qualitative agreement

3.) Novel Structures: replace glue pillars; micromechanical engineering

Physics Studies

study effect of different detector geometries (thickness, position, number of layers)

on physics performance using MC tools: JAS (OO software being developed at SLAC), SGV

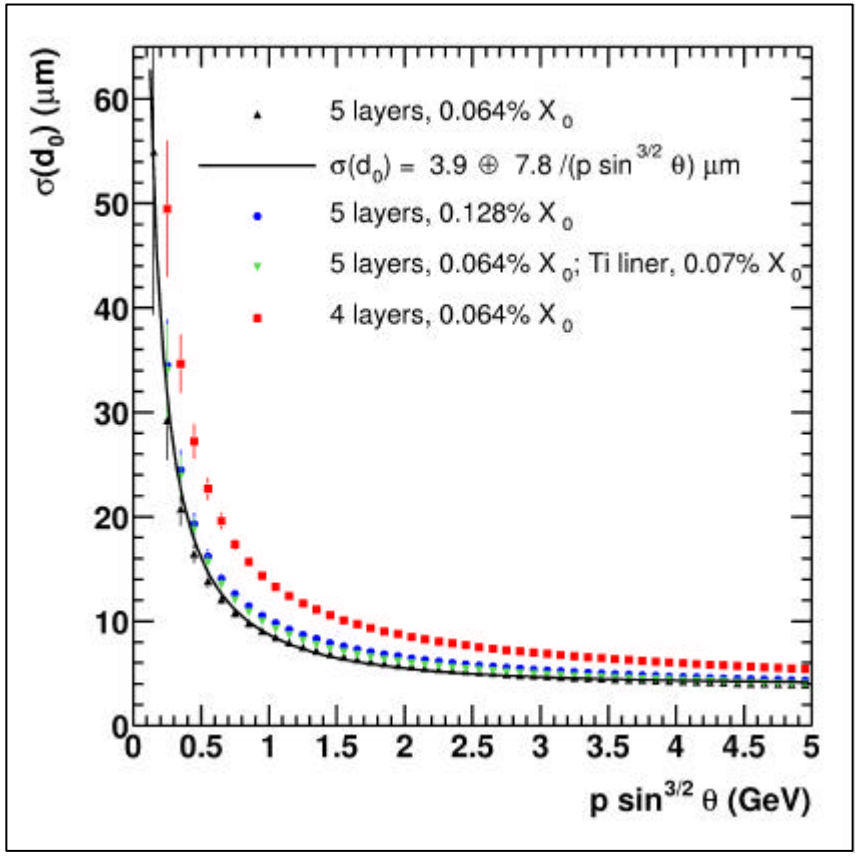


➢b-tag efficiency in multi-jet events:

(e+e- → Zh, e+e- → Zhh):

stronger dependence on jet energy

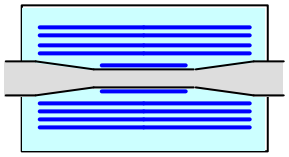
than on angle between the jets



➢Study of impact parameter resolution:

larger beam-pipe radius: worse resolution

Summary and Outlook



Sensor development:

- Excellent standalone performance of our first CPCCD and readout chip
- First signals obtained from wire-bonded assembly: major milestone reached
- Tests on bump-bonded assembly about to commence

Thin ladder R&D:

- qualitative agreement between measurements and FEA analysis of thinned Silicon with Beryllium support
- longer term: consider novel ideas → micromechanical engineering

Physics studies:

- develop existing flavour-tagging tools further and apply them to the ongoing studies of the influence of the detector geometry on physics performance