Development of the CMS Silicon Strip Tracker Readout

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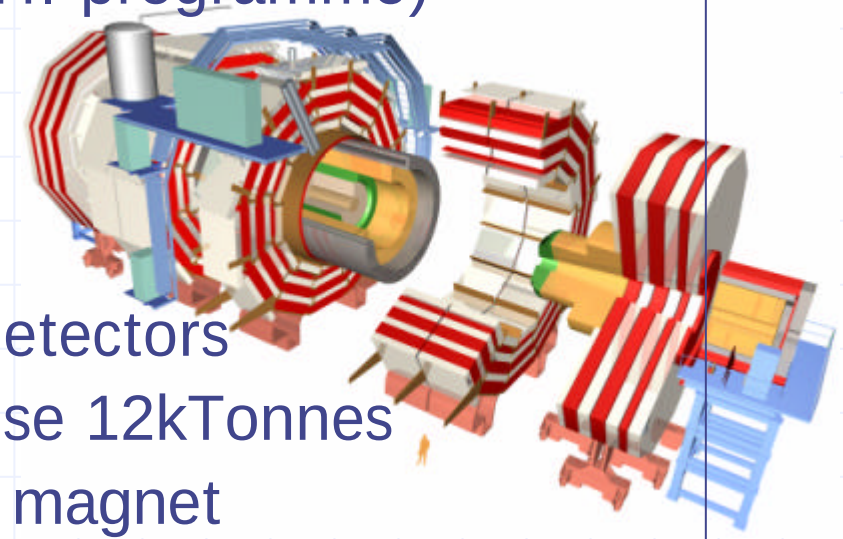
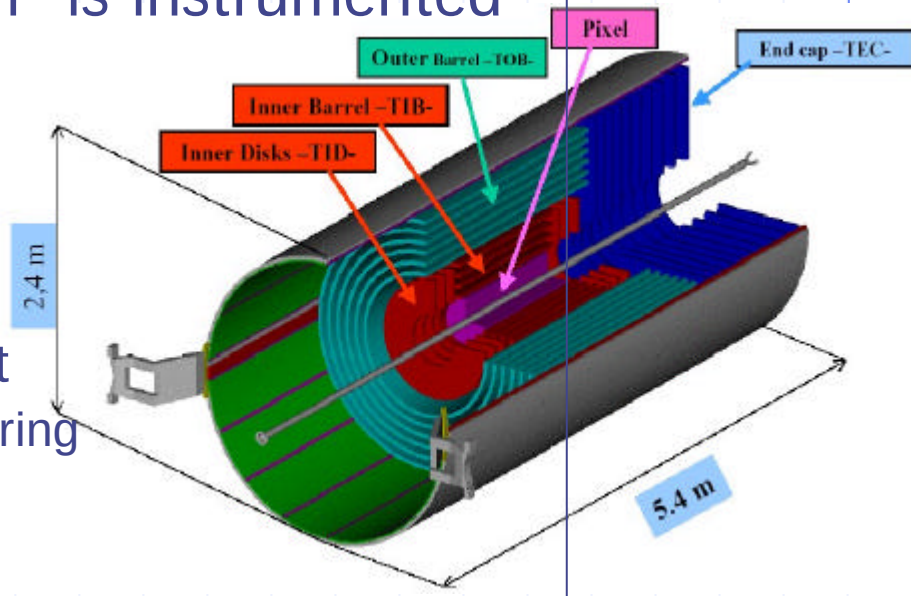
Introduction

- LHC: CERN, Geneva.
  - To replace LEP (same tunnel) starts ~2007
  - 14 TeV P-P collisions (+ HI programme)
  - Design L ~ 10^{34} $cm^{-2}s^{-1}$
  - Bunch Crossing ~40MHz
- CMS:
  - 1 of 2 General Purpose detectors
  - Solonoidal design, v. dense 12kTonnes
  - Largest superconducting magnet
  - L~21m, D~14m
  - Higgs, SUSY, others



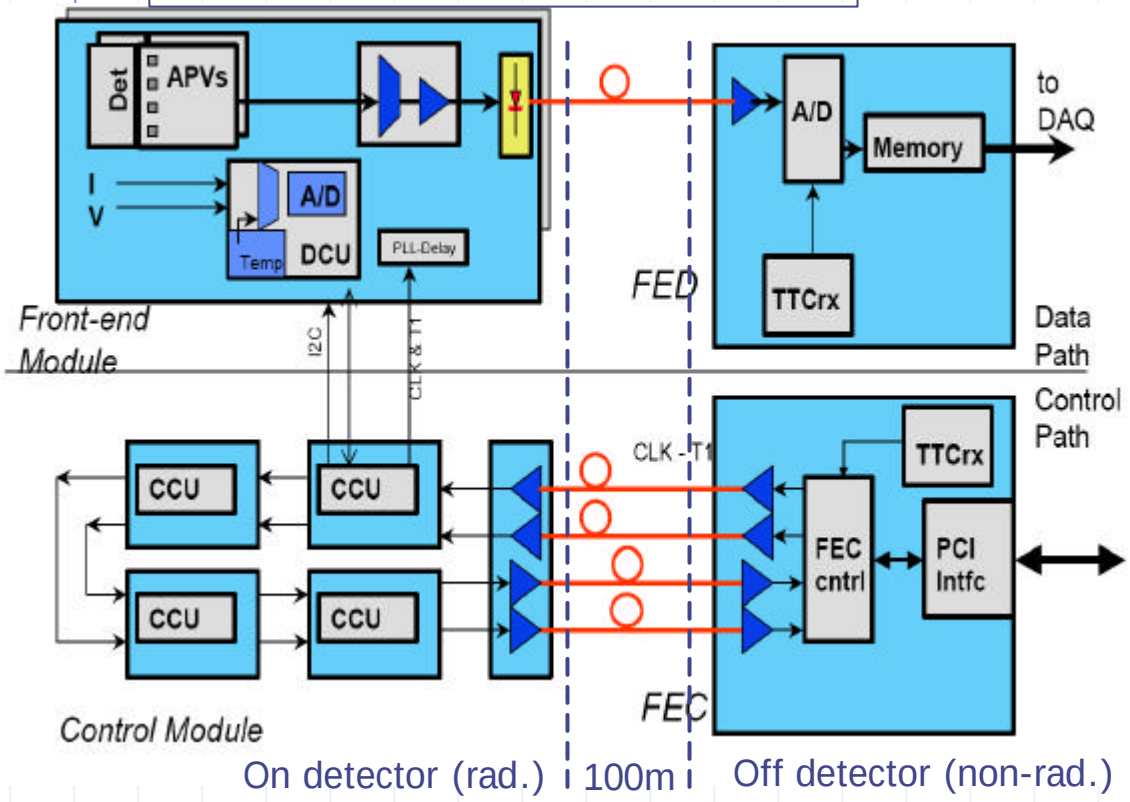
Silicon Microstrip Tracker

- Cylindrical volume of ~25m^3 is instrumented
  - ~210m^2 of Si
  - 10^7 Si Microstrip Channels
  - length 5.4m, Diameter 2.4m
- Analogue readout
  - No L1A decision involvement
    - On detector analogue buffering
      - APV25 (IC/RAL col.)
    - Expected rate ~100kHz
  - ~80000 Analogue Optical readout links
- Harsh environment
  - Operates in 4T magnetic field
  - Expected 10MRads integrated over lifetime
    - Everything on-detector is rad-hard



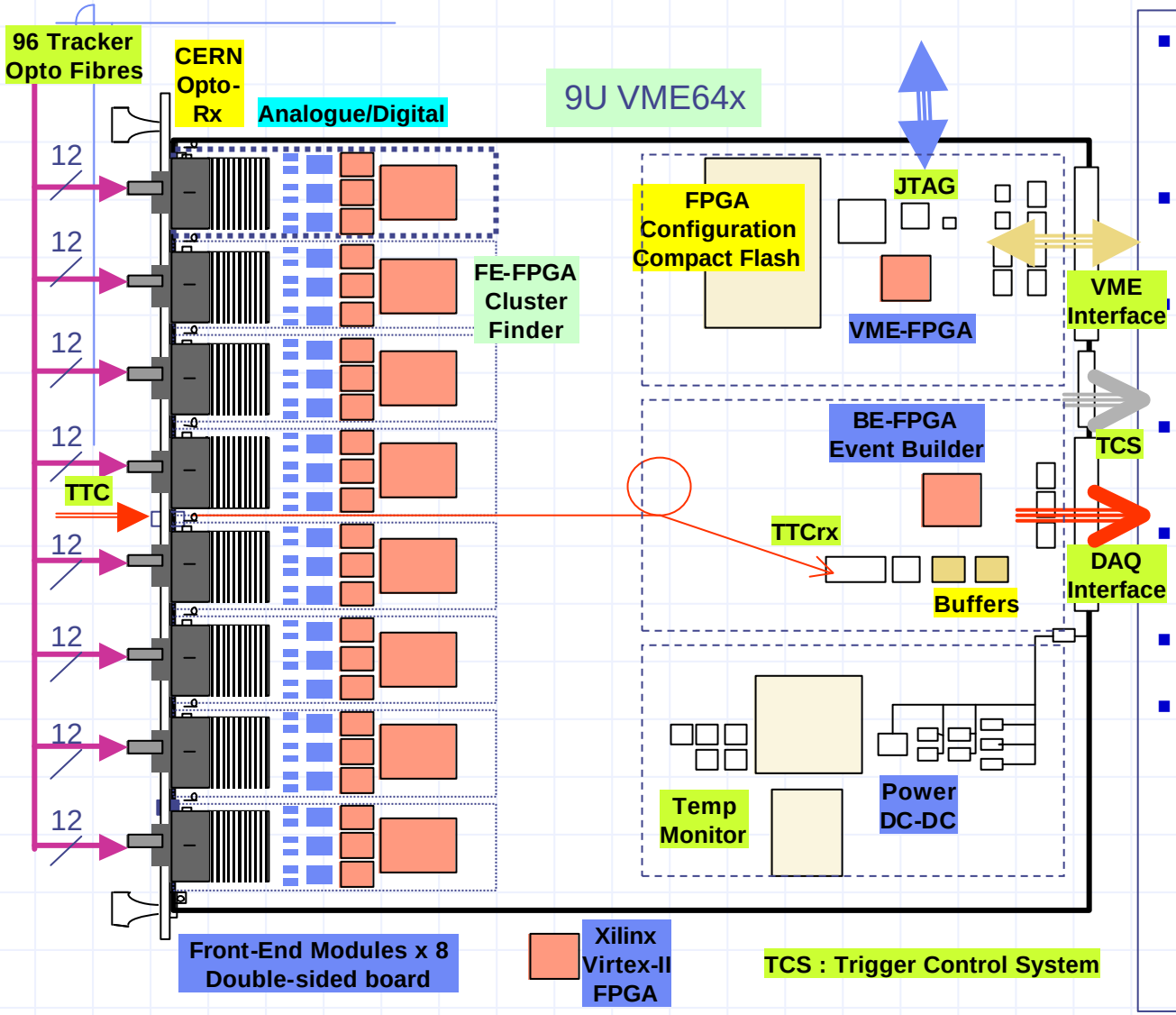
Control and Readout Architecture

- Generic
  - 40MHz
  - Occupancy ~ few %
  - Total noise < 2000e$^-$



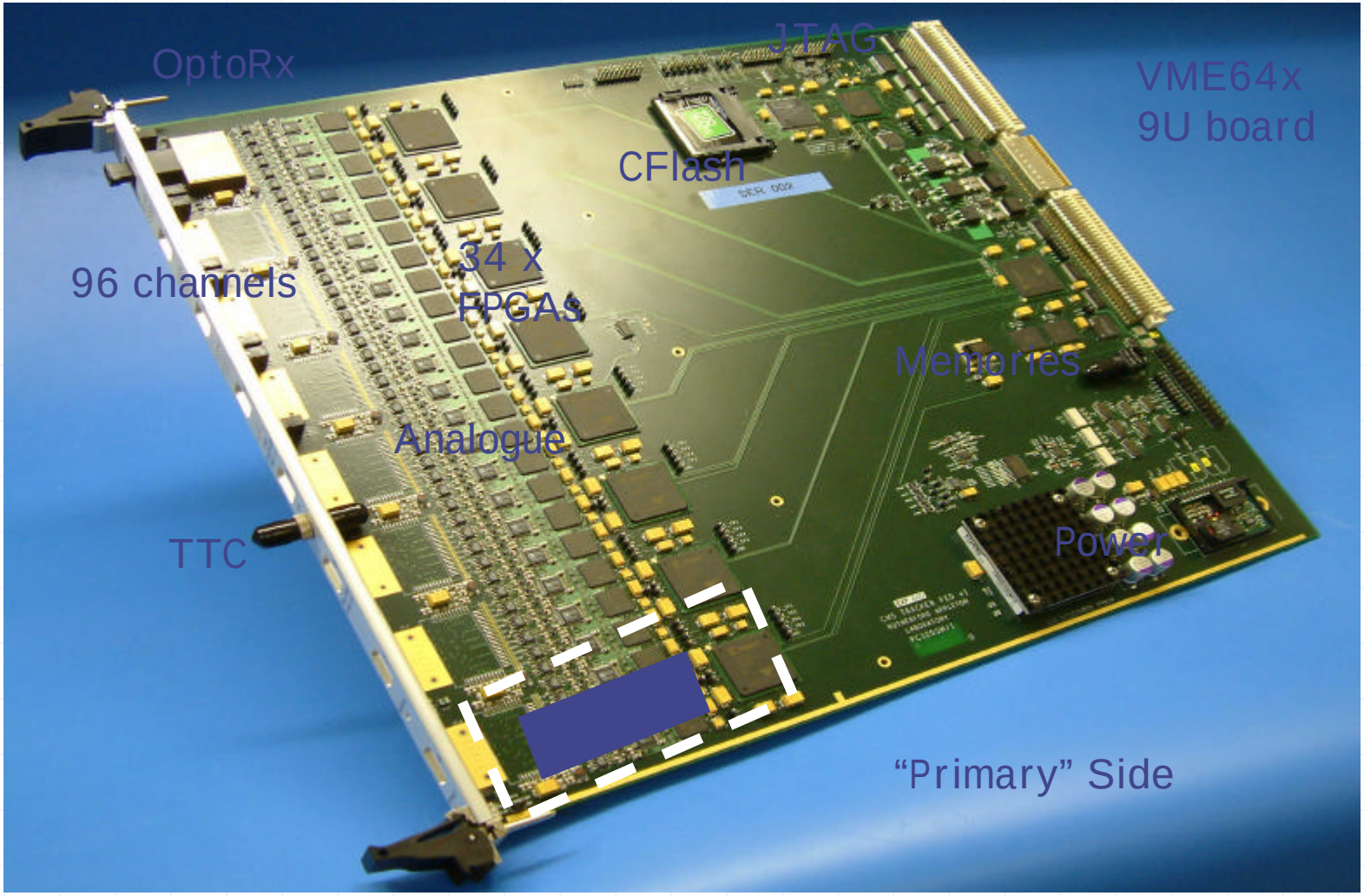
- Control
  - Token ring arch.
  - Timing ~ 1ns (indv. ch.)
  - I^{2}C on detector control
  - L1A ~ 100kHz
- Readout
  - 40MSs^{-1}
    - ~ 3GBs^{-1}FED^{-1}
  - Serialised: 256:1
  - Undersampling
  - Zero Suppression etc.

FED Architecture/Interfaces

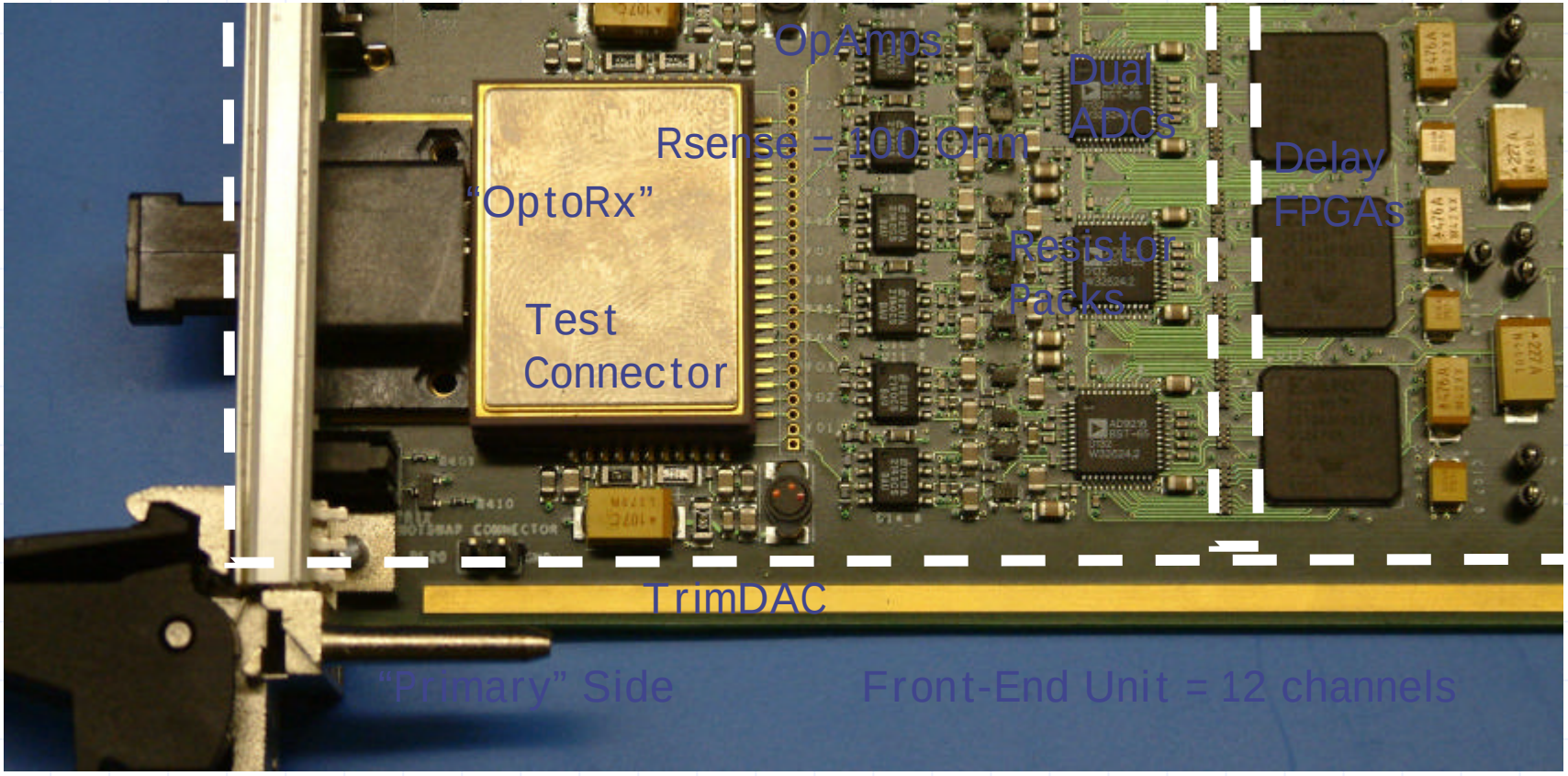


- 9U VME64x Form Factor
  - VME module / Configuration
- Modularity matches Opto Links
- 8 x Front-End “modules”
  - 96 channels in tot.
- OptoRx/Digitisation/Cluster Finding
- Back-End module / Event Builder
- Power module
- Other Interfaces:
  - TTC : Clk / L1 / BX
  - DAQ : Fast Readout Link
  - TCS : Busy & Throttle
  - *JTAG : Test & Configuration*

First FED Prototype (01/03)



CMS Tracker FED
Zoom in on FE Unit



"OptoRx" modules CERN project
Commercial Package with PIN Diode + **Custom Analogue ASIC**

FED Collaboration

- RAL responsibilities
  - Design/Layout
    - Complex analogue sec.
  - Firmware
    - Provide/test functionality
  - Low level software
    - Closely linked to firmware
    - Abstraction to middle UI
- Brunel responsibilities
  - software

- IC responsibilities
  - Modelling
    - Design sufficient?
  - Performance
    - Does it do what we need?
  - Software
    - Online interfaces
  - Test benches
    - Internal/Fed Tester

Development and Testing I

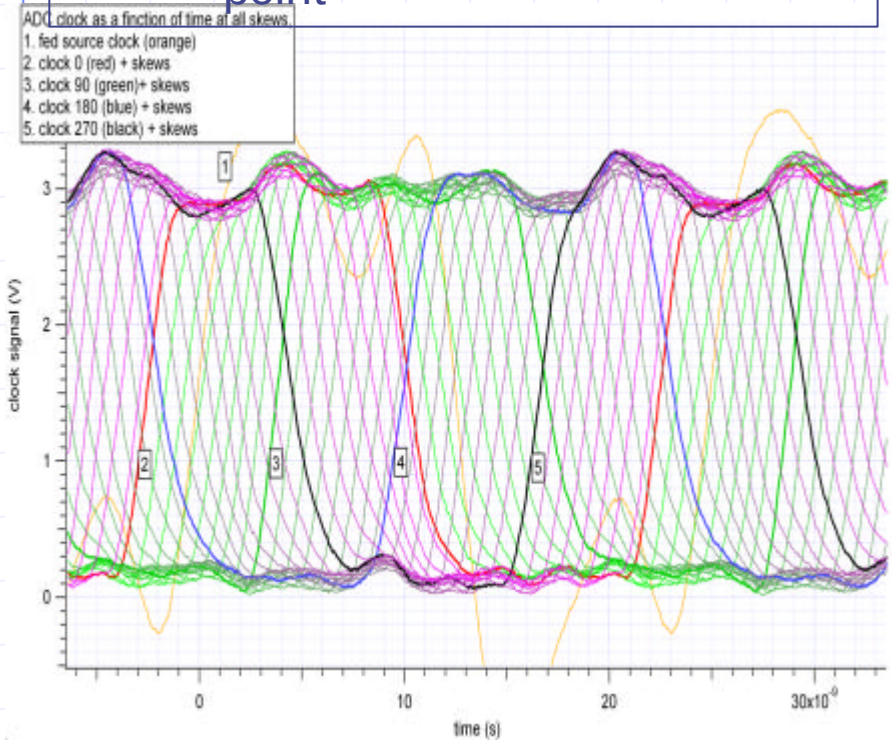
- Design Verification
  - Hardware (Hw)
    - Performance
    - Permits firmware
    - Has required interfaces
  - Firmware (Fw)
    - Performance
    - Provides functionality
    - Respects interfaces
    - Stable

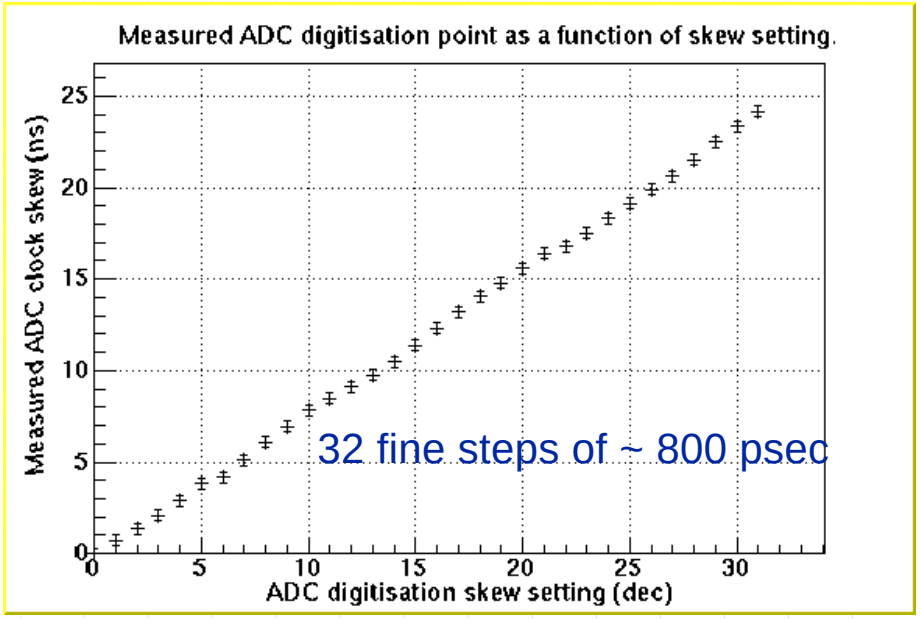
- Software (Sw)
  - Robust
  - Efficient
  - Abstracts complexity to user interface
  - Interfaces/respects online environment
- Nearly there...
  - FED in use
    - Pisa, CERN (now),
    - Lyon (after Easter)
  - Beam Test (25ns)
    - June and Oct. 04.
    - LHC-like conds.

Timing Functionality (M. Noy)

- Timing control crucial
  - Time-of-flight delays
  - Fibre propagation differences
- Undersampling readout
  - Careful choice of sampling point

- Xilinx® Virtex II® FPGA DCM
  - Implementation of clock skewing
  - 96 independent ADC clock points





Development and Testing II

- Need ~500
- Have seen failures
  - Problem for similar ATLAS boards
  - BGA Soldering problems (batch 10.03)
  - Overcome with latest batch (03.04)
- Produced in industry
  - JTAG B.S. amongst others.

- Internal/Self Testing (M. Noy)
  - Significant software task
  - Development of robust algorithms
  - Abstract complexity
    - Simple interface
    - Pass/Fail decision
- Provides
  - Rapid, accurate feedback to assembly co.
  - Identification of:
    - Assembly mistakes
    - Component failures

Summary

- FED card
  - First off detector electronics
  - 9U VME form
  - 96 ADC ch, ~3GBs^{-1}
    - V. dense analogue sec.
    - 36 FPGAs (big, complex)
- Hw, Fw, Sw
  - High degree of development,testing required, and done
  - Robust, stable, nearly full functionality
  - Performant

- Production
  - Begin 2005
    - We will be ready.
- In Use
  - CERN, Pisa (now)
  - Lyon (soon)
  - Beam Test
    - June, Oct. 04.