Some Aspects of Epitaxial Silicon
(Based on my previous life at Okmetic Plc)

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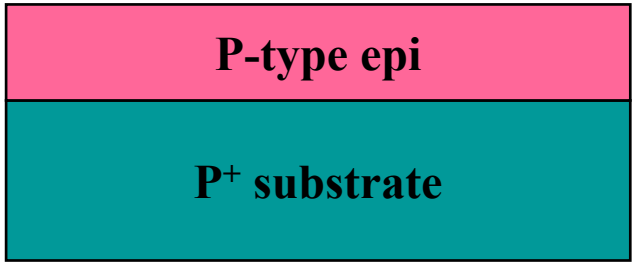
- Epitaxy process and equipment
- Properties of epitaxial wafers
- Defects and contamination

Epitaxy

- Epitaxy = Deposition of single crystalline layer of semiconductor.
- Deposition is done on a single crystal substrate (silicon wafer).
- High temperature process 700- 1200^{o}C.
- Deposition from vapour phase with CVD.
- Precursors $SiCl_4$, $SiHCl_3$, SiH_2Cl_2 or SiH_4.
- More than 70% of all silicon wafers get epi on them.
- Two types of epi: blanket or in-line.
- Atmospheric process for blanket epi. Reduced pressure often used for in-line epi.

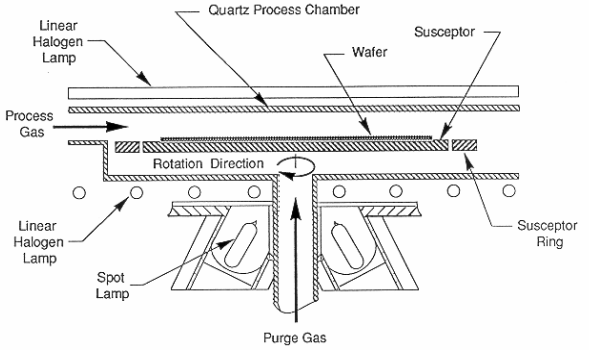


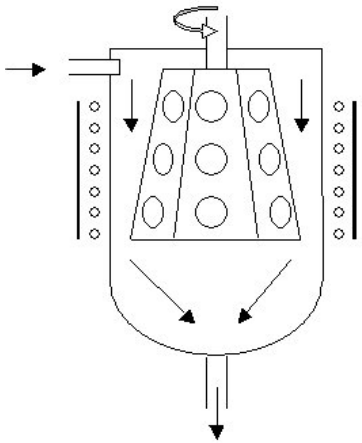
Features of epitaxial wafers

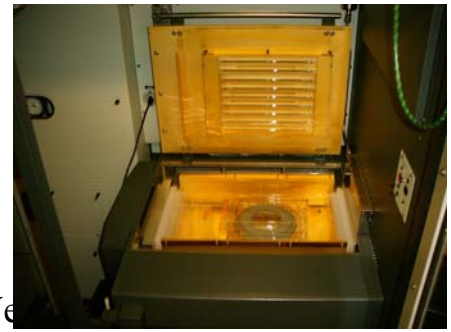
- The epitaxial layer lacks some of the impurities (C, O) and defects (COPs) of the substrate wafer.
- The resistivity of the epi layer can differ from the substrate by a factor of 10000.
- The electrical interface between substrate and epilayer is abrupt and sharp.
- The resistivity of the epi layer is reproducible and uniform.
- The thickness of the epi layer is very reproducible and uniform.
- Complicated multilayer structures are possible.
- And it's relatively expensive.

Reactors

- **Two types of reactors: single wafer and batch.**
- **Process chamber made out of fused silica.**
- **During processing wafer rests on a SiC coated graphite susceptor.**
- **Heating inductively or with lamps.**

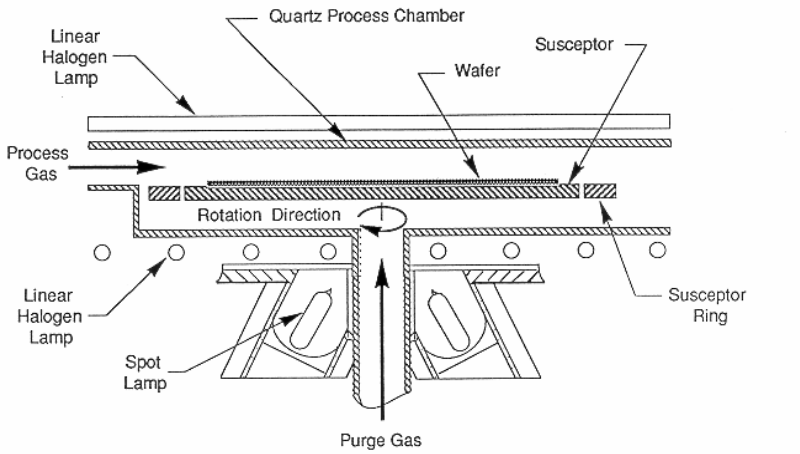






Advantages of the single wafer reactor

- **Heating by IR lamps: fast**
- **Horizontal laminar gas flow: less autodoping**
- **Very low particle levels**
- **Excellent thermal profile: less slip**
- **Excellent stability and uniformity**
- **Lower cost for large wafers and thin epi**

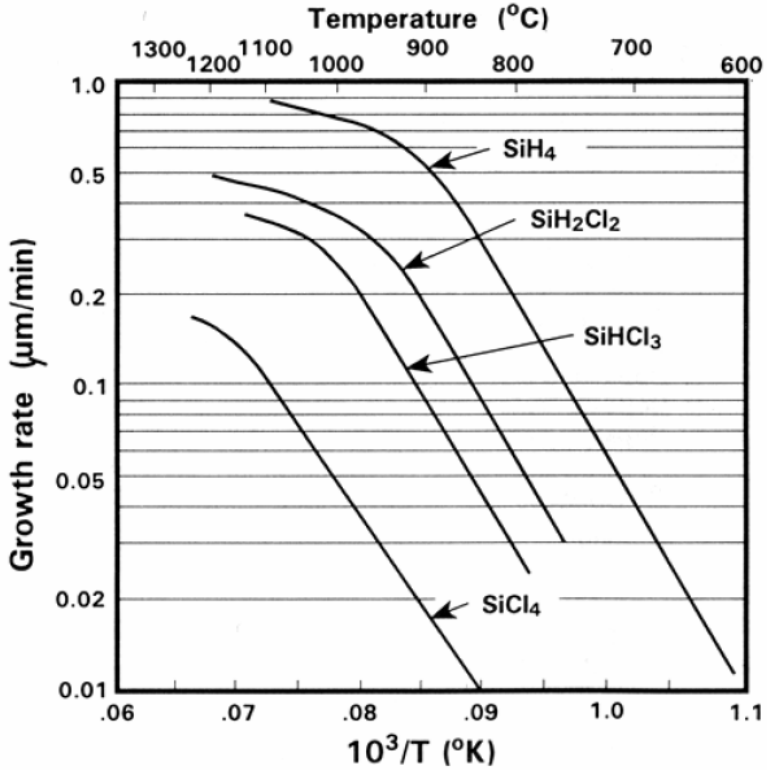


Process

- Reactor etched clean with HCl prior to deposition.
- Wafer(s) loaded in by wafer handler (or manually in batch process).
- Native oxide removal at 1120-1200 ^{o}C. (Other techniques used for low temperature epi processing.)
- Typical epi deposit temperature 1080- 1190 ^{o}C with trichlorosilane (TCS) and 950- 1080 ^{o}C with dichlorosilane (DCS). H_2 used as carrier gas.
- Dopants: PH_3, AsH_3 (n-type) or B_2H_6 (p-type).
- Deposition rate:4 - 4.5 µm/min (TCS) and 1 - 1.5 µm/min (DCS) Total process time: 8 minutes for 10 µm epi (TCS process).

Deposit rate and temperature

- Epi growth rate depends on temperature.
- High growth temperature is also advantageous due to reduced stacking faults.



Who uses epi?

Technology	Use	Epi structure	Typical thickness (µm)	Typical resistivity (ohm-cm)	Advantages	Comments
CMOS	Digital Ics	p/P^+	5-20	5-10	Minimize latch-up	Backsealing!
MOS	Power devices	n/N^+	10-20	5-10	Thick doped layer	
MOS	CCD	n/N^-	20-30	25-35	Uniformity, low leakage	
Analog bipolar	Amplifiers, Power devices	p/P^+	10-100	1-40	Thick doped layer	
Analog bipolar	**Optical, X-ray detectors**	**n/N^+**	**30-40**	**300-2000**	High resistivity, low leakage	Backsealing!
MEMS	Etch stop, active layer of device	n/P $p/P^{++}/N^-$	7-15	1-10	Uniform layer, abrupt interface	Usually DSP-wafer

Important specifications for epi wafers

- Epi thickness.
- Thickness variation (within wafer and wafer-to-wafer).
- Dopant.

- Epi resistivity.
- Resistivity variation (within wafer and wafer-to-wafer).
- Defect levels: particles and stacking faults.
- Allowed metallic contamination level.

Single Wafer Process Performance

- Typical
  - Thickness uniformity (wafer-to-wafer) 1.0%
  - Resistivity uniformity (wafer-to-wafer) 4.0%
- Best
  - Thickness uniformity (wafer-to-wafer) 0.60%
  - Thickness uniformity (within wafer) 0.85%
  - Resistivity uniformity (wafer-to-wafer):
    - <10 Ohm-cm 2.0%
    - 10-50 Ohm-cm 4.5%
  - Resistivity uniformity (within wafer):
    - <10 Ohm-cm 1.5%
    - 10-50 Ohm-cm 3.0%

Resistivity range (in production)

	Resistivity		Carrier concentration	
Dopant:	Minimum (ohm*cm)	Maximum (ohm*cm)	Minimum (cm^{-3})	Maximum (cm^{-3})
B	0.0005	50	$2.5*10^{14}$	$2.4*10^{20}$
P, As	0.04	1200	$3.5*10^{12}$	$3.3*10^{17}$

Problems with Epitaxial Wafers

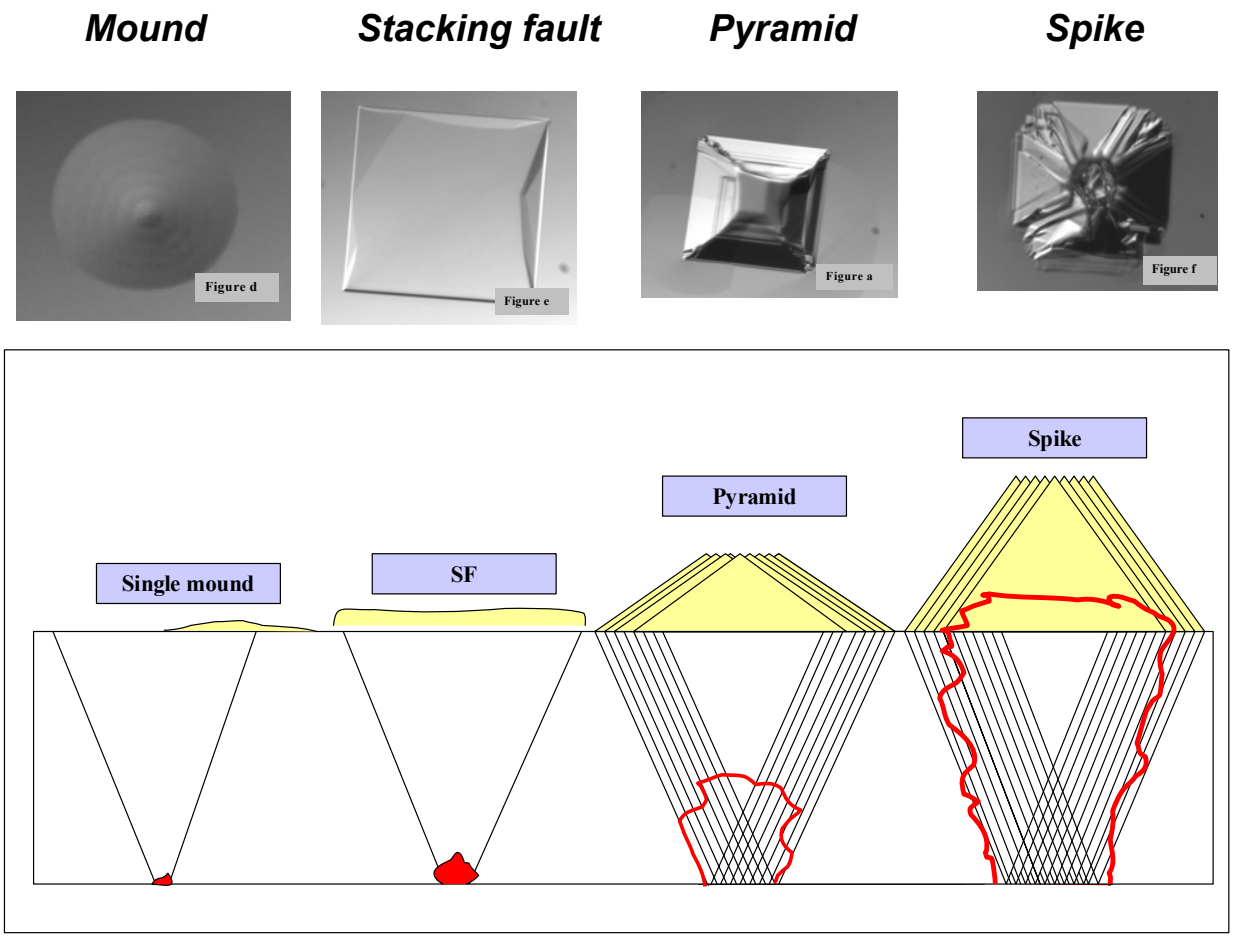
- Autodoping.
- Surface defects (stacking faults).
- Metallic contamination

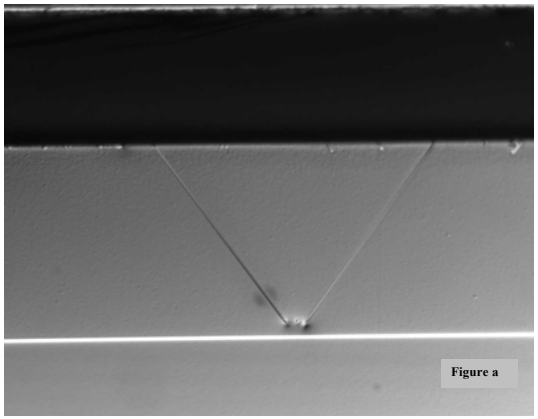
Autodoping

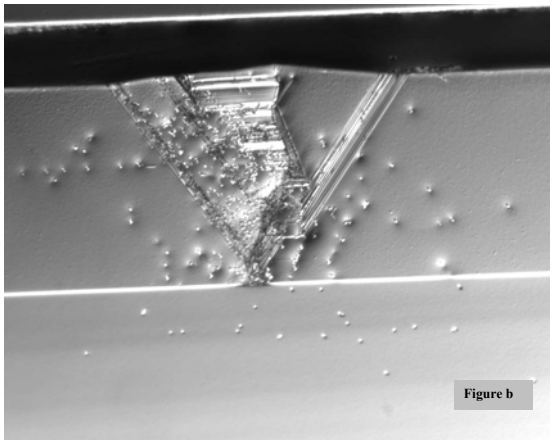
- Autodoping: unintentional doping due to background impurities (from substrate, reactor, gases…)
- Autodoping is reduced primarily by raising hydrogen flow which increases the potential for slip and resistivity uniformity problems.
- For lowest background doping (high resistivity), a high growth rate is essential.
- Resistivities of 1000-2000 ohm-cm are routinely produced on Sb-doped substrates.
- Resistivities of up to 10000 ohm-cm are technically possible.

Stacking faults

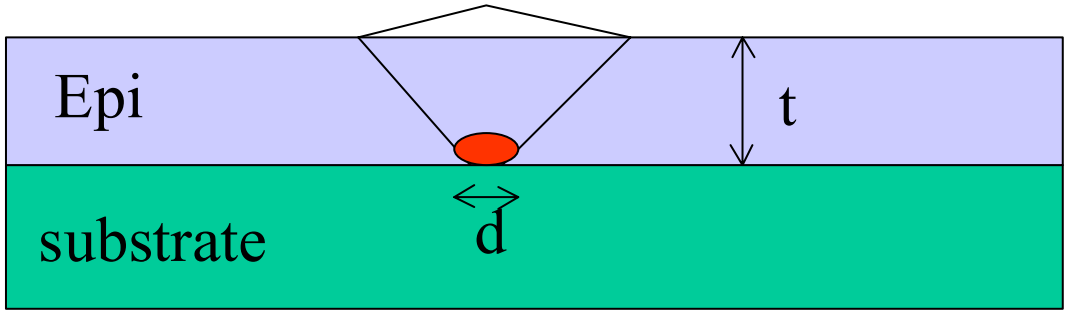
- Also called pyramids, hillocks or mounds.
- Defects originating from the epi-substrate interface.
- Typically 0 - 2 SFs on a wafer.
- Affect subsequent processing, especially lithography and wafer bonding.
- Cause high leakage currents if within the active area of device.







- Stacking fault is caused by a defect on the starting wafer surface (particle, damage, oxide island...).
- Quality of starting surface is crucial for the prevention of SFs.
- SF grows on the (111) plane.
- Size is proportional to epi thickness.



$$s = d + \frac{2t}{\tan(54.74°)}$$

Metallic Contamination

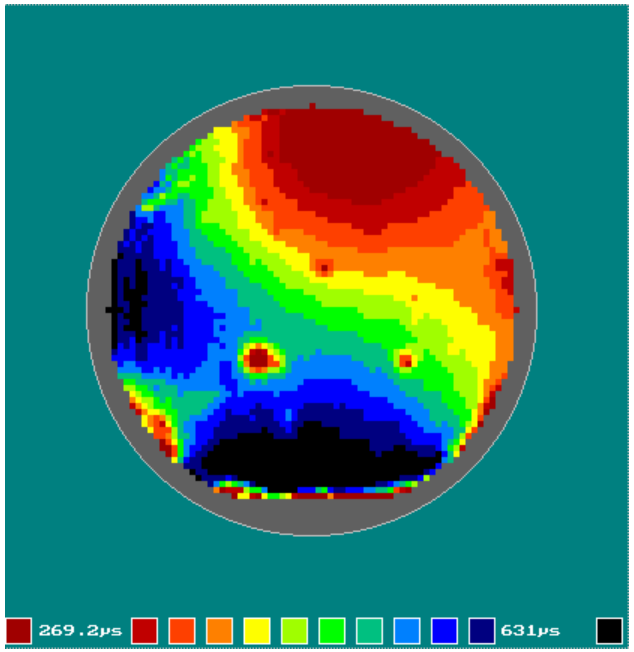
- Leakage currents can be significantly increased by metals.
- In most applications most contamination occurs during device processing. Metal levels are controlled by gettering.
- For some applications (i.e. detectors) low metal levels have been found to be important.
- Due to measurement problems knowledge about contaminants and contamination sources is patchy.

Metallic Contamination

- Important contaminants: Fe, possibly Mo and Ti, occasionally Cu and Ni.
- Cu and Ni are very fast diffusers; Fe moderately fast; Mo and Ti slow.
- Behaviour of Fe is known best due to easy, quantitative measurement in p-type material using recombination lifetime.
- Recently quantitatitive techniques for Cu have been developed.

Metallic Contamination: Fe, Mo, Ti

- Epi process is inherently clean due to high concentration of Cl and H_2 in the ambient.
- Normally epi contains a slow diffusing contaminant (either Mo or Ti) in significant concentrations. The source of this contaminant is not known and it cannot be controlled.
- Fe contamination occurs due to contamination from equipment: Leaks in gas system (Cl containing gas), pinholes in SiC coating of susceptor, or faulty pre-epi cleaning.



Metallic Contamination: Cu and Ni

- Fast diffusers (Cu and Ni) tend to segregate to wafer surface during cooldown.
- Cu, however, can also precipitate in n-type silicon. (Formation of Cu precipitates is controlled by the Fermi-level.)
- Source of Cu is polishing slurry. P-type substrates may contain relatively high levels of Cu!