Introduction to Electronics for High Energy Physics

CERN Summer school 2005

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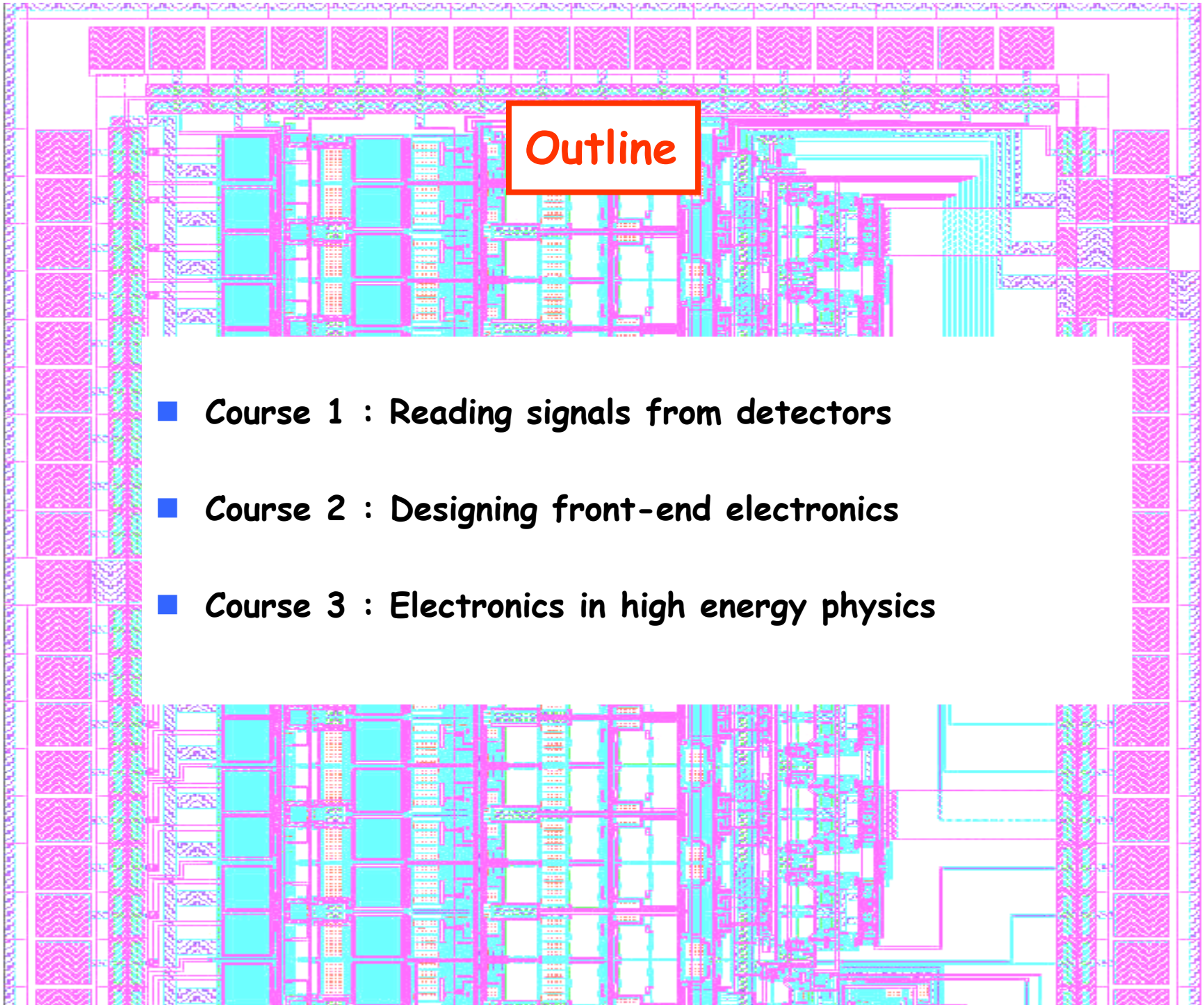
CENTRE NATIONAL DE LA RECHERCHE SCIENTIFIQUE



Outline

- Course 1 : Reading signals from detectors
- Course 2 : Designing front-end electronics
- Course 3 : Electronics in high energy physics

Introduction

- **Speak "electronician" in just 3 lessons…**
  - "Did you cascode your charge preamp to increase your open loop gain ?"
  - "Did you find an FPGA with LVDS I/Os for your digital filter ?"
  - A lot of vocabulary (and abreviations…) to get used to, but :

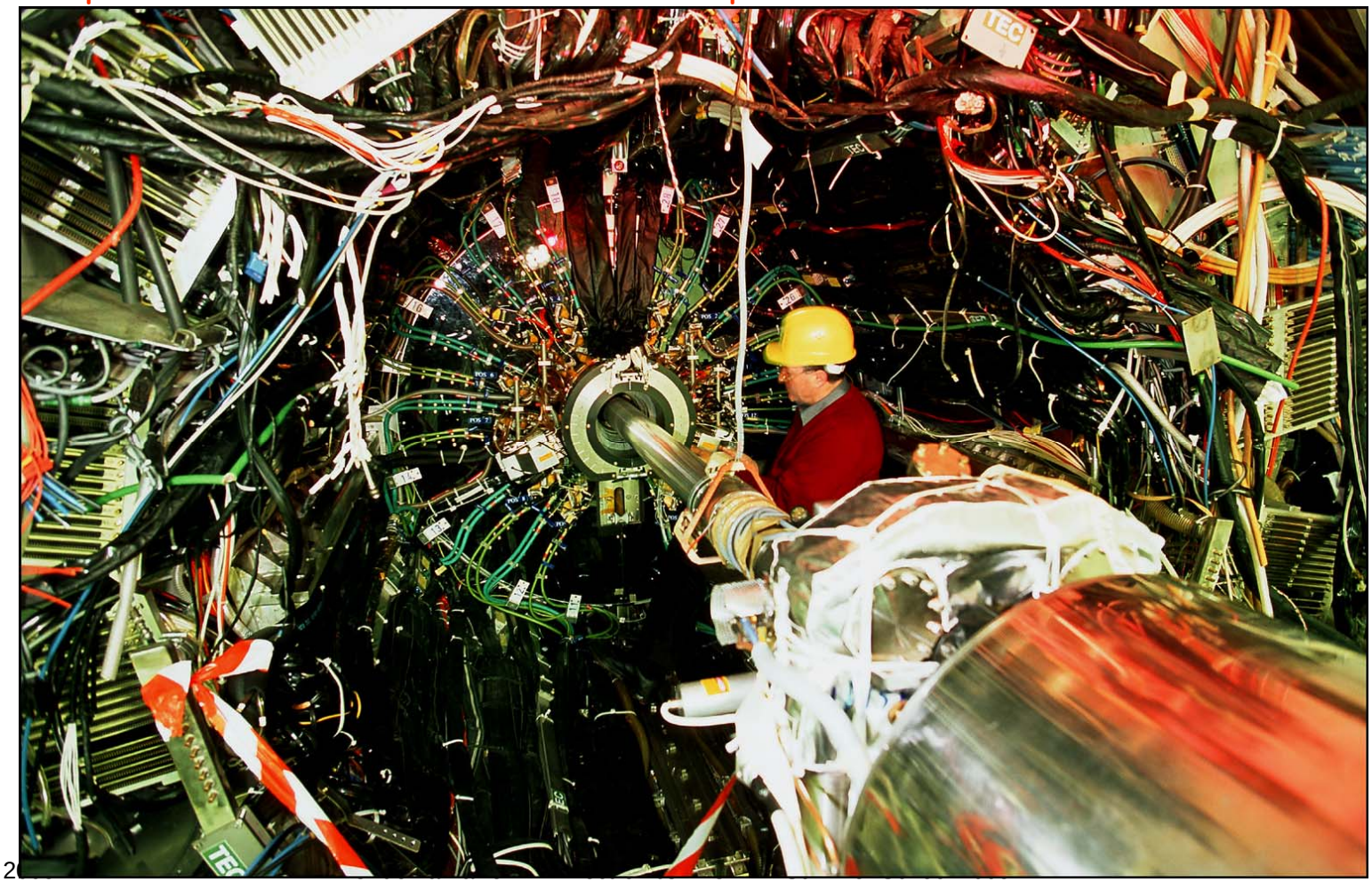
- **Little prerequisite knowledge required :**
  - Ohm's law : U = Z I
  - Some basics of Fourier (or Laplace) transforms cannot hurt for signal theory

  - *Many more details are given in the transparencies -> don't be scared !*

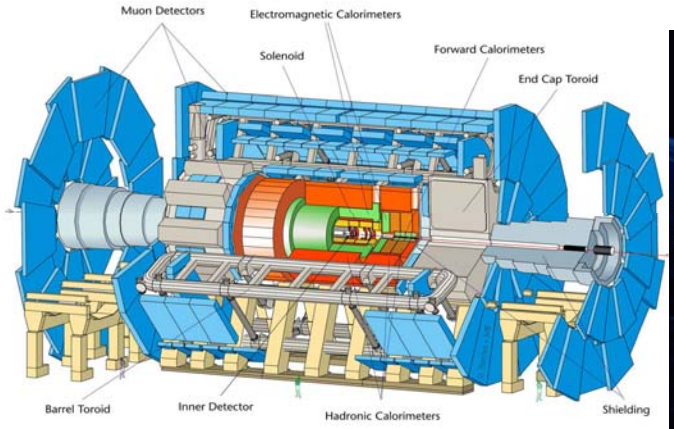
  - *Emphasis on front-end electronics : « electronics for physicists » not engineers*

Electronics in experiments

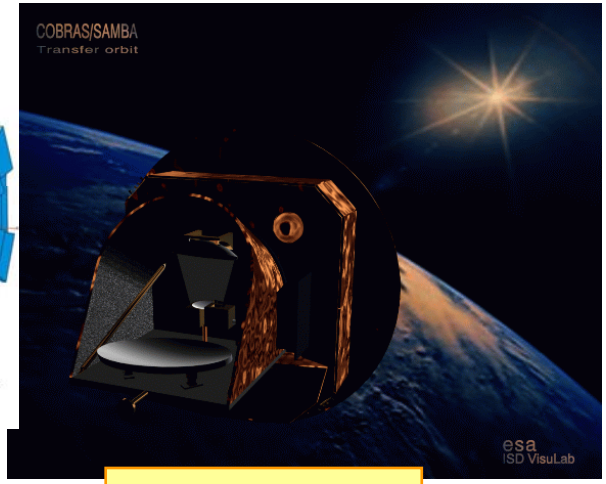
- **A lot of electronics in the experiments…**
  - Readout electronics : amplification, filtering… : Analog electronics (A,V,C)
  - Processing & Trigger electronics : Digital electronics (bits) [see lecture by P. Sphicas]
  - The performance of electronics often impacts on the detectors



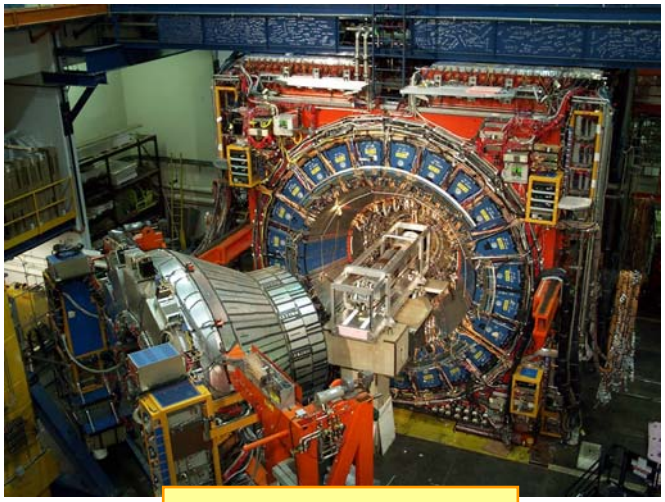
A large variety of detectors…



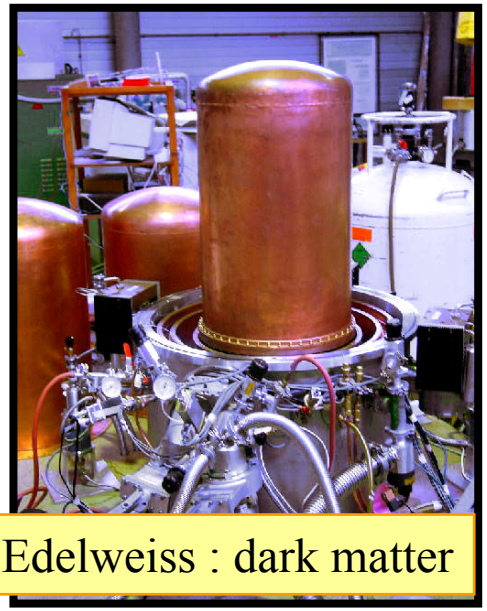
ATLAS : Higgs boson



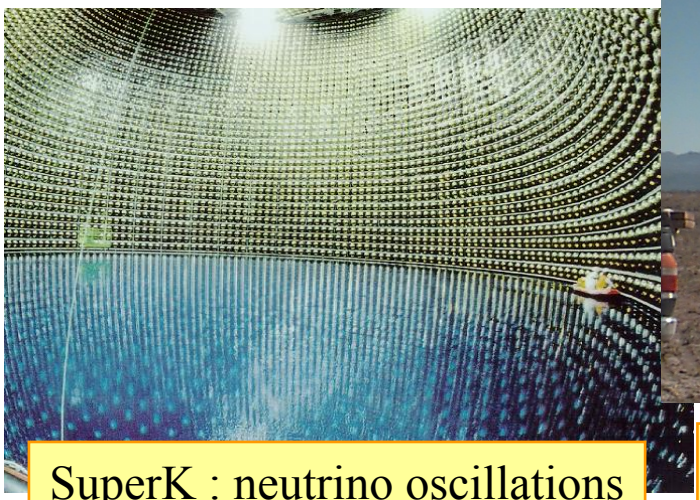
Planck : CMB



CDF : top quark



Edelweiss : dark matter



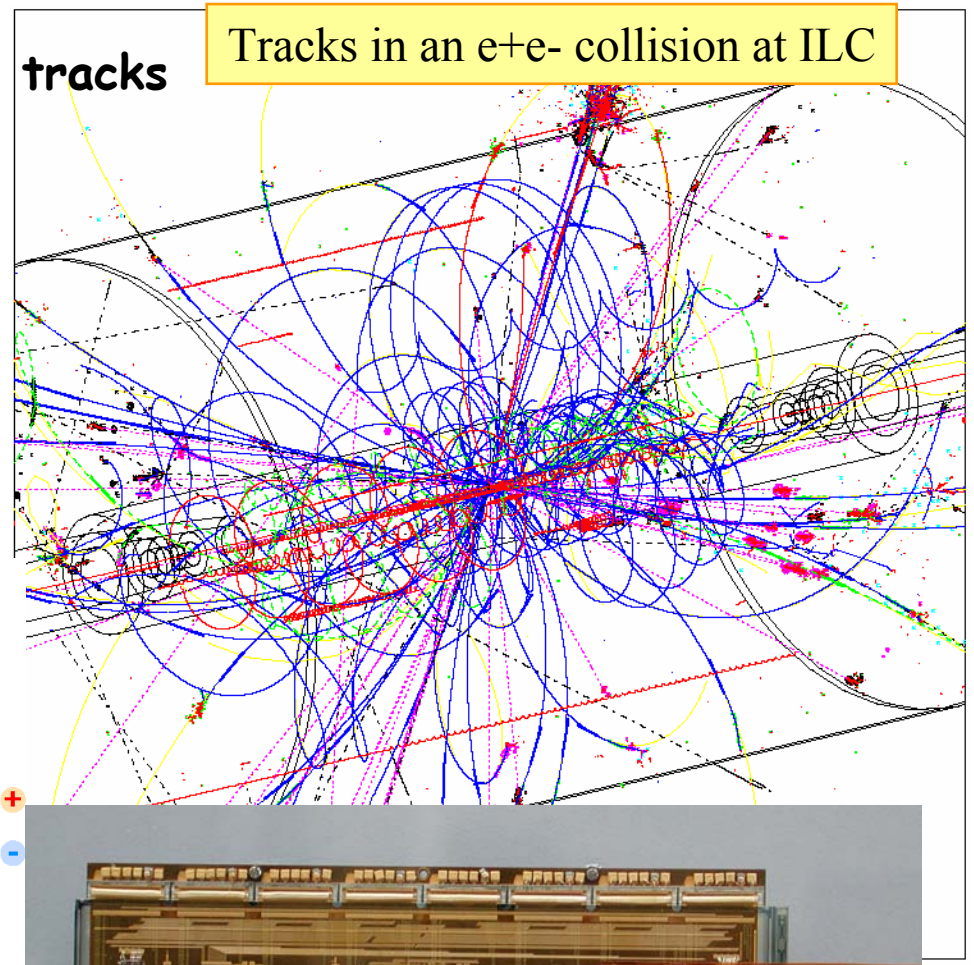
SuperK : neutrino oscillations

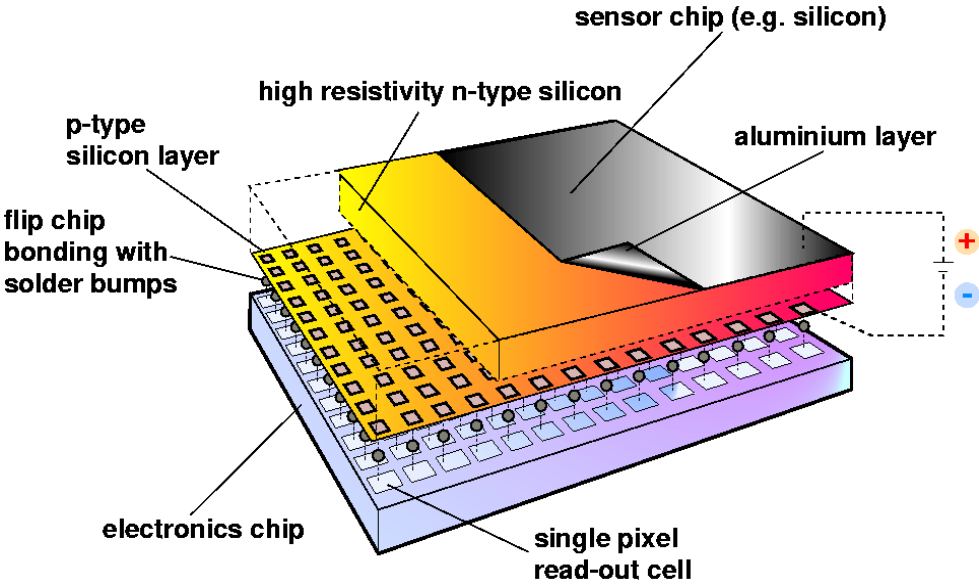
AUGER : cosmic rays 10^{20}eV

Electronics allowing better detectors : trackers

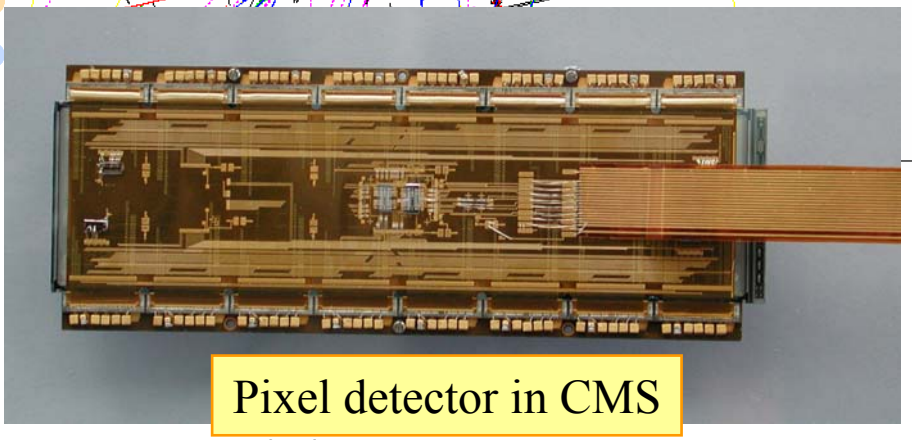
- **Measurement of (charged) particle tracks**
  - millions of pixels (~100 μm)
  - (quasi) binary readout at 40 MHz
  - High radiation levels
  - Made possible by ASICs

Tracks in an e+e- collision at ILC





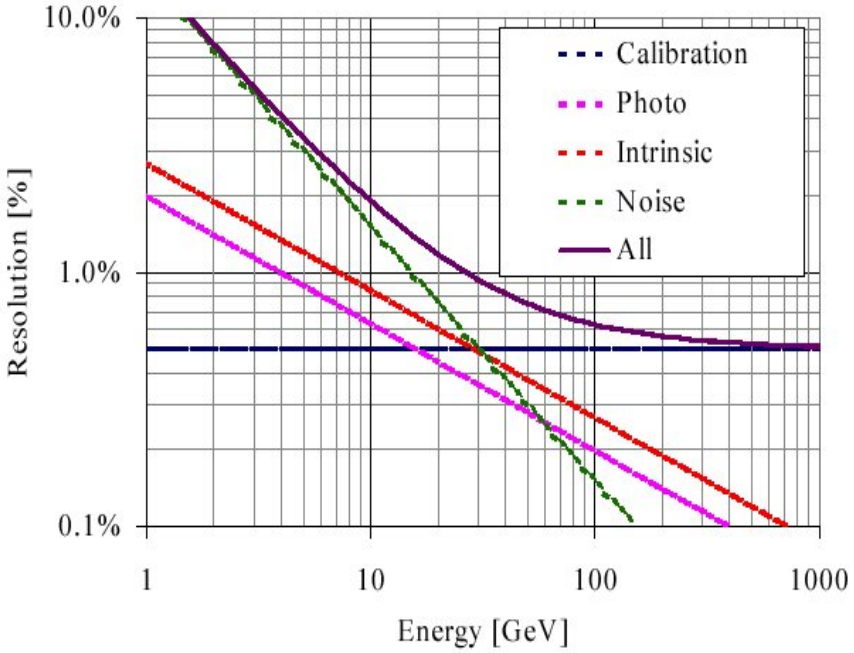
Pixel detector and readout electronics



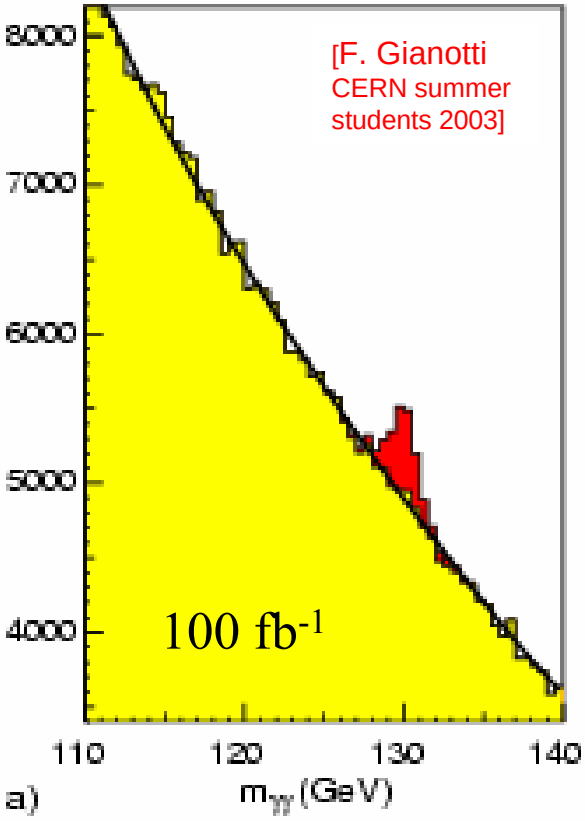
Pixel detector in CMS

Importance of electronics : calorimeters

- **Calorimetry = energy measurement** (≈ mass)
- **Dynamic range : maximum signal/minimum signal (or noise)**
  - Typically : 10^3 – 10^5
  - Often specified in dB (=20log Vmax/Vmin) = 60 – 100 dB
  - Also in bits : 2^n = Vmax/vmin = 10 – 18 bits
- **Precision ~1%**
  - Energy resolution : **σ(E)**
  - Importance of low noise, uniformity, linearity…

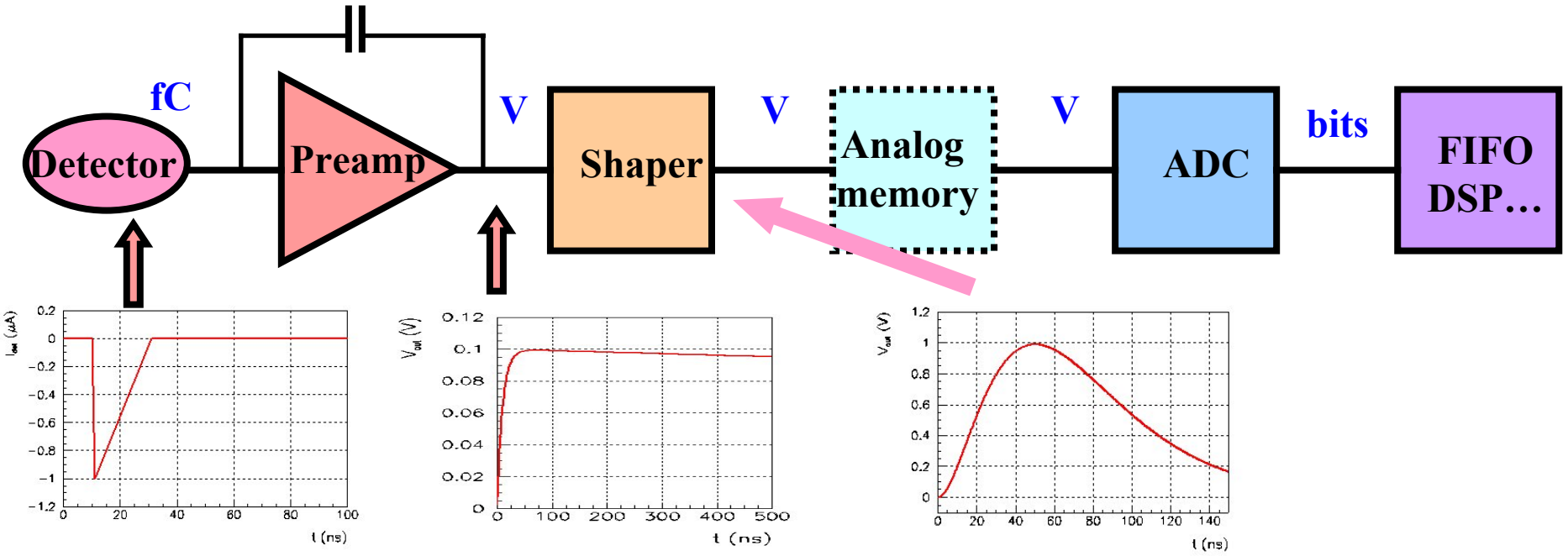


H-> γ γ in CMS calorimeter



Overview of readout electronics

- Most front-ends follow a similar architecture



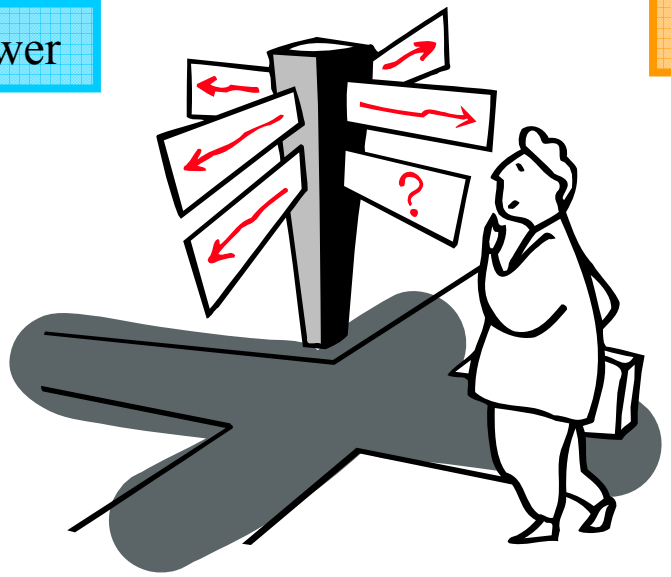
- Very small signals (fC) -> need amplification
- Measurement of amplitude and/or time (ADCs, discris, TDCs)
- Several thousands to millions of channels

Readout electronics : requirements

Low noise

Low power

High speed



High reliability

Large dynamic range

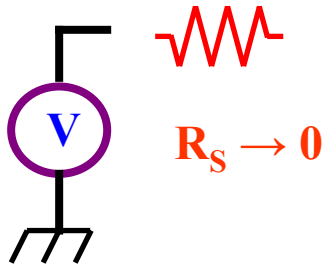
Radiation hardness

Low cost !
(and even less)

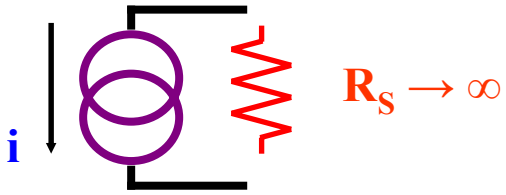
Low material

The foundations of electronics

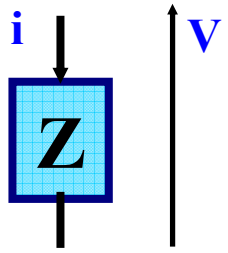
- **Voltage generators or source**
  - Ideal source : constant voltage, independent of current (or load)
  - In reality : non-zero source impedance R_S



- **Current generators**
  - Ideal source : constant current, independent of voltage (or load)
  - In reality : finite output source impedance R_S

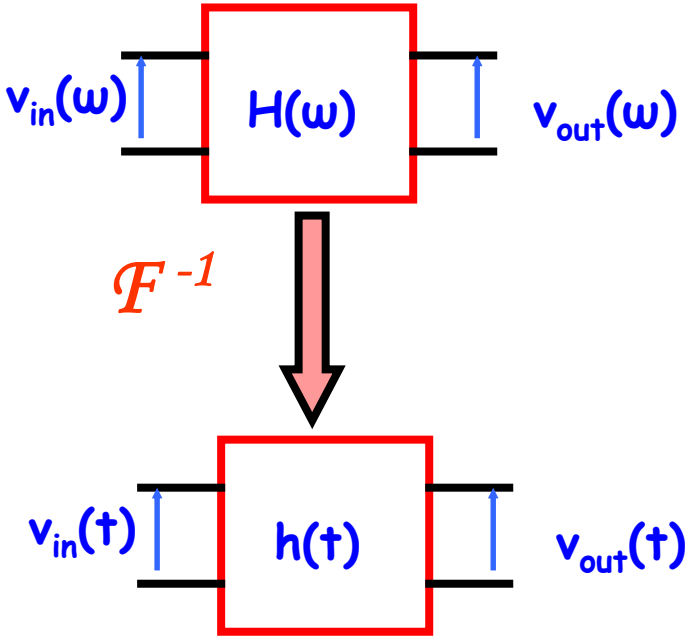


- **Ohms' law**
  - Z = R, 1/jωC, jωL
  - Note the sign convention



Frequency domain & time domain

- **Frequency domain :**
  - $V(\omega,t) = A \sin(\omega t + \varphi)$
    - Described by amplitude and phase (A, φ)
  - **Transfer function : $H(\omega)$** [or $H(s)$]
  - = The ratio of output signal to input signal in the frequency domain assuming linear electronics
  - $V_{out}(\omega) = H(\omega)\, V_{in}(\omega)$



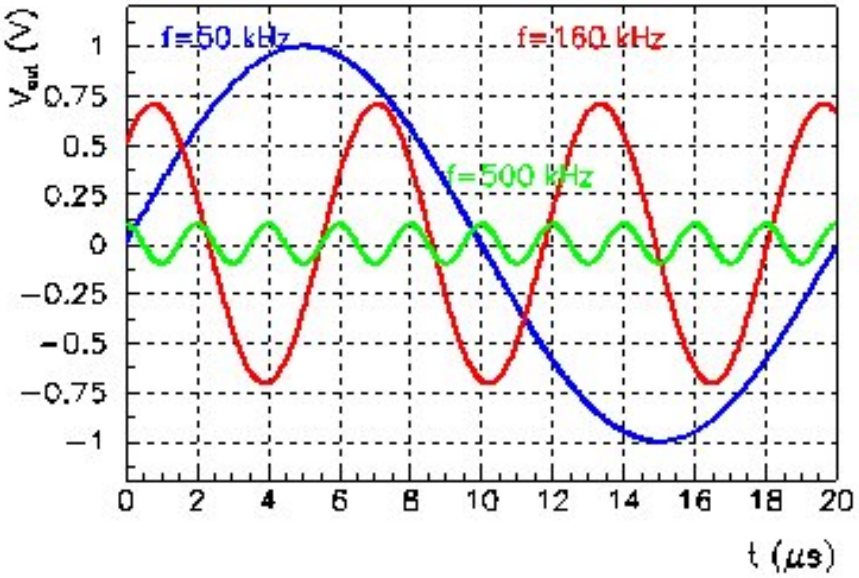
- **Time domain**
  - Impulse response : h(t)
  - = the output signal for an impulse (delta) input in the time domain
  - The output signal for any input signal $v_{in}(t)$ is obtained by convolution : «*» :
  - $V_{out}(t) = v_{in}(t) * h(t) = \int v_{in}(u) * h(t-u)\, du$

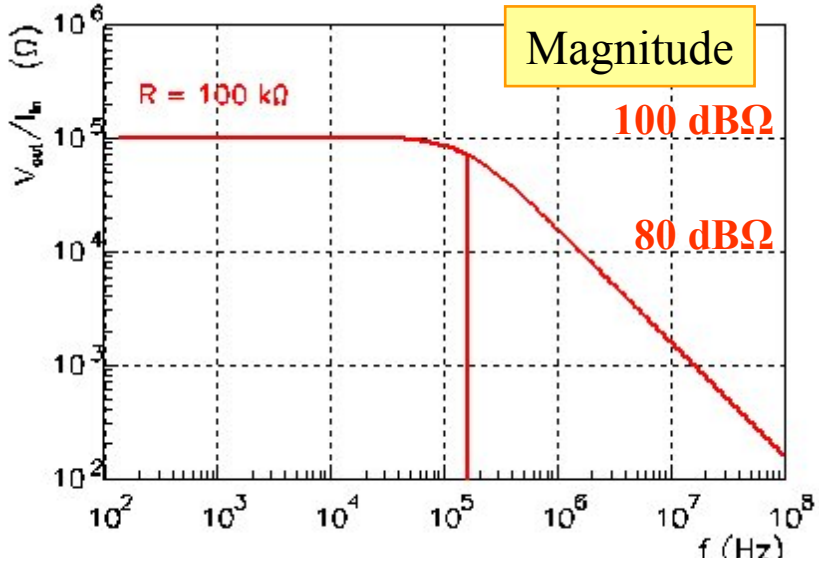
- **Correspondance through Fourier transforms**
  - $X(\omega) = \mathcal{F}\{x(t)\} = \int x(t) \exp(j\omega t) dt$
  - a few useful Fourier transforms in appendix

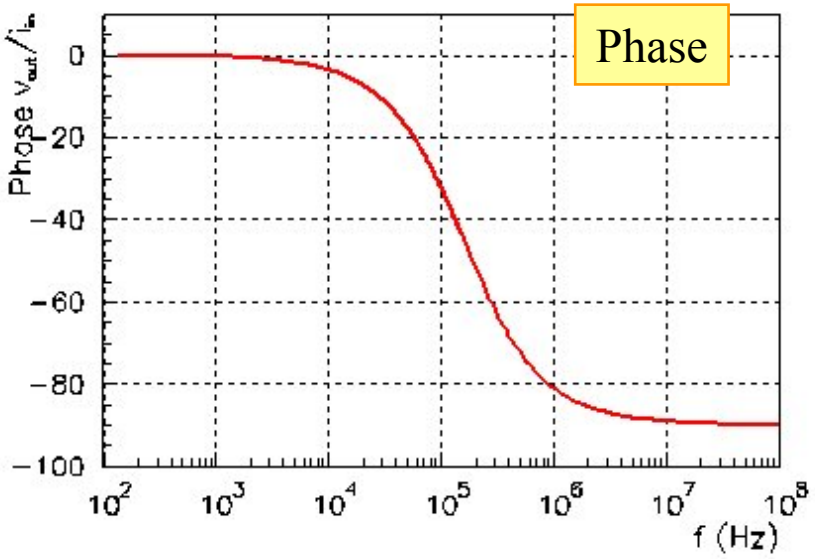
- $H(\omega) = 1 \rightarrow h(t) = \delta(t)$ (impulse)
- $H(\omega) = 1/j\omega \rightarrow h(t) = S(t)$ (step)
- $H(\omega) = 1/j\omega\,(1+j\omega T) \rightarrow h(t) = 1 - \exp(-t/T)$
- $H(\omega) = 1/(1+j\omega T) \rightarrow h(t) = \exp(-t/T)$
- $H(\omega) = 1/(1+j\omega T)^n \rightarrow h(t) = 1/n!\,(t/T)^{n-1} \exp(-t/T)$
- ...

Frequency response

- **Bode plot**
  - Magnitude (dB) = 20 log |H(jw)|
  - -3dB bandwidth : $f_{-3dB} = 1/2\pi RC$
    - $R=10^5\Omega$, C=10pF => f_{-3dB}=160 kHz
    - At f_{-3dB} the signal is attenuated by 3dB = $\sqrt{2}$, the phase is -45°
  - Above f_{-3dB} , gain rolls-off at -20dB/decade (or -6dB/octave)



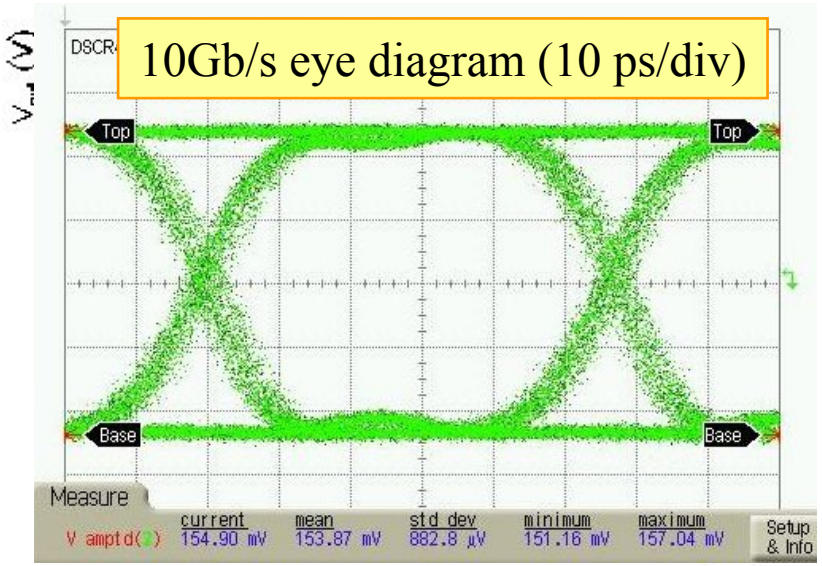


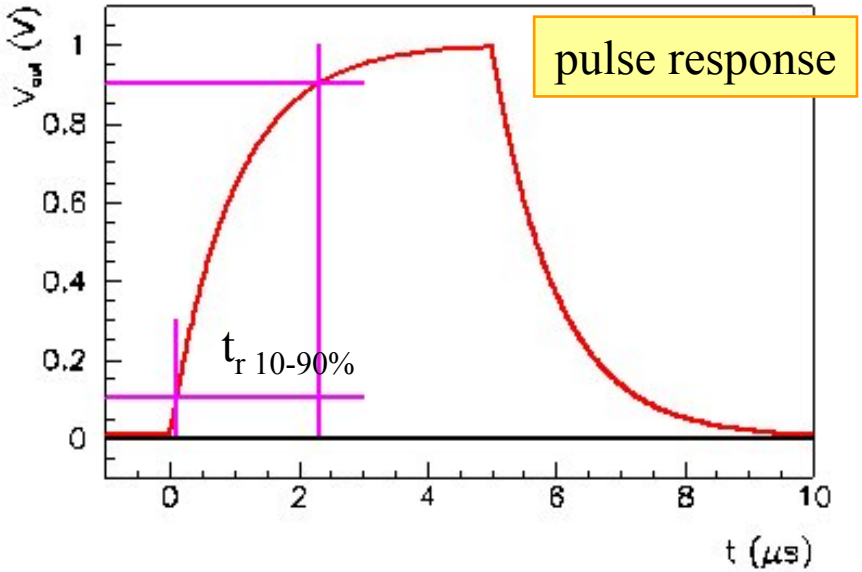


Time response

- **Impulse response**
  - h(t) = $\mathcal{F}^{-1}$ { R/(1+jωRC) }
    = R/ τ exp(-t/τ)
  - τ *(tau)* = RC = 1 μs : time constant

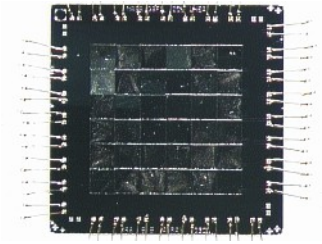
- **Step response : rising exponential**
  - H(t) = $\mathcal{F}^{-1}$ { 1/jω R/(1+jωRC) }
    = R [1 - exp(-t/ τ)]
  - Rise time : $t_{10\text{-}90\%}$ = 2.2 τ
  - « eye diagramm »





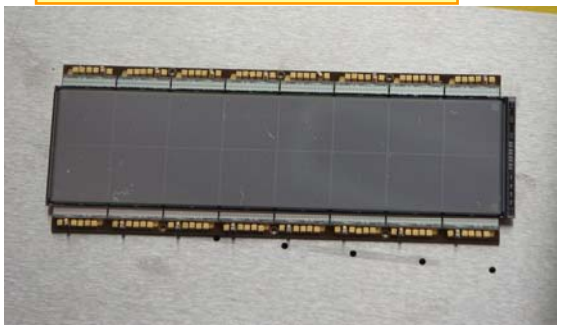
Detector(s)

- A large variety
- A similar modelization

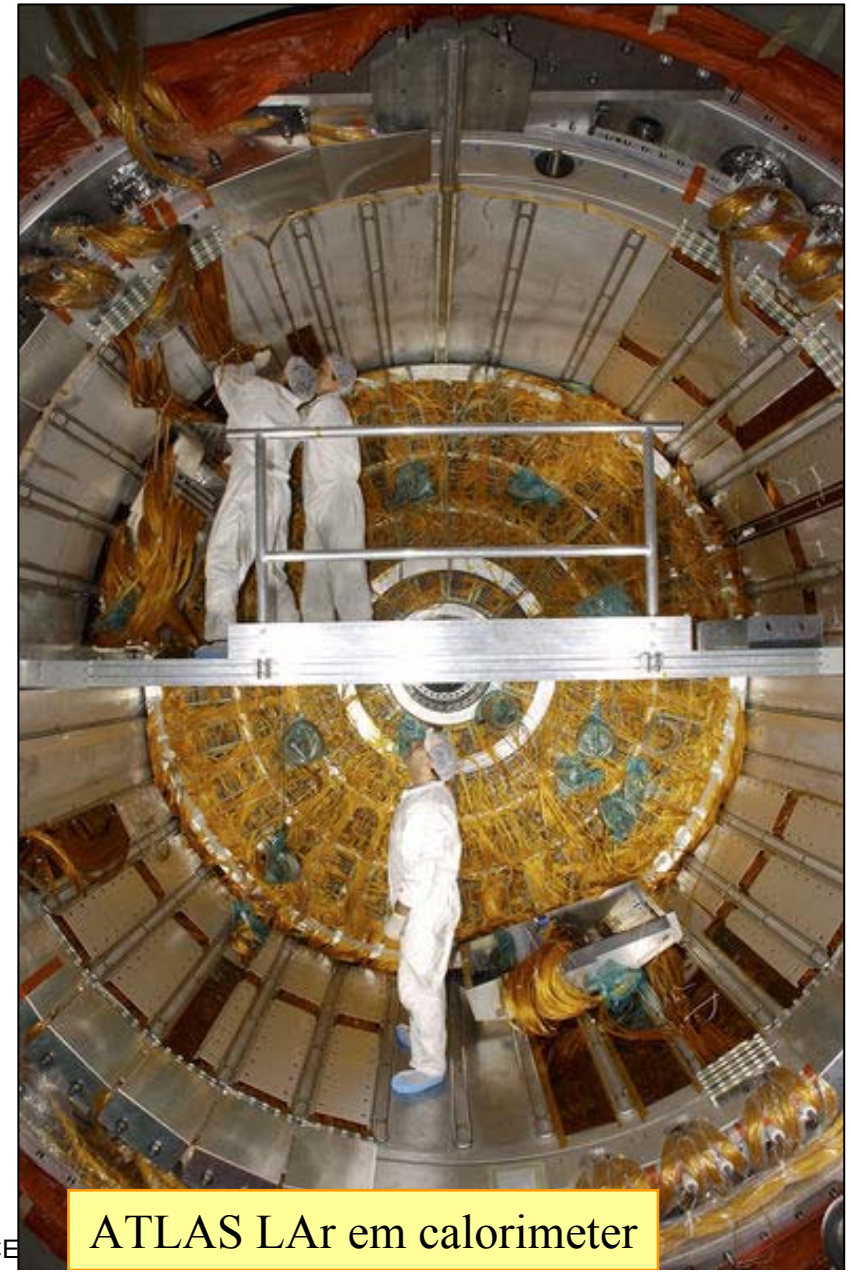


6x6 pixels,4x4 mm^2
HgTe absorbers, 65 mK
12 eV @ 6 keV

CMS Pixel module



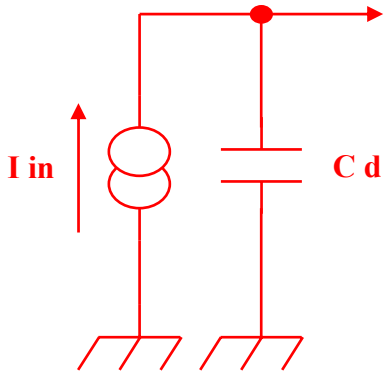
PMT for Antares



ATLAS LAr em calorimeter

Detector modelization

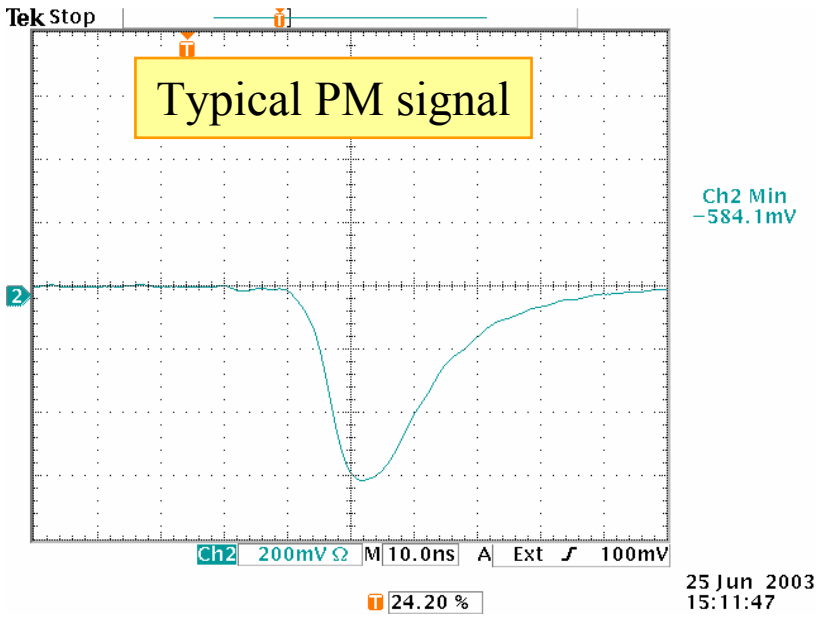
- **Detector = capacitance Cd**
  - Pixels : 0.1-10 pF
  - PMs : 3-30pF
  - Ionization chambers 10-1000 pF
  - Capa or transmission line?



Detector modelisation

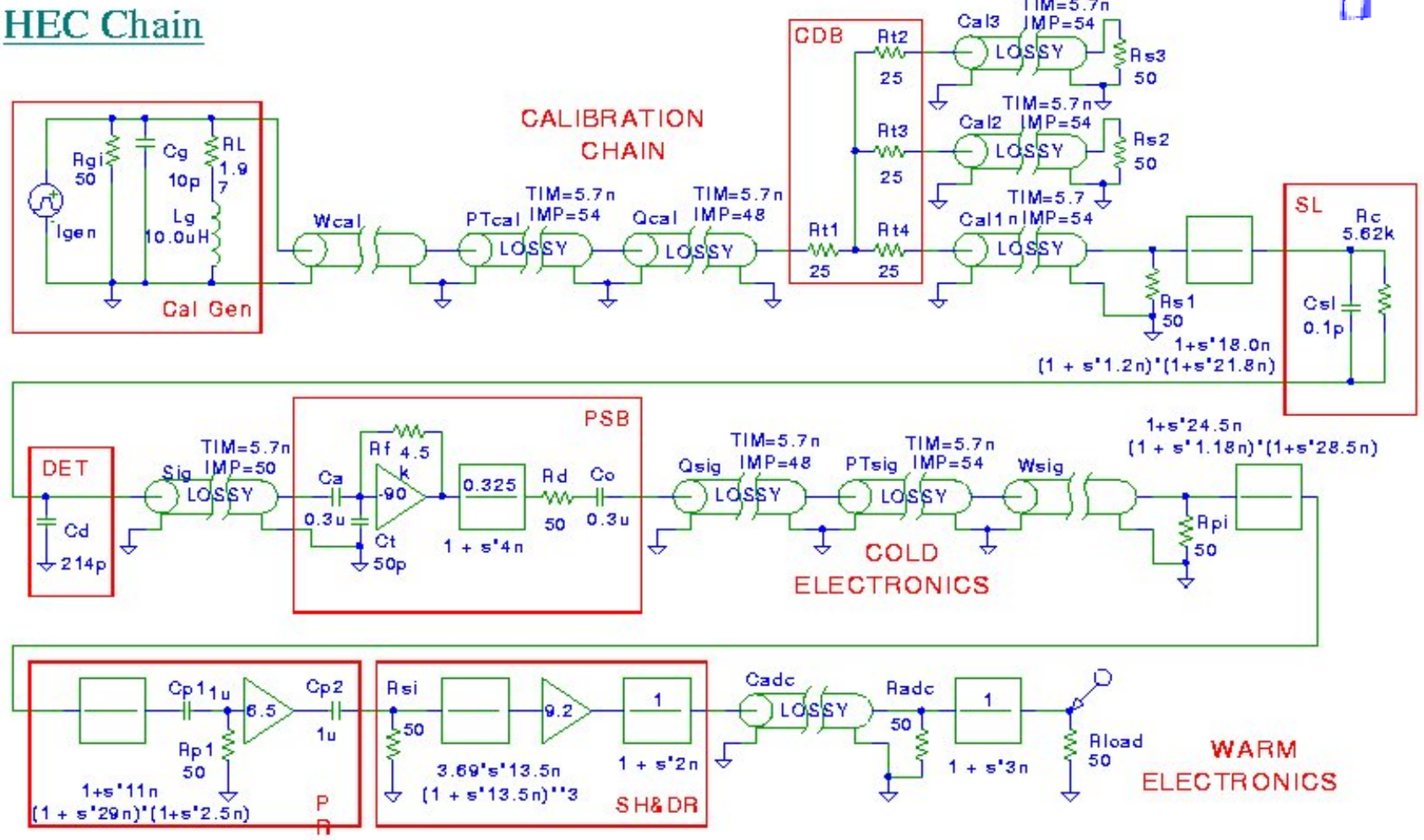
- **Signal : current source**
  - Pixels : ~100e-/µm
  - PMs : 1 photoelectron -> 10^5-10^7 e-
  - Modelized as an impulse (Dirac) : $i(t)=Q_0\delta(t)$

- **Missing :**
  - High Voltage bias
  - Connections, grounding
  - Neighbours
  - Calibration…



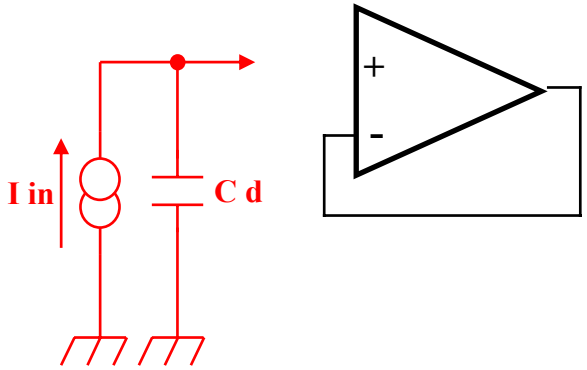
Sometimes a rather complex modelling…

- **Modelizing the ATLAS HEC calorimeter** [L. Kurchaninov LEB 2000]
  - Measure parameters for all element : more than thirty poles and zeros
  - Fit residuals within +/- 1%

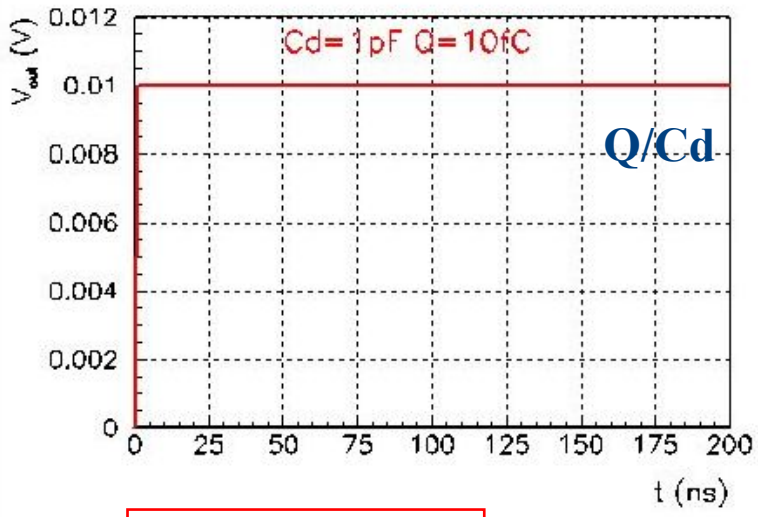


Reading the signal

- **Signal**
  - Signal = current source
  - Detector = capacitance C_d
  - Quantity to measure
    - Charge => integrator needed
    - Time => discriminator + TDC

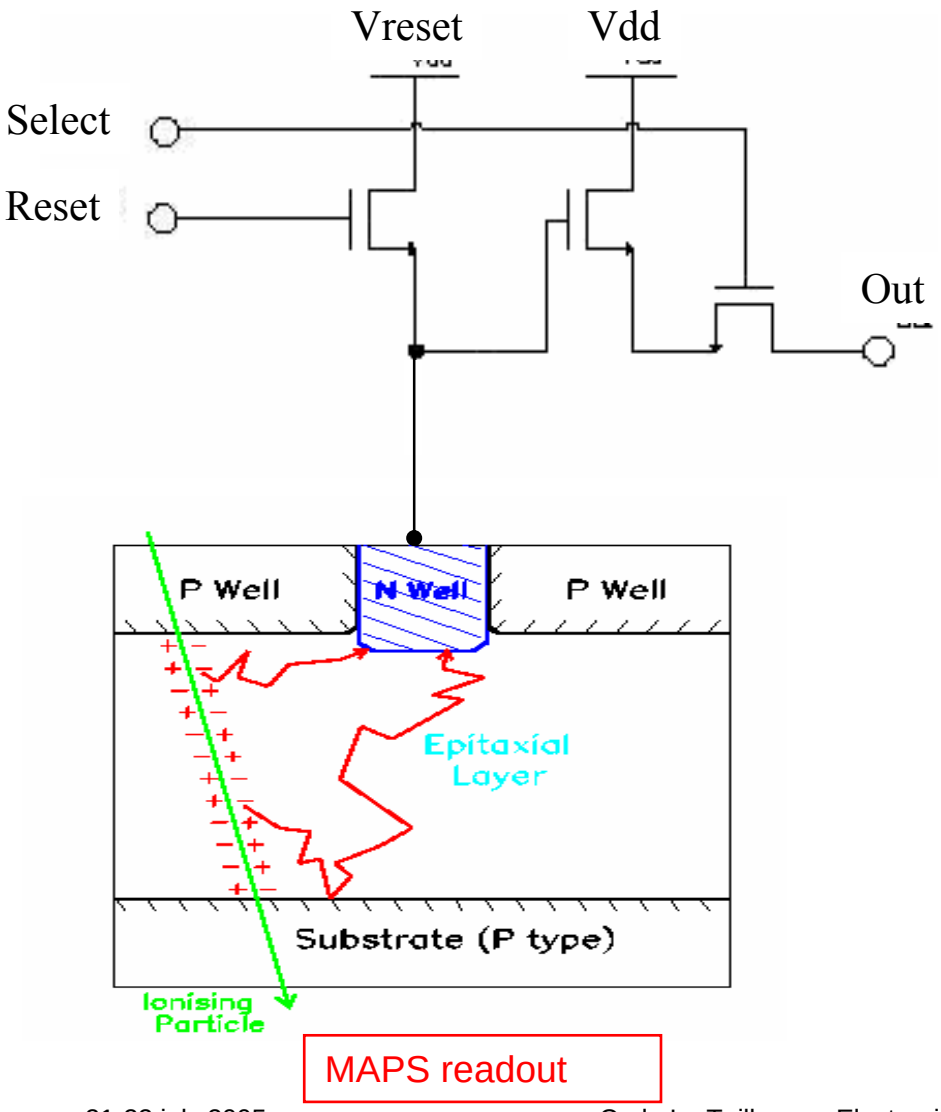


- **Integrating on Cd**
  - Simple : $V = Q/C_d$
  - « Gain » : $1/C_d$: 1 pF -> 1 mV/fC
  - Need a follower to buffer the voltage…
  - Input follower capacitance : Ca // Cd
  - Gain loss, possible non-linearities
  - crosstalk
  - Need to empty Cd…

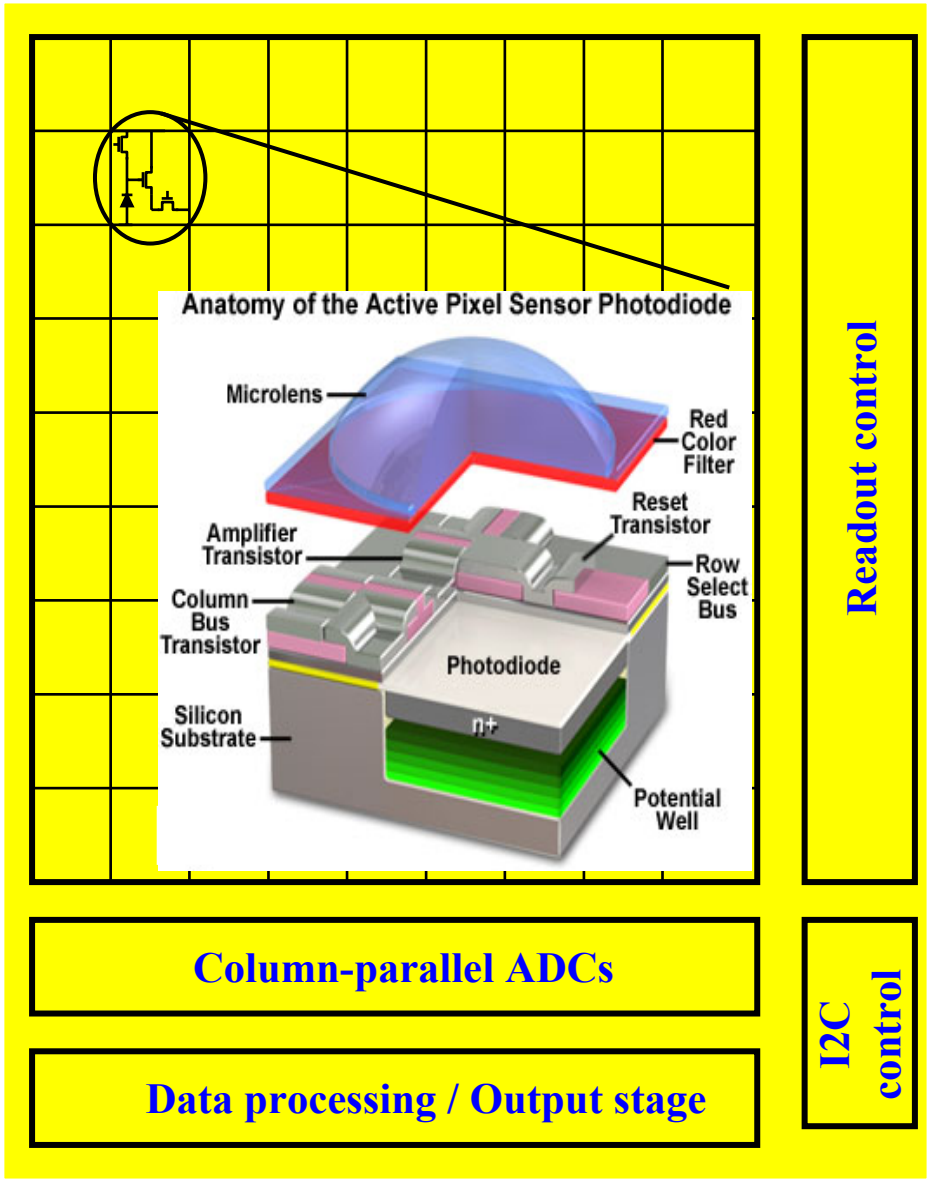


Impulse response

Monolithic active pixels



MAPS readout

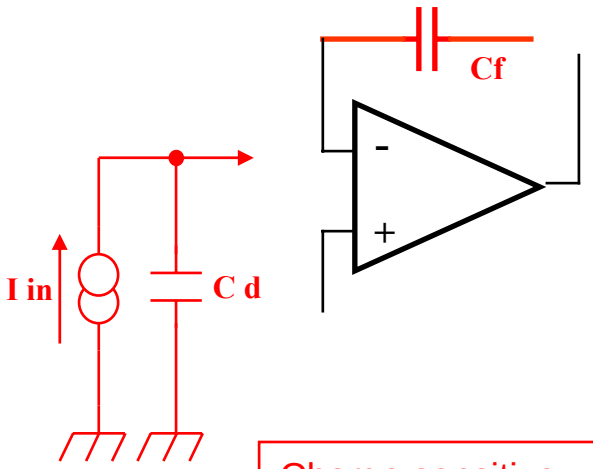


Ideal charge preamplifier

- **ideal opamp in transimpedance**
  - Shunt-shunt feedback
  - transimpedance : v_{out}/i_{in}
  - Vin-=0 =>$V_{out}(\omega)/i_{in}(\omega) = - Z_f = - 1/j\omega C_f$
  - Integrator : $v_{out}(t) = -1/C_f \int i_{in}(t)dt$

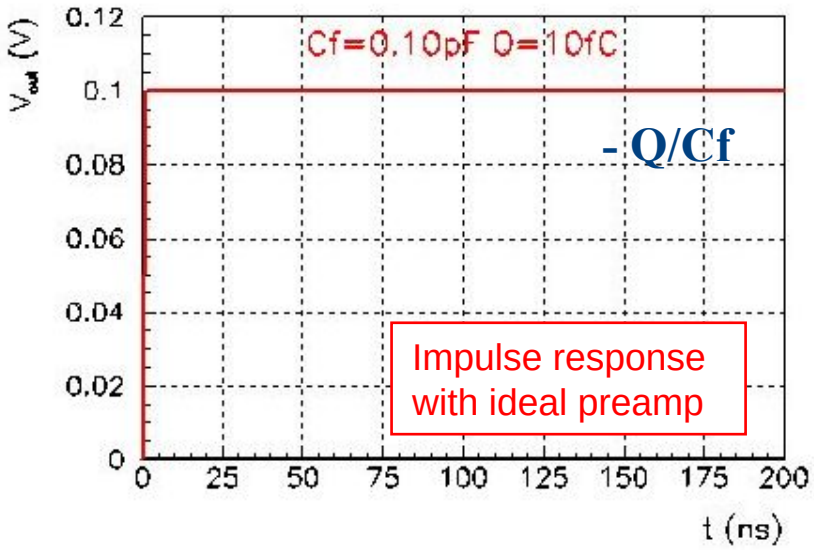
$$v_{out}(t) = - Q/C_f$$

  - « Gain » : $1/C_f$: 0.1 pF -> 10 mV/fC
  - C_f determined by maximum signal



Charge sensitive preamp

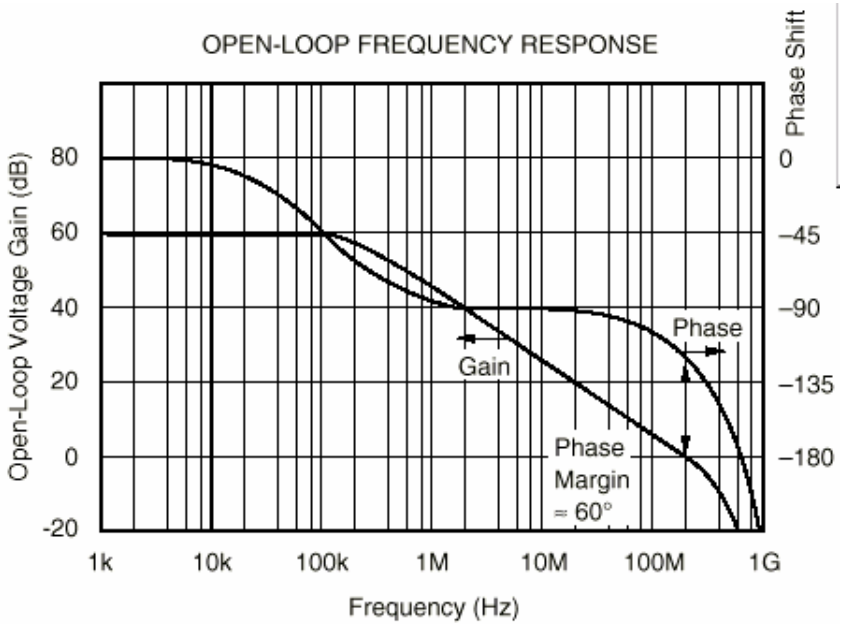
- **Integration on Cf**
  - Simple : V = - Q/C_f
  - Unsensitive to preamp capacitance C_{PA}
  - Turns a short signal into a long one
  - The front-end of 90% of particle physics detectors…
  - But always built with custom circuits…

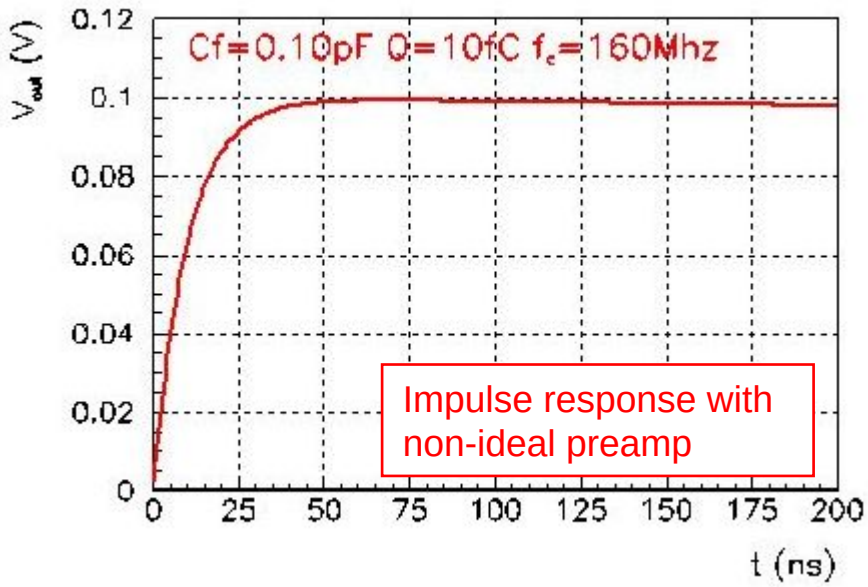


Impulse response with ideal preamp

Non-ideal charge preamplifier

- **Finite opamp gain**
  - $V_{out}(\omega)/i_{in}(\omega) = - Z_f / (1 + C_d / G_0 C_f)$
  - Small signal loss in $C_d / G_0 C_f \ll 1$ (ballistic deficit)
- **Finite opamp bandwidth**
  - First order open-loop gain
  - $G(\omega) = G_0/(1 + j\, \omega/\omega_0)$
    - G_0 : low frequency gain
    - $G_0\omega_0$: gain bandwidth product
- **Preamp risetime**
  - Due to gain variation with ω
  - Time constant : τ *(tau)* $= C_d / G_0\omega_0 C_f$
  - Rise-time : $t_{10\text{-}90\%} = 2.2\ \tau$
  - Rise-time optimised with $w_{C\ or}\ C_f$





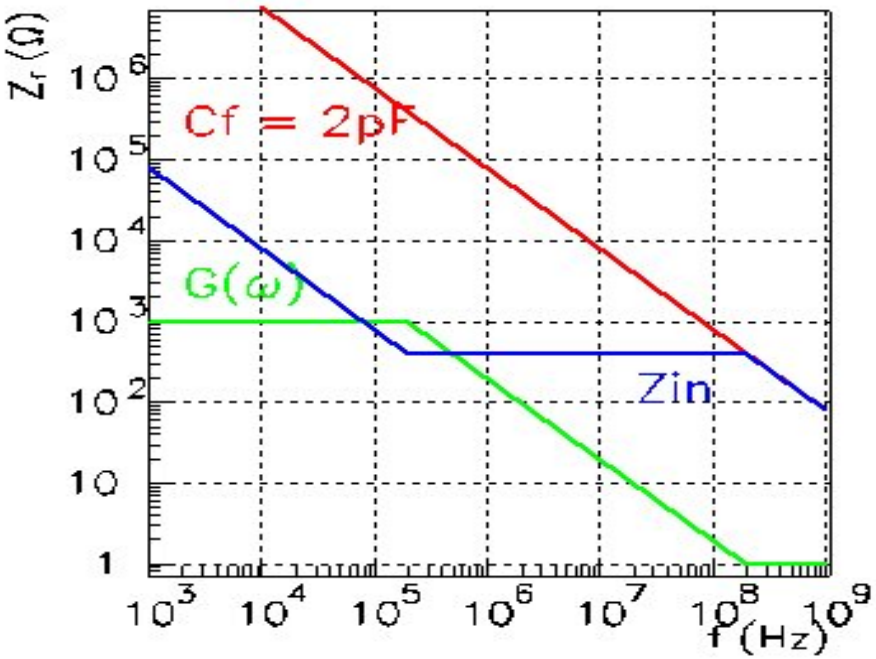
Charge preamp seen from the input

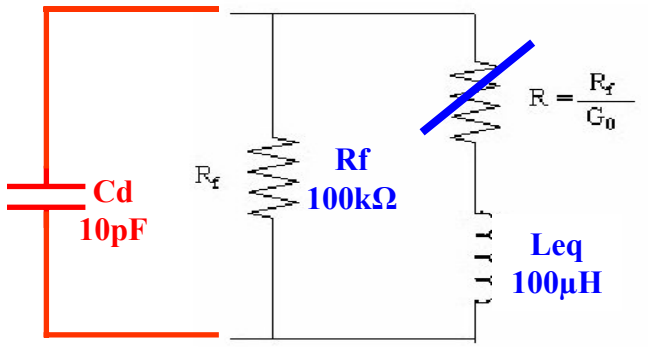
- **Input impedance with ideal opamp**
  - Zin = Zf / G+1
  - Zin->0 for ideal opmap
  - « Virtual ground » : Vin = 0
  - Minimizes sensitivity to detector impedance
  - Minimizes crostalk

- **Input impedance with real opamp**
  - Zin = $1/j\omega\, G_0 C_f + 1/ G_0 \omega_0 C_f$
  - Resistive term : Rin = $1/ G_0 \omega_0 C_f$
    - Exemple : $w_c = 10^9$ rad/s C_f= 0.1 pF => Rin 10 k
  - Determines the input time constant : $t = R_{eq} C_d$
  - Good stability= (…!)

- **Equivalent circuit :**

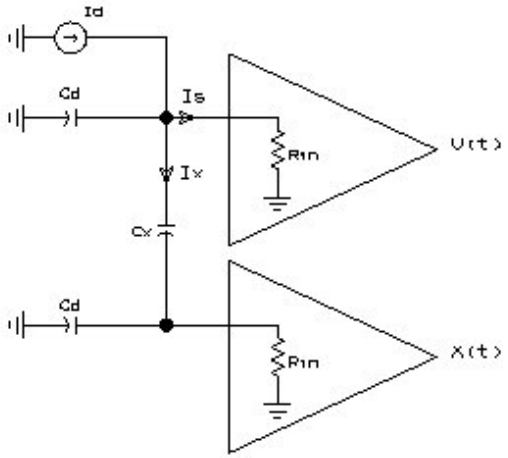
Input impedance or charge preamp



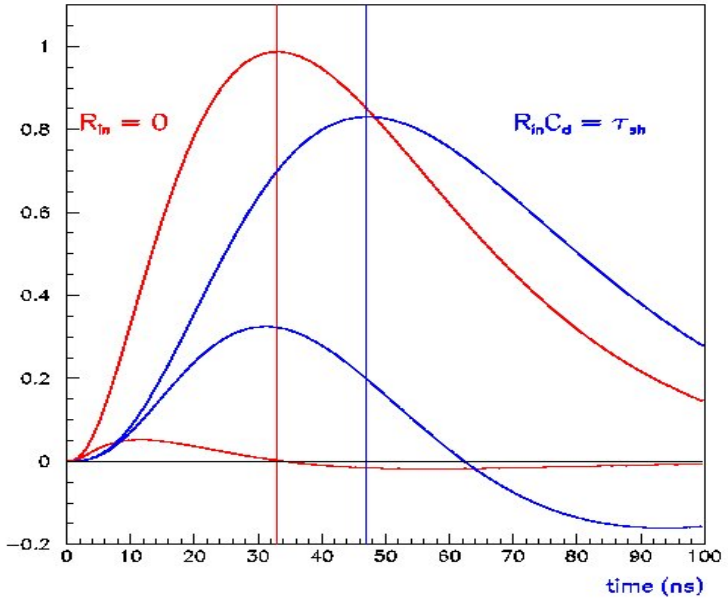


Crosstalk

- **Capacitive coupling between neighbours**
  - Crosstalk signal is differentiated and with same polarity
  - Small contribution at signal peak
  - Proportionnal to Cx/Cd and preamp input impedance
  - Slowed derivative if RinCd ~ tp => non-zero at peak

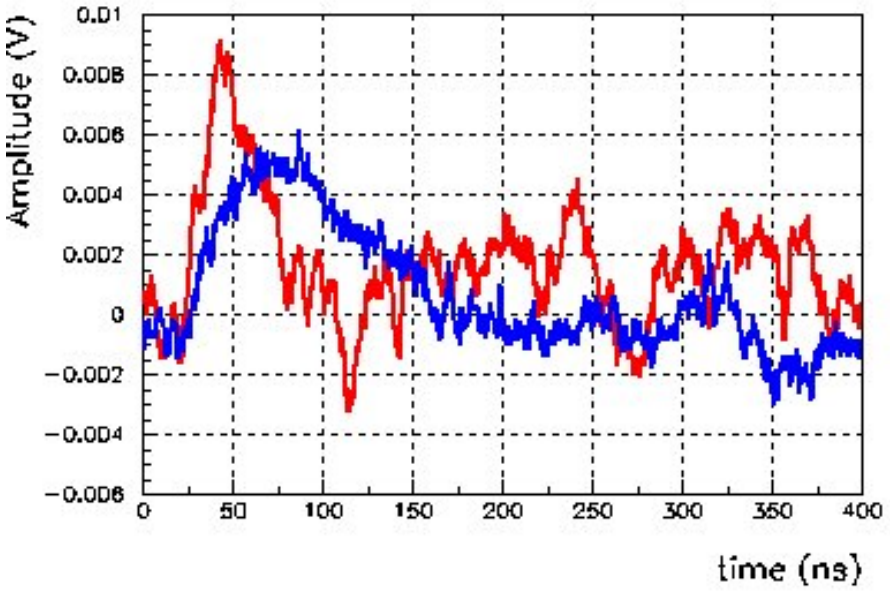


- **Inductive coupling**
  - Inductive common ground return
  - "Ground apertures" = inductance
  - Connectors : mutual inductance



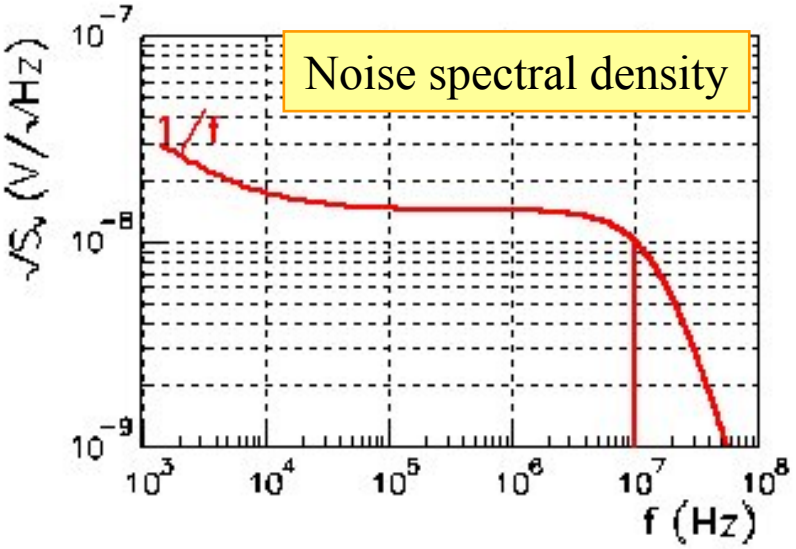
Electronics noise

- **Definition of Noise**
  - Random fluctuation superposed to interesting signal
  - Statistical treatment
- **Three types of noise**
  - Fundamental noise (Thermal noise, shot noise)
  - Excess noise (1/f …)
  - Parasitics -> EMC/EMI (pickup noise, ground loops…)

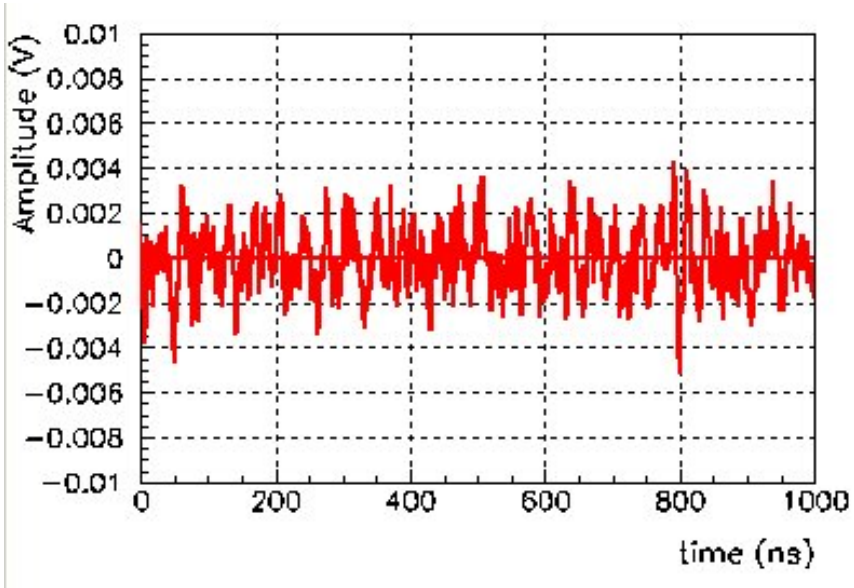


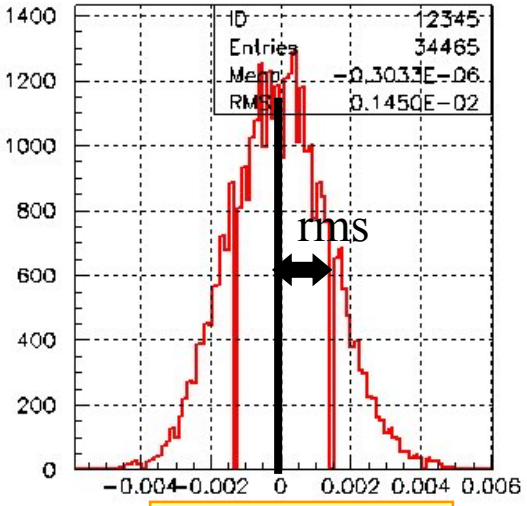
Electronics noise

- **Modelization**
  - Noise generators : e_n, i_n,
  - Noise spectral density of e_n & i_n : $S_v(f)$ & $S_i(f)$
  - $Sv(f) = | \mathcal{F}(e_n) |^2$ (V^2/Hz)



- ***Rms* noise Vn**
  - $V_n^2 = \int e_n^2(t)\, dt = \int Sv(f)\, df$
  - White noise (e_n) : $v_n = e_n \sqrt{\frac{1}{2}\pi f_{-3dB}}$





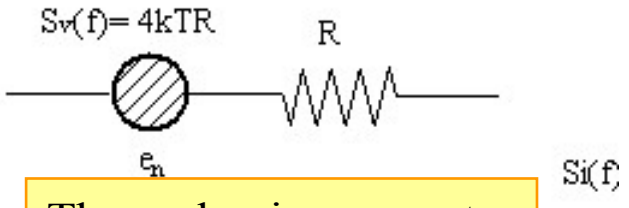
Rms noise vn

Calculating electronics noise

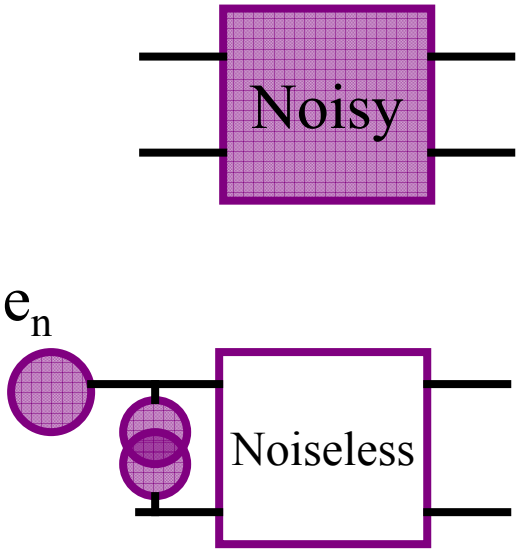
- **Fundamental noise**
  - Thermal noise (resistors) : Sv(f) = 4kTR
  - Shot noise (junctions) : Si(f) = 2qI

- **Noise referred to the input**
  - All noise generators can be referred to the input as 2 noise generators :
  - A voltage one e_n in series : series noise
  - A current one i_n in parallel : parallel noise
  - Two generators : no more, no less… why ?
  - To take into account the Source impedance

- **Golden rule**
  - Always calculate the signal before the noise what counts is the signal to noise ratio
  - Don't forget noise generators are V^2/Hz => calculations in module square
  - Practical exercice next slide



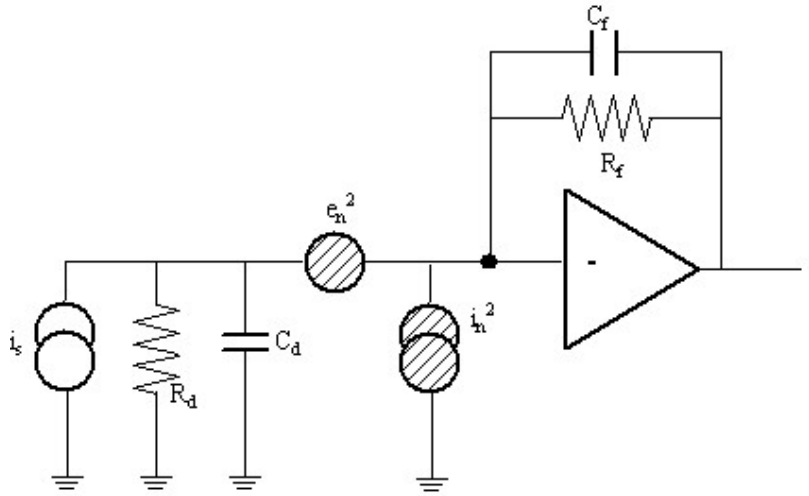
Thermal noise generator



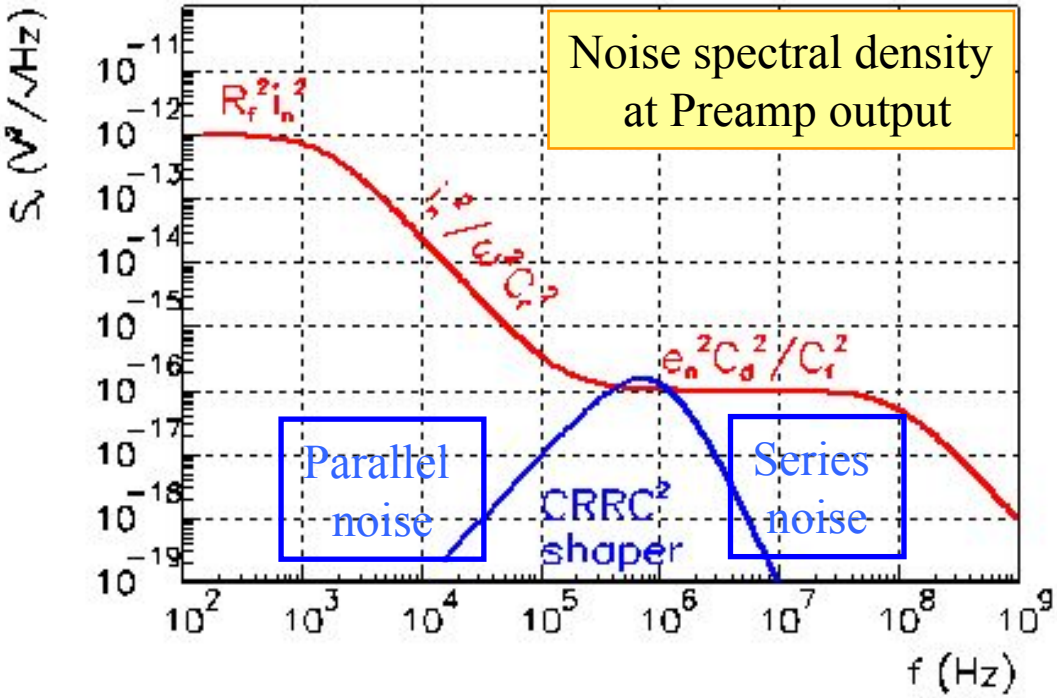
Noise generators referred to the input

Noise in charge pre-amplifiers

- **2 noise generators at the input**
  - Parallel noise : (i_n^2) (leakage currents)
  - Series noise : (e_n^2) (preamp)



- **Output noise spectral density :**
  - $Sv(\omega) = (i_n^2 + e_n^2/|Z_d|^2) / \omega^2 C_f^2$
    $= i_n^2 / \omega^2 C_f^2 + e_n^2 C_d^2 / C_f^2$
  - Parallel noise in $1/\omega^2$
  - Series noise is flat, with a « noise gain » of C_d/C_f

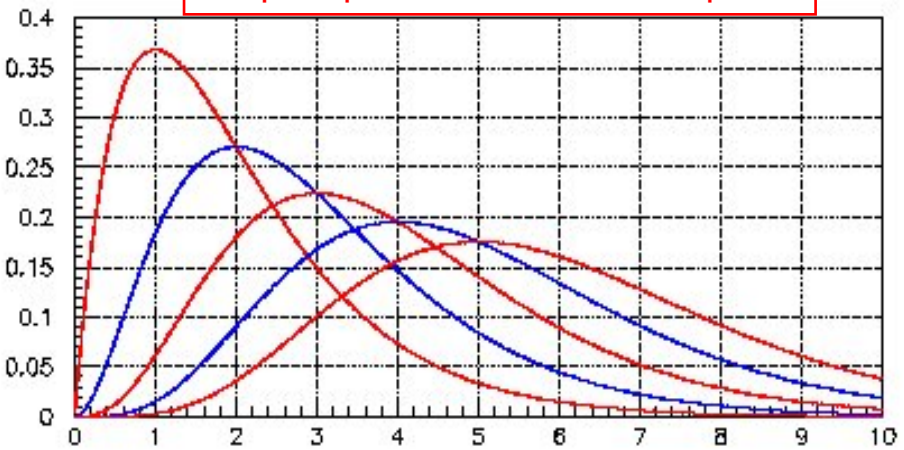


- ***rms* noise V_n**
  - $V_n^2 = \int Sv(\omega)\, d\omega/2\pi \rightarrow \infty$ (!)
  - Benefit of shaping…

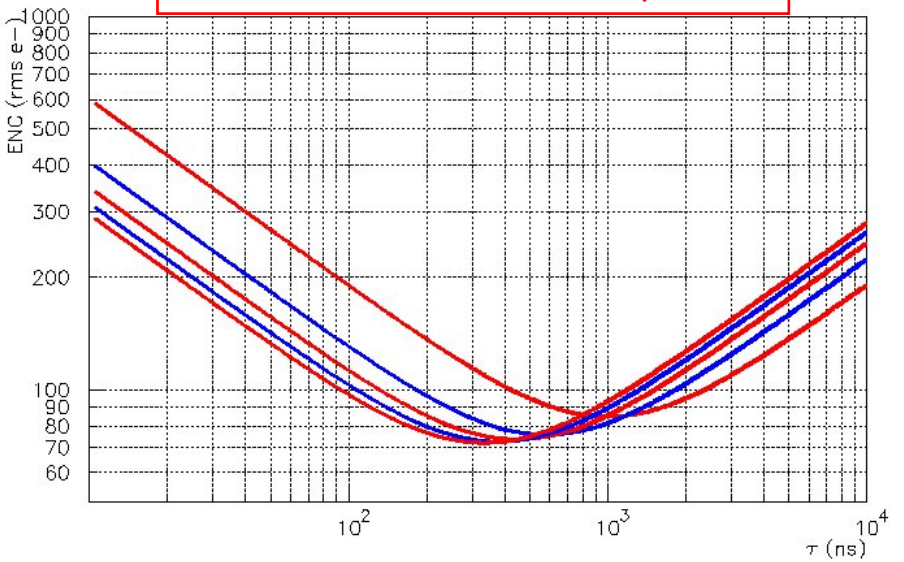
Equivalent Noise Charge (ENC) after CRRC^n

- **Noise reduction by optimising useful bandwidth**
  - Low-pass filters (**RC^n**) to cut-off high frequency noise
  - High-pass filter (**CR**) to cut-off parallel noise
  - -> pass-band filter CRRC^n
- **Equivalent Noise Charge : ENC**
  - Noise referred to the input in electrons
  - ENC = Ia(n) $e_n C_t/\sqrt{\tau} \oplus$ Ib(n) $i_n * \sqrt{\tau}$
  - Series noise in $1/\sqrt{\tau}$
  - Paralle noise in $\sqrt{\tau}$
  - 1/f noise independant of τ
  - Optimum shaping time $\tau_{opt} = \tau_c/\sqrt{2n-1}$
- **Peaking time tp (5-100%)**
  - ENC(**tp**) independent of n
- **Complex shapers are obsolete :**
  - Power of digital filtering
  - Analog filter = CRRC ou CRRC^2

Step response of CR RCn shapers



ENC vs tau for CR RCn shapers



Equivalent Noise Charge (ENC) after CRRC^n

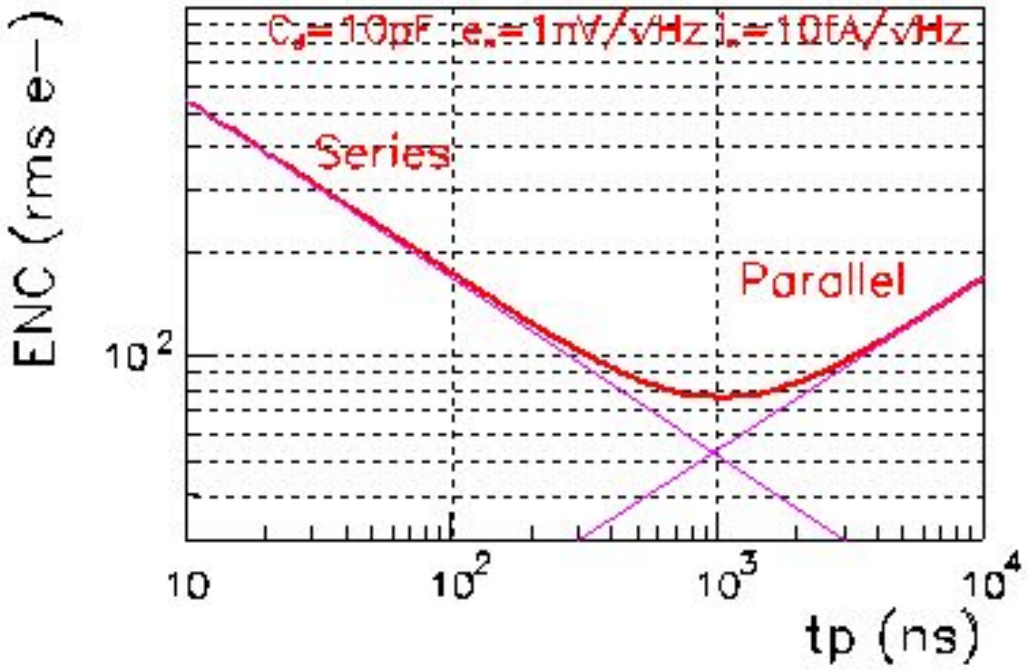
- **A useful formula** : ENC (e- rms) after a CRRC^2 shaper :

$$ENC = 174\ e_n C_{tot}/\sqrt{t_p}\ (\delta) \oplus 166\ i_n \sqrt{t_p}\ (\delta)$$

  - e_n in nV/ √Hz, i_n in pA/ √Hz are the preamp noise spectral densities
  - C_{tot} (in pF) is dominated by the detector (C_d) + input preamp capacitance (C_{PA})
  - t_p (in ns) is the shaper peaking time (5-100%)

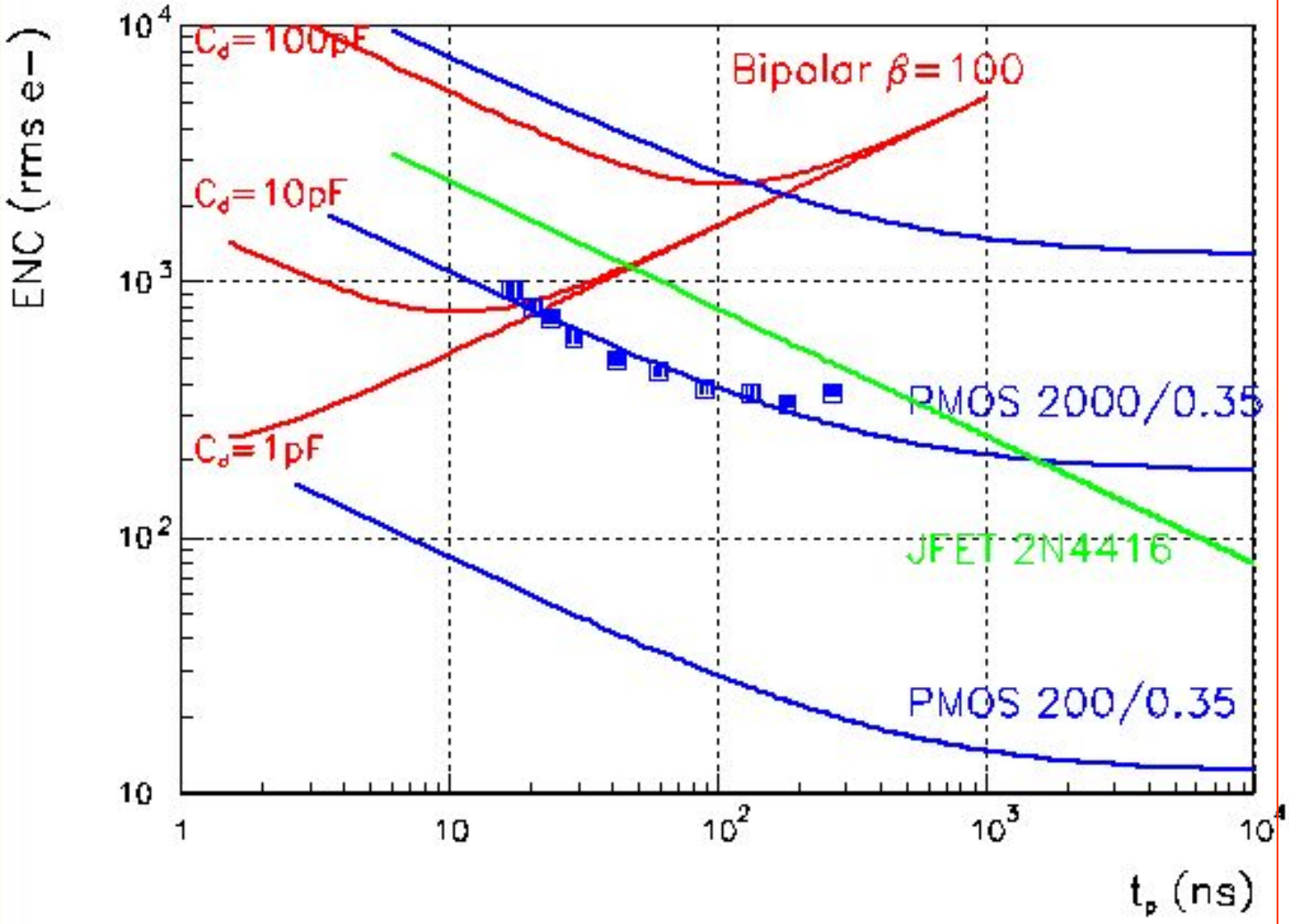
- **Noise minimization**
  - Minimize source capacitance
  - Operate at optimum shaping time
  - Preamp series noise (en) best with high trans-conductance (g_m) in input transistor

    => large current, optimal size



ENC for various technologies

- **ENC for Cd=1, 10 and 100 pF at I_D = 500 uA**
  - MOS transistors best between 20 ns – 2 μs

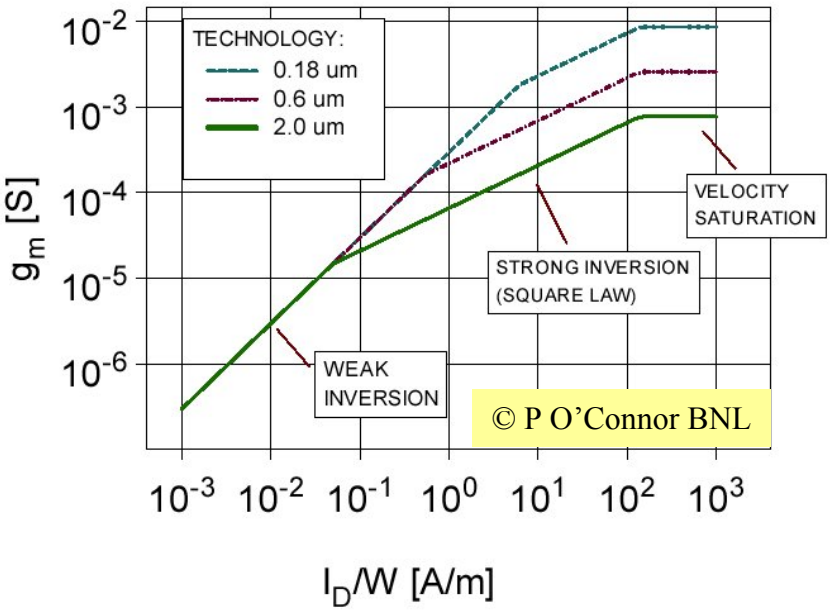


- **Parameters**
- Bipolar :
  - g_m = 20 mA/V
  - $R_{BB'}$=25 Ω
  - e_n= 1 nV/√Hz
  - I_B=5uA
  - i_n = 1 pA/√Hz
  - C_{PA}=100fF
- **PMOS 2000/0.35**
  - g_m = 10 mA/V
  - e_n = 1.4 nV/√Hz
  - C_{PA} = 5 pF
  - 1/f :

MOS input transistor sizing

- **Capacitive matching : strong inversion**
  - g_m proportionnal to $W/L \sqrt{I_D}$
  - C_{GS} proportionnal to W*L
  - ENC propotionnal to $(Cdet+C_{GS})/ \sqrt{gm}$
  - Optimum W/L : C_{GS} = 1/3 Cdet
  - Large transistors are easily in moderate or weak inversion at small current

- **Optimum size in weak inversion**
  - g_m proportionnal to I_D (indep of W,L)
  - ENC minimal for C_{GS} minimal, provided the transistor remains in weak inversion

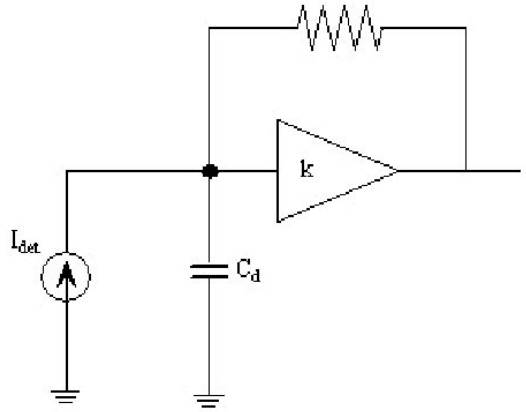


Current preamplifiers :

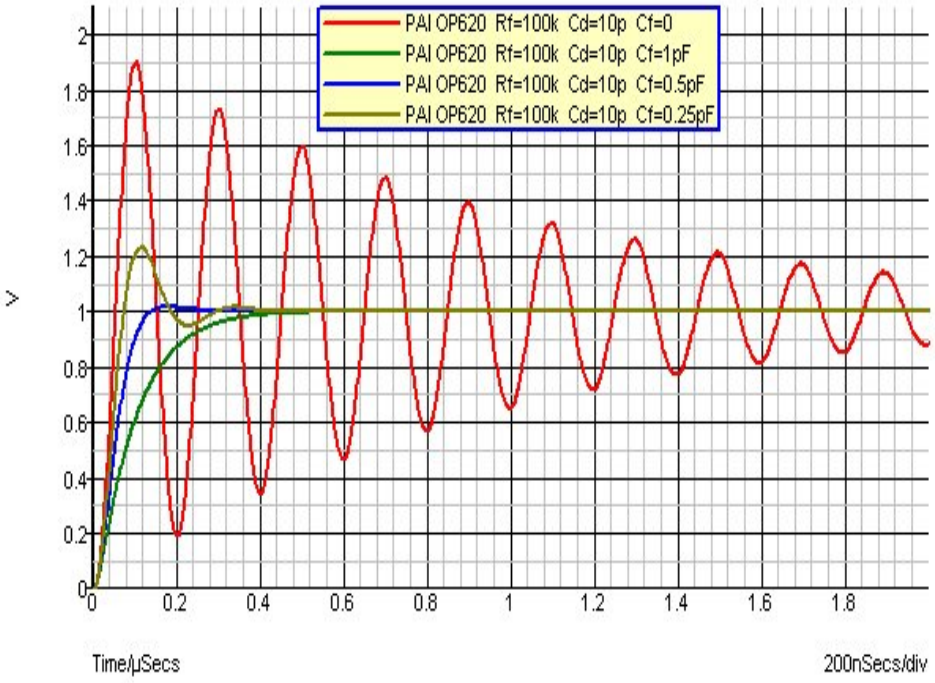
- **Transimpedance configuration**
  - $V_{out}(\omega)/i_{in}(\omega) = - R_f / (1+Z_f/GZ_d)$
  - Gain = R_f
  - High counting rate
  - Typically optical link receivers

- **Easily oscillatory**
  - Unstable with capacitive detector
  - Inductive input impedance

    $L_{eq} = R_f / \omega_C$
  - Resonance at : $f_{res} = 1/2\pi \sqrt{L_{eq}C_d}$
  - Quality factor : $Q = R / \sqrt{L_{eq}/C_d}$
    - $Q > 1/2$ -> ringing
  - Damping with capacitance C_f
    - $C_f = 2\sqrt{(C_d/R_f\, G_0\omega_0)}$
    - Easier with fast amplifiers
    -

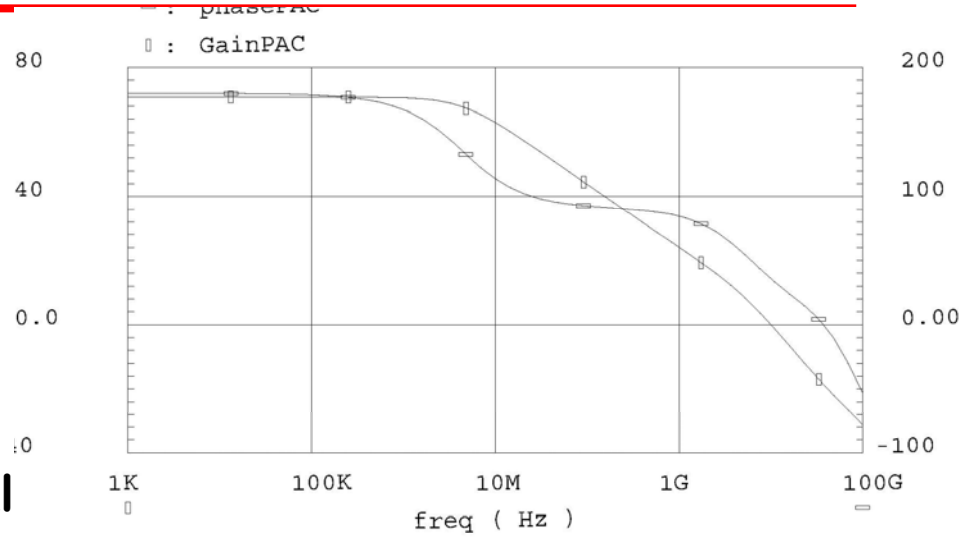


Current sensitive preamp



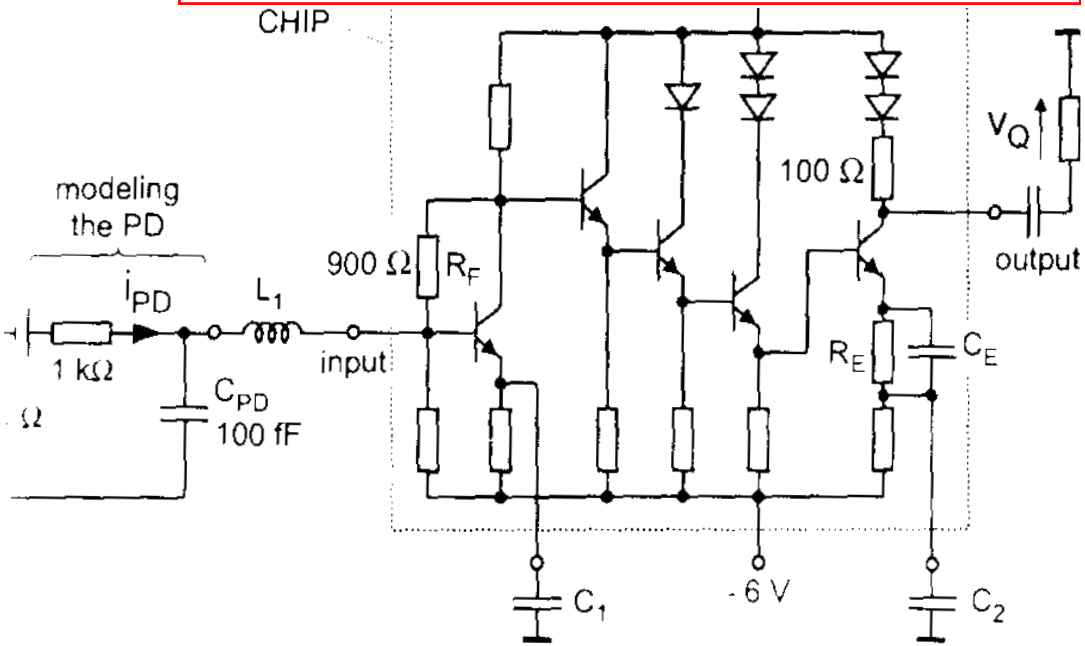
High speed transimpedance amplifier

- **Fast transimpedance amplifiers**
  - Rf= 25k Cf=10fF
  - SiGe process
  - 15 GHz gain-bandwidth product



Open loop frequency response of SiGe amplifier

- **40 Gb/s transimpedance for optical**
  - Simple architecture (CE + CC)
  - SiGe bipolar transistors
  - CC outside feedback loop
  - « pole splitting »



Course 2 : Front-end electronics
Example of design

CERN Summer school 2005

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LABORATOIRE DE L'ACCÉLÉRATEUR LINÉAIRE

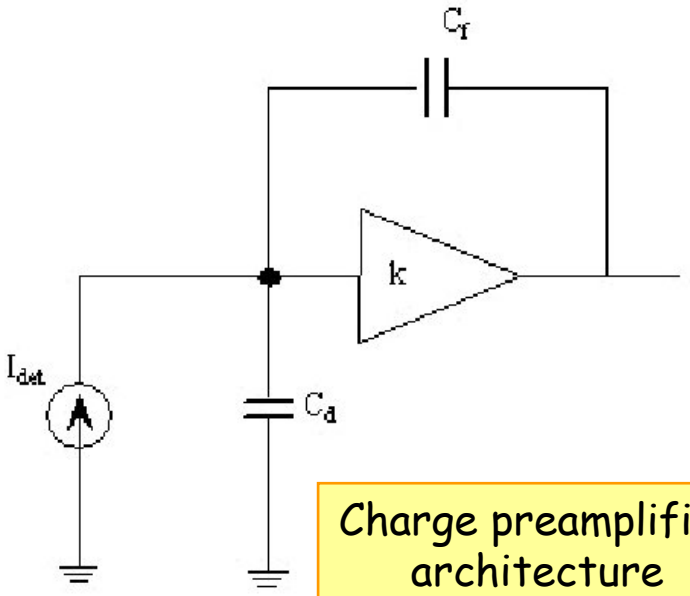
CENTRE NATIONAL DE LA RECHERCHE SCIENTIFIQUE

Summary of lecture 1

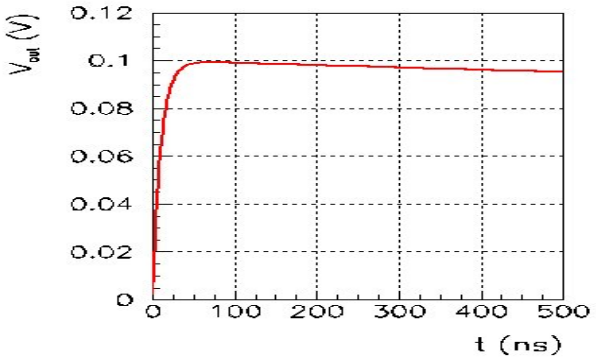
- **Ohm's law enough to do electronics**
  - Without forgetting Z complex…
  - The science of Electronics engineering…
- **Current sensitive preamplifiers (PAI)**
- **Charge sensitive preamplifiers (PAC)**
  - Output proportionnal to the incoming charge

$$v_{out}(t) = - Q/C_f$$

  - « Gain » : $1/C_f$; C_f = 1 pF -> 1 mV/fC
  - Transforms a short pulse into a long one
  - Low input impedance -> current sensitive
  - Virtual resistance R_{in}-> stable with capacitive detector
  - The front-end of 90% of particle physics detectors…
  - But always built with custom circuits…

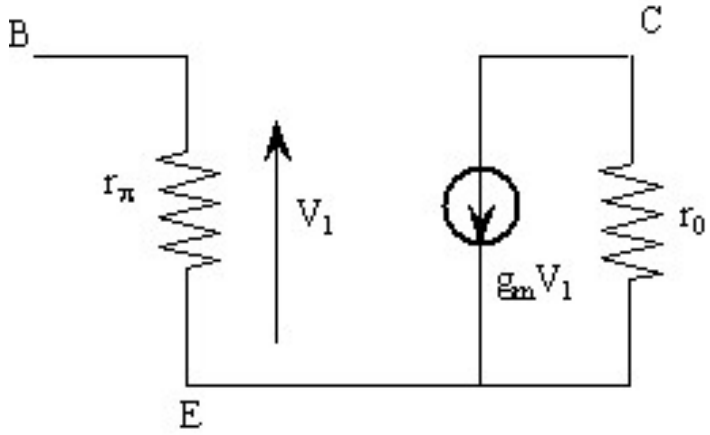


Charge preamplifier architecture



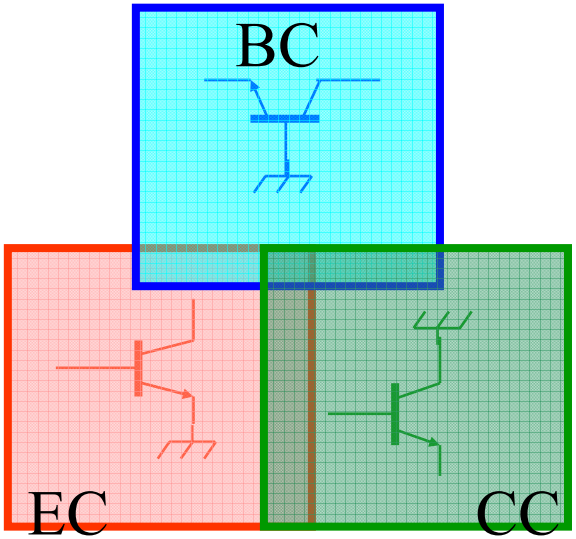
Design in micro-electronics

- performant design is at transistor level
- Simples models
  - Hybrid π model
  - Similar for bipolar and MOS
  - Essential for desgin



Low frequency hybrid model of bipolar

- Three basic bricks
  - Common emitter (CE) = V to I (transconductance)
  - Common collector (CC) = V to V (voltage buffer)
  - Common base (BC) = I to I (current conveyor)

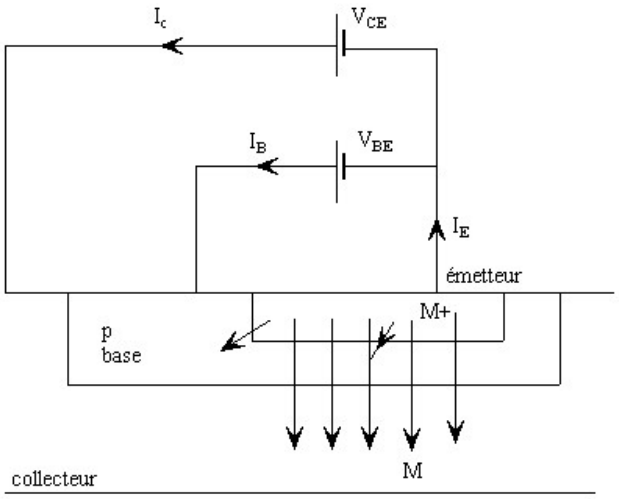


- Numerous « composites »
  - Darlington, Paraphase, Cascode, Mirrors…

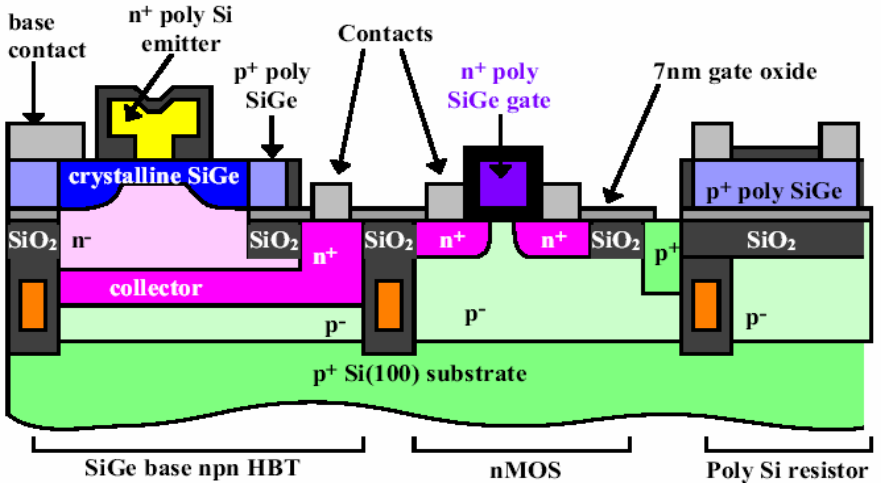
The *Art* of electronics design

Components : bipolar transistors (1)

- **Principle of operation :**
  - Forward bias of base emitter junction injects carriers which are swept in the collector due to the high collector-base electric field
  - collector current (I_C) controlled by base-emitter voltage (V_{BE})
  - Transconductance device : $g_m = \partial I_C / \partial V_{BE}$



First transistor (1949)
(Brattain-Bardeen Nobel 56)



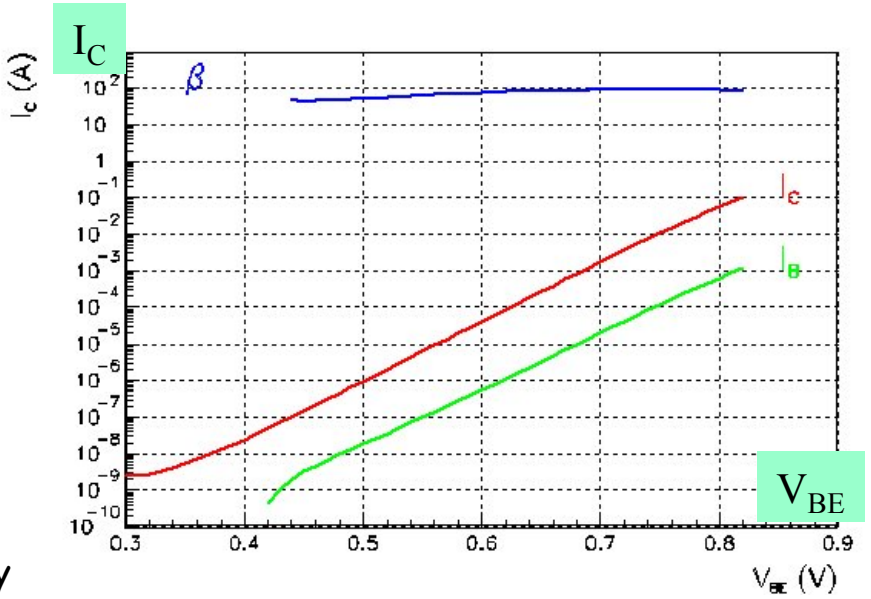
SiGe Bipolar in 0.35µm monolithic process

Components : bipolar transistors (2)

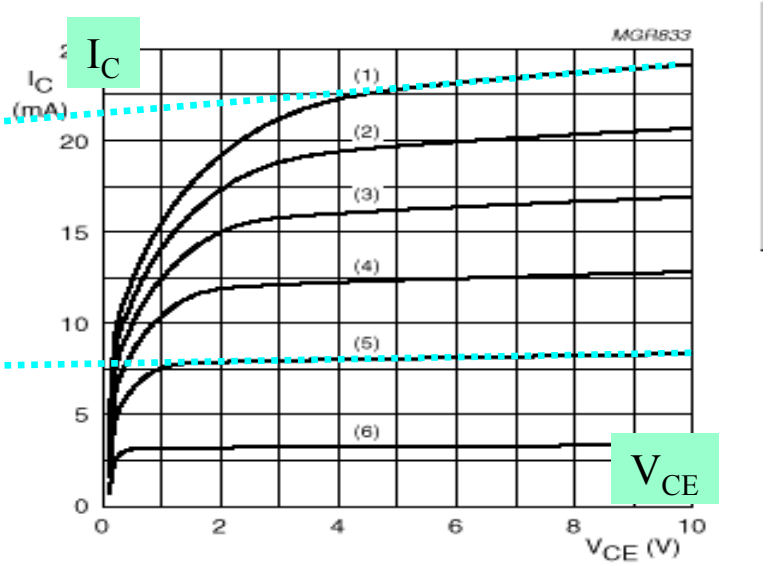
- **State equation :**

$$I_C = I_S \exp(V_{BE}/U_T)$$

  - $U_T = kT/q$ = 26 mV : thermal potential
  - Is = 10^{-16}-10^{-14} A : technological param.
- Very wide validity range : nA -> mA
- small input (base) current I_B
- $I_B = I_C/\beta_0$ β_0 >>1 is the current *gain* : a very misleading term !

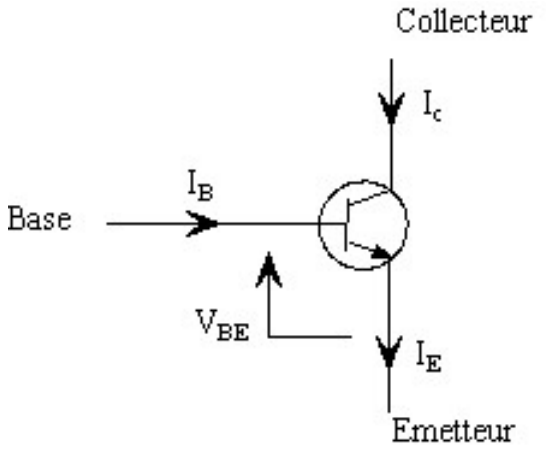


- **Early effect**
  - Very small dependance of I_C with collector voltage (V_{CE})
  - $I_C(V_{CE})$ are straight lines which cross at the same « Early » voltage -V_E (20-200V)



Small signal model

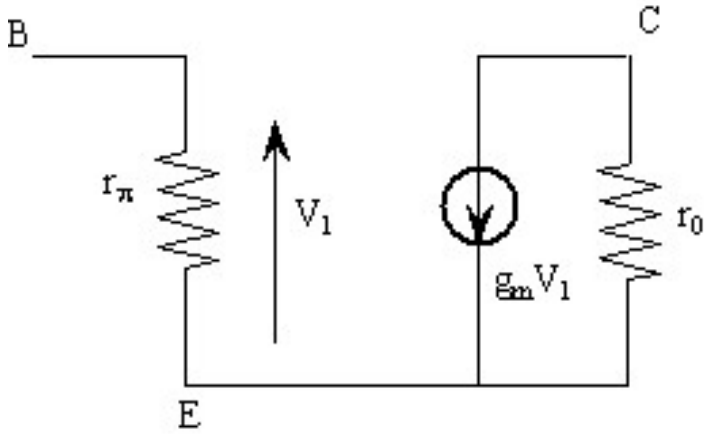
- **Equivalent circuit around bias point**
  - Signal = small variation around DC operating point (« bias point »)
  - => Linearisation : signal $v_{in} << V_{BE}$
  - $V_{BE} \rightarrow V_{BE} + v_{in} \Rightarrow I_C = I_C (1 + v_{in}/U_T + ...)$
  - Tranconductance : $\mathbf{g_m} = \partial I_C / \partial V_{BE} = I_C/U_T$
    - g_m depends only on bias current I_C and $U_T = kT/q$
    - *Ex : I_C = 1 mA => g_m = 1mA/26mV = 40 mA/V*



Schematic drawing of NPN transistor

- **Input impedance = r_π**
  - Base current => Rin = $r_\pi = \partial V_{BE} / \partial I_B = \beta_0 / g_m$
  - Relatively large : r_π = 1-100 kΩ
    - *Ex : I_C = 1 mA ; β_0=100 => r_π = 2.6 kΩ*

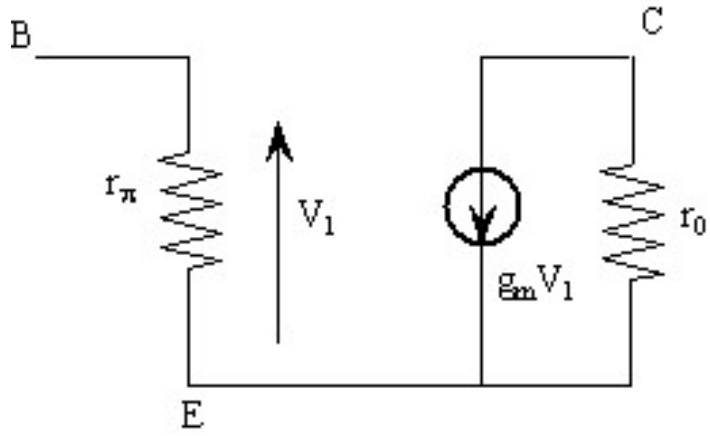
- **Output impedance : r_0**
  - Early effect : Rout = $r_0 = \partial V_{CE} / \partial I_C = V_E/I_C$
    - V_E is the Early voltage = 10-100 V
  - Large value : 10k-10MΩ
    - *Ex : Ic=1 mA ; V_E=100V => r_0 = 100 kΩ*



Low frequency hybrid model of bipolar

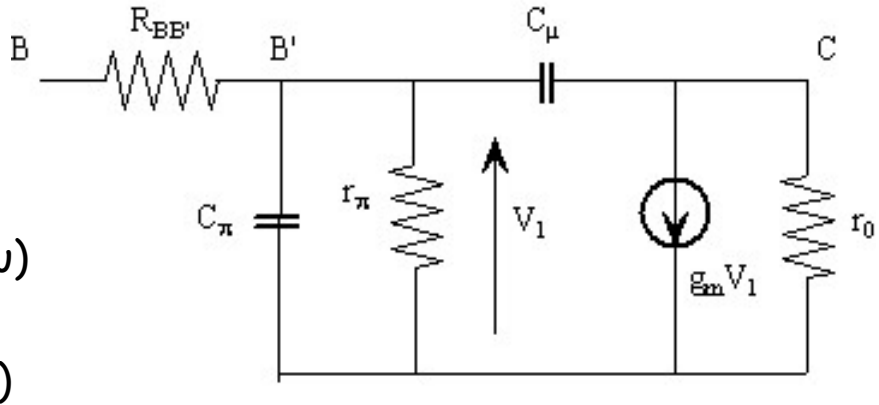
Hybrid π model

- **Simple hybrid model :**
  - Voltage controlled current source $g_m v_{BE}$
  - Transconductance $g_m = I_C/U_T$
  - Large input resistance $r_\pi = \beta_0 / g_m$
  - Large output resistance $r_0 = V_A/I_C$



Low frequency hybrid model of bipolar

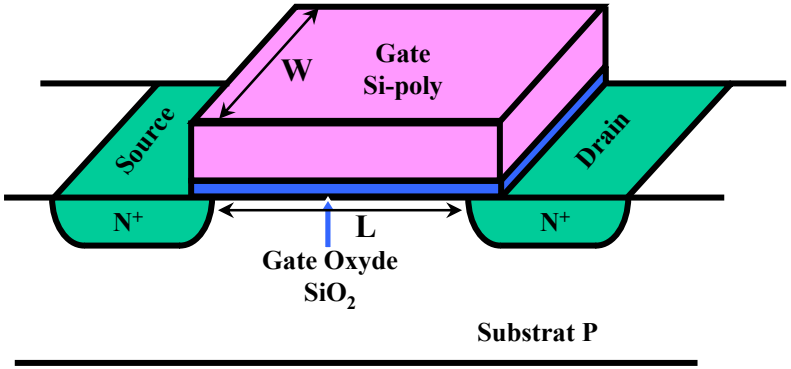
- **Frequency response**
  - Include capacitors :
    - Base-emitter junction C_π
    - Base collector junction C_μ
  - => β varies with frequency : $\beta(\omega) = g_m z_\pi(\omega)$
  - $\beta(\omega) = \beta_0 / [1 + j\,\beta_0(C_\pi + C_\mu)/g_m]$
  - $\beta(f) = 1$ for $f = f_T$ (transition frequency)
    - f_T is a function of I_C but asymptotic to a max F

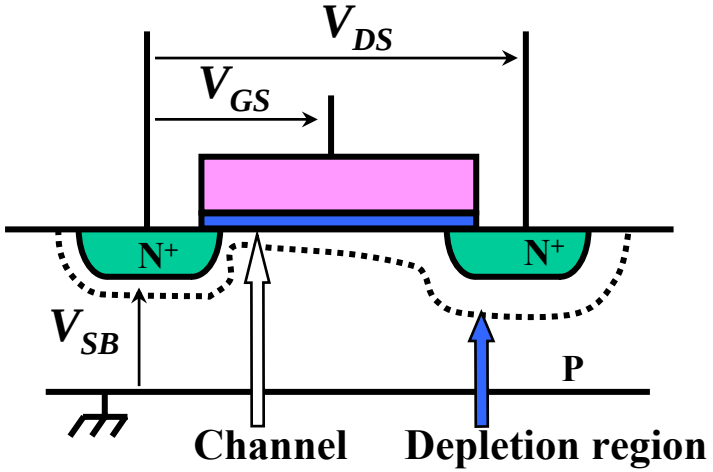


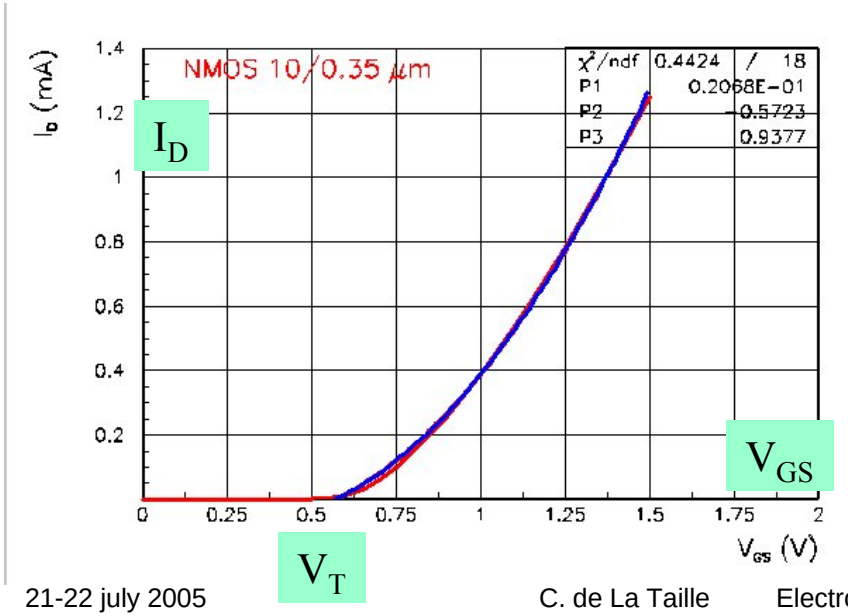
High frequency hybrid model of bipolar

Components : MOS transistors

- **Strong inversion :**
  - quadratic approximation
  - $I_D = \frac{1}{2} \mu_n C_{ox} W/L (V_{GS}-V_T)^2$
    - V_T : threshold voltage : technology dépendant
    - μ_n carrier mobility, C_{ox} gate thickness
    - W and L : dimensions = "designer's choice"
  - Voltage controlled current source
  - No gate current : $I_G=0$

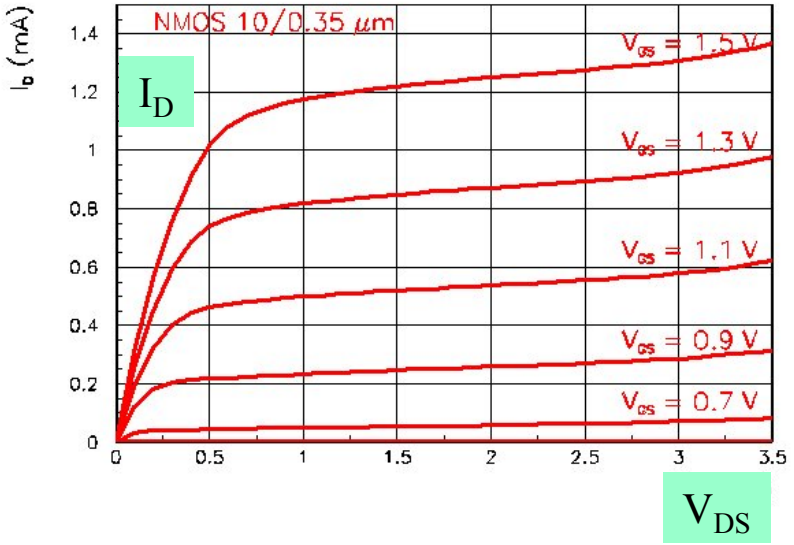


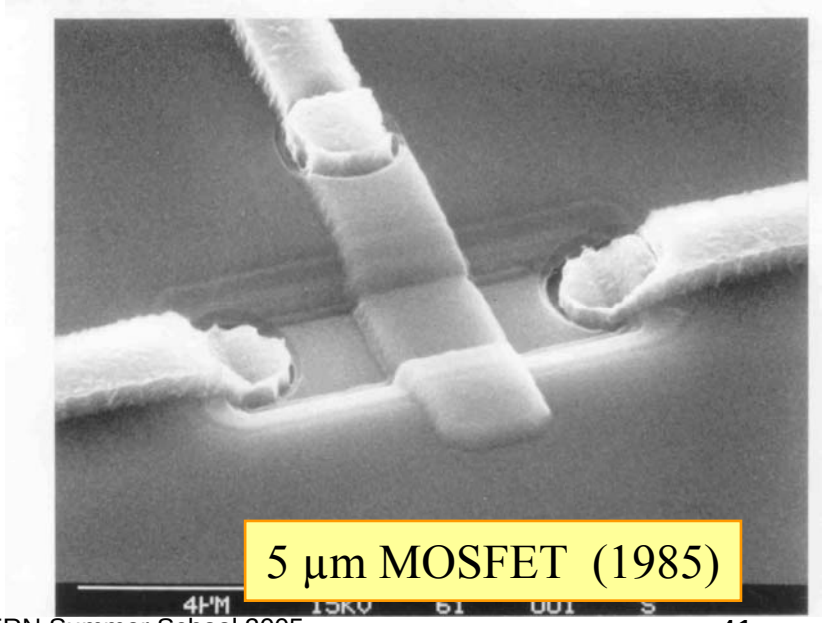




Components : MOS transistors

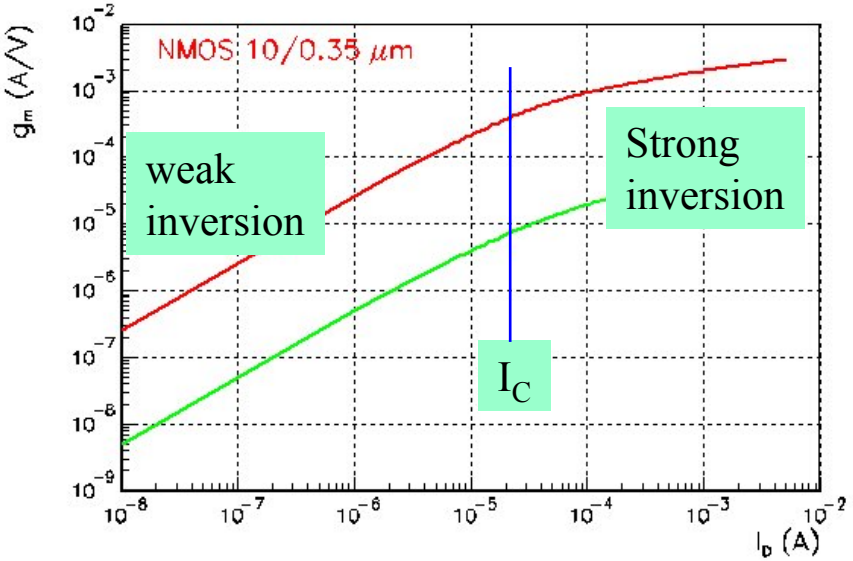
- **Weak inversion : exponential law**
  - when V_{GS} close to V_T
  - $I_D = I_{D0}\ \mathbf{exp}(V_{GS}/nU_T)$ $(1 < n < 2)$
  - Similar to bipolar with $\beta_0 \rightarrow \infty$
- **Early effect**
  - Small dependance of I_D with V_{DS}
  - Similar to bipolar transistor, but smaller V_A
- **Body effect**
  - Effect of back gate : change in effective channel thickness
  - MOS is a 4 terminals device

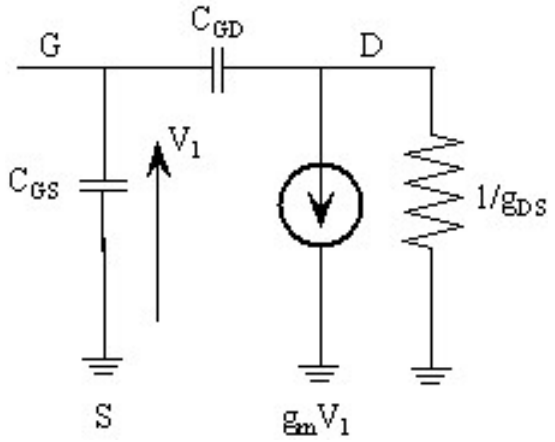




MOS hybrid π model :

- **Small signal equivalent circuit**
  - Voltage-controlled (V_{GS}) current source
  - Transconductance : $\mathbf{g_m} = \partial I_D / \partial V_{GS}$
    - Strong inversion : $g_m = (\mu_n C_{ox}\ W/L\ I_D)^{\frac{1}{2}}$
    - Weak inversion : $g_m = I_D / n U_T$
  - Input impedance : C_{GS}
  - Output impedance : $1/g_{DS} = V_E/I_D$
    - V_E : Early voltage $V_E = \alpha L$
  - Capacitance :
    - Gate-Source : C_{GS} ~ 2/3 Cox W L
    - Gate-Drain : C_{GD} ~ 1/3 Cox W L

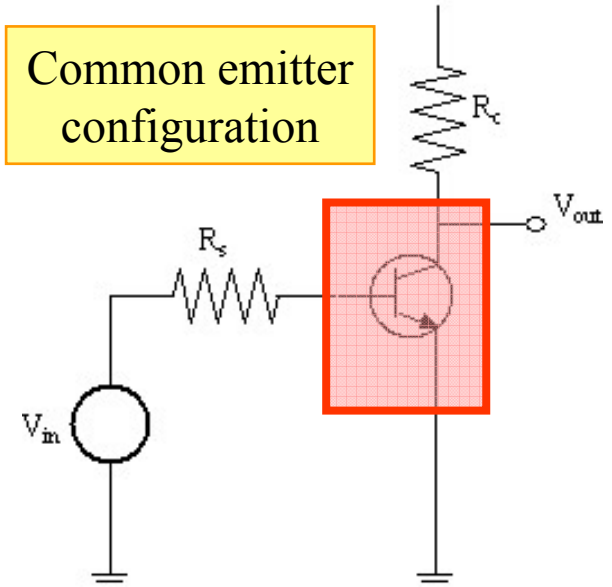


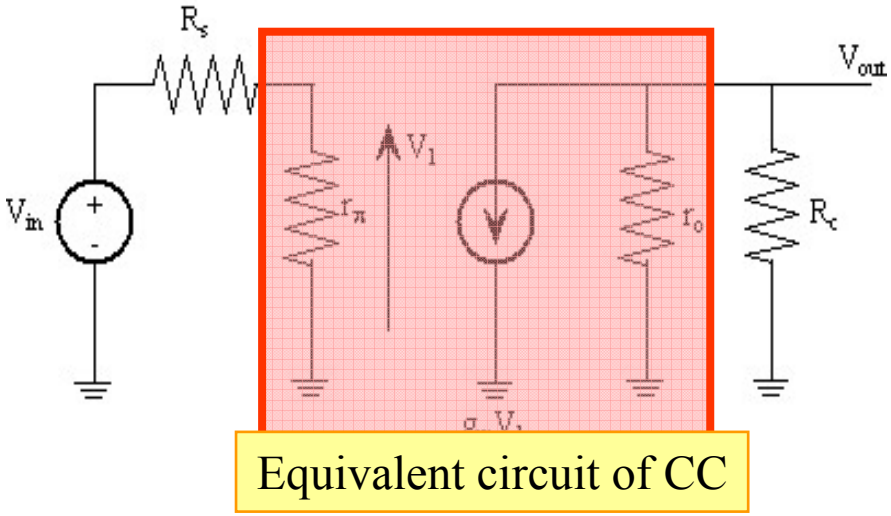


- Similar hybrid π model as the bipolar
  - g_m remains g_m (but smaller)
  - r_π -> ∞
  - r_0 -> $1/g_{DS}$

Common emitter (CE) configuration

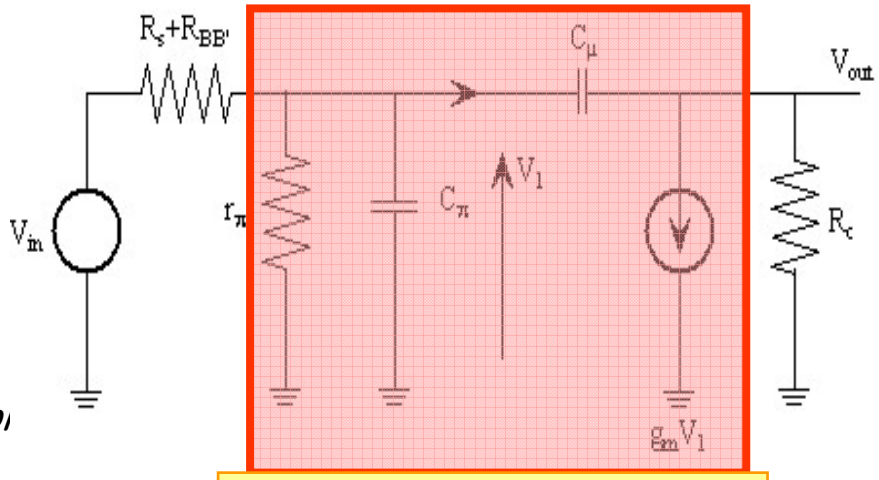
- **Emitter common to input and output**
  - Input on the base
  - Output on the collector
  - "common source" with MOS
- **Low frequency characteristics**
  - Input impedance Rin = r_π $(=\beta_0/g_m)$
  - Output impedance: Rout = r_0 $(=V_A/I_C)$
  - Voltage gain : $G = v_{out}/v_{in} = - g_m R_L$
  - Inverting amplifier
- ***Transconductance stage***
  - Large Zin : voltage sensitive input
  - Large Zout : current driven output
  - Transconductance g_m determined by bias current I_C





Common emitter frequency response

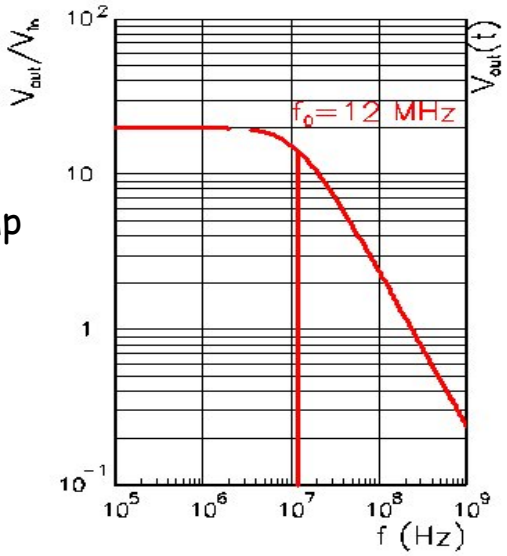
- **Frequency response**
  - Include capacitors : Cπ, Cμ
  - Effect of C_μ: Miller effect
  - = apparent input capacitance C_{Mi}
  - $C_{Mi} = (1 + g_m R_L) C_\mu$
  - Gain : $Av = -g_m R_L / [1 + j\omega R_S (C_\pi + C_{Mi})]$
  - *Ex : R_S=1 kΩ R_L=20kΩ g_m=1 mA/V C_π=2.5 pF C_μ=0.5 pF => C_{Mi} = 10 pF tau=12.5ns*

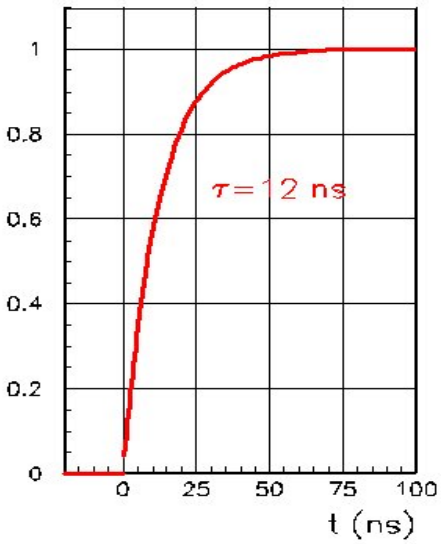


Frequency response of CE

- **Time response**
  - $H(t) = \mathcal{F}^{-1} \{ 1/j\omega \; R/(1+j\omega RC) \}$
    $= R [1 - \exp(-t/\tau)]$
  - $\tau = R_S (C_\pi + C_{Mi})$
  - Similar calculation as photodiode preamp

- **Slow configuration**

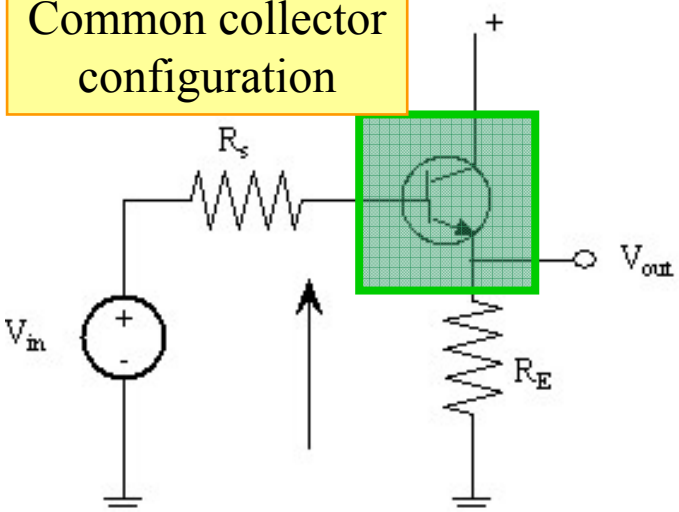


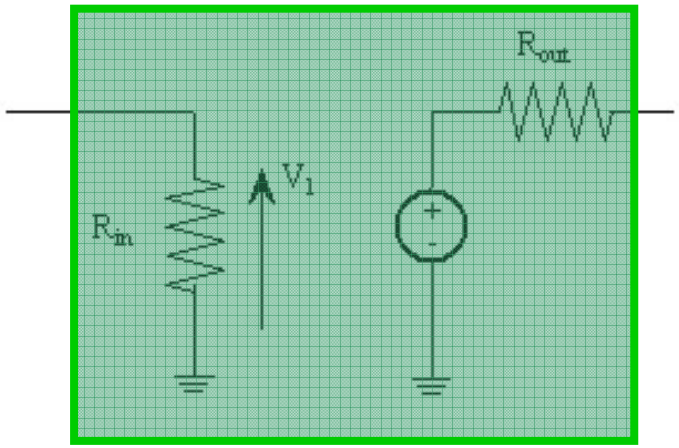


Common collector (CC) :

- **Collector common to input and output**
  - Input on the base
  - Output on the emitter
  - = Common drain for MOS
- **Low frequency characteristics**
  - Input impedance Rin = $r_\pi + \beta_0 R_E$
  - Output impedance: Rout = $R_S/\beta_0 + 1/g_m$
  - Voltage gain : Av = $v_{out}/v_{in} = 1/(1+1/g_m R_E) \leq 1$
  - Non inverting
- **Voltage follower or "emitter follower"**
  - Large Zin : voltage sensitive input
  - Small Zout : voltage driven output
  - Unity gain buffer : "the emitter follows the base"
- **Frequency response : ~F_T**
  - Small apparent input capacitance

Common collector configuration

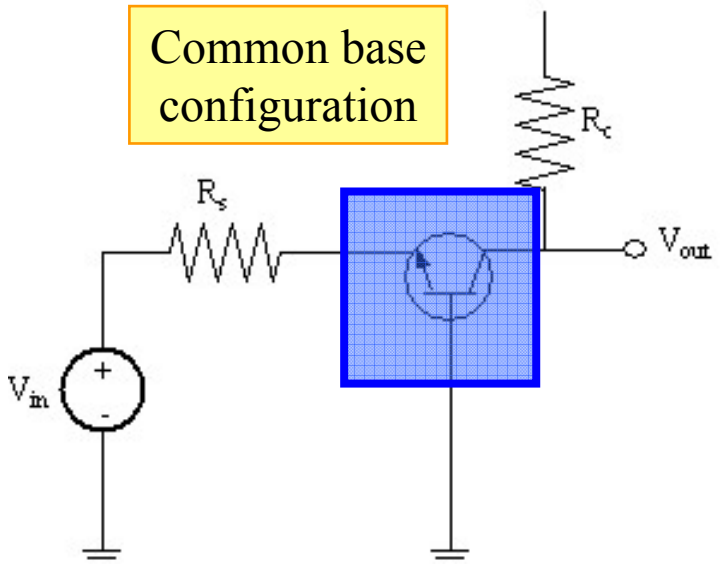


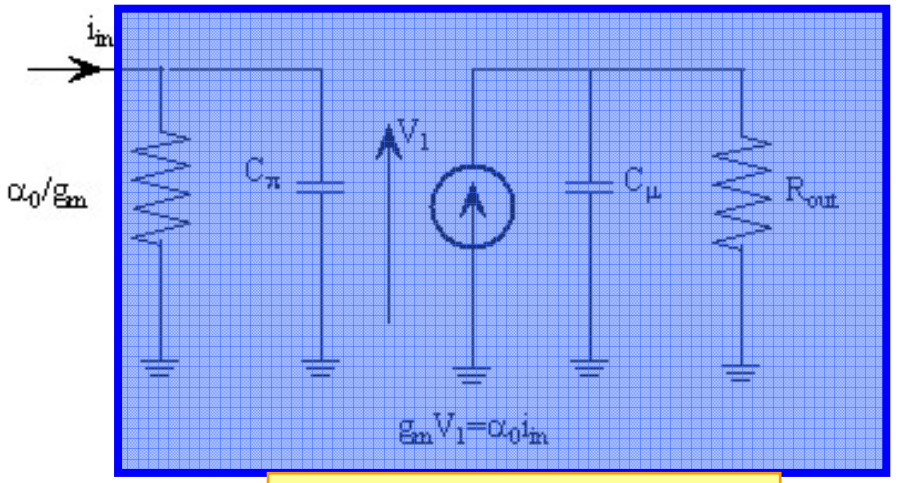


Equivalent circuit of CC

Common base (CB) :

- **Collector common to input and output**
  - Input on the emitter
  - Output on the collector
- **Low frequency characteristics**
  - Input impedance Rin = $1/g_m$
  - Output impedance: Rout = $(1+g_m R_S)r_0$
  - Current gain : $A_i \sim 1$
  - Non inverting
- **Current conveyor**
  - Small Zin : current sensitive input
  - Large Zout : current driven output
  - Unity gain current conveyor
- **Frequency response : ~F_T**
  - Very fast
  - Excellent isolation input/output

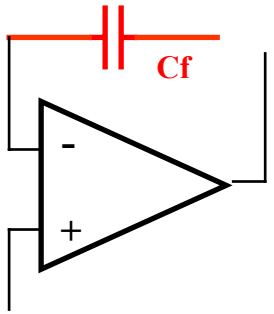


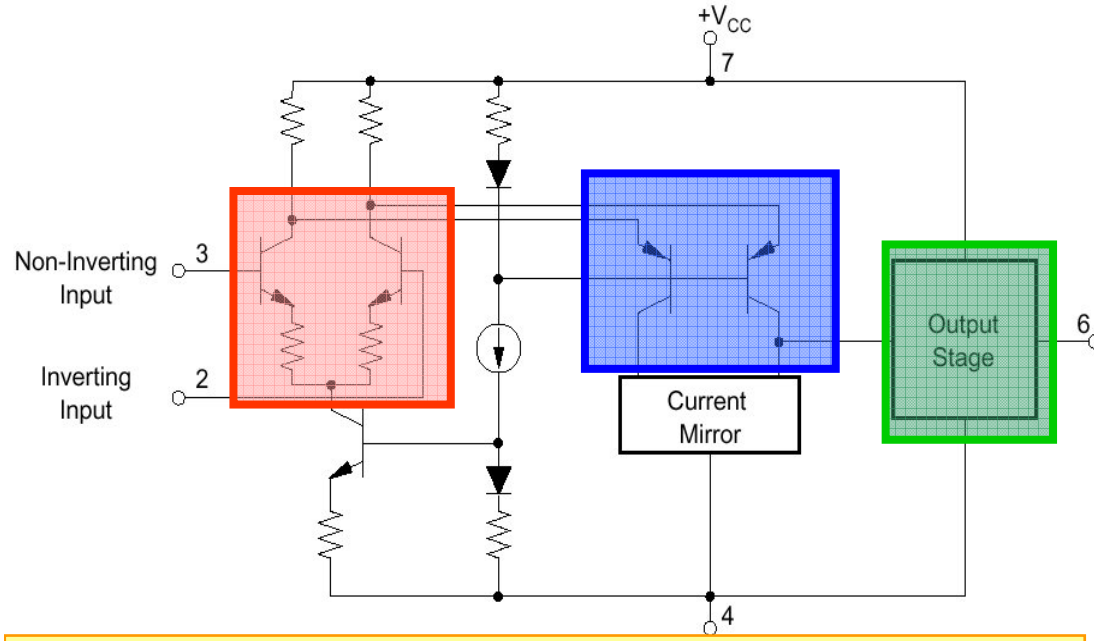


Equivalent circuit of CC

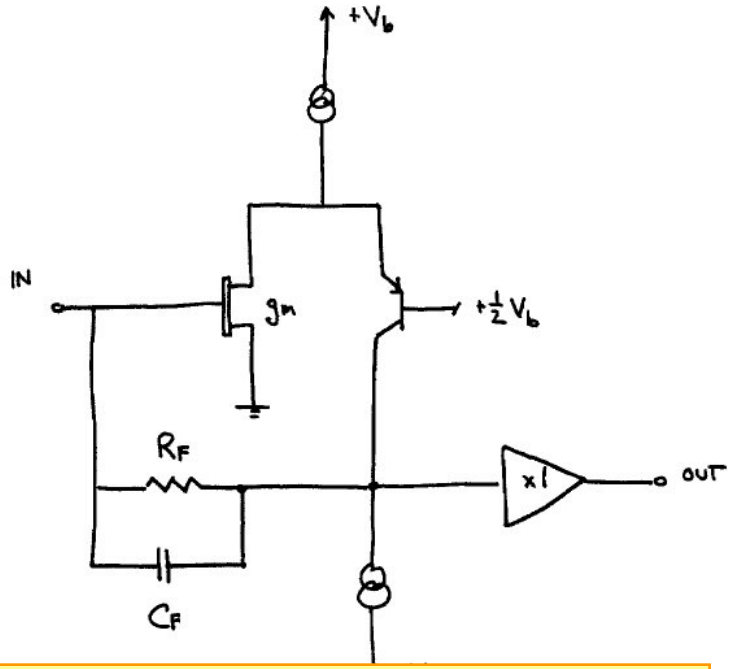
Example : designing a charge preamp (1)

- **From the schematic of principle**
  - Using of a fast opamp (OP620)
  - Removing unnecessary components…
  - Similar to the traditionnal schematic «Radeka 68 »
  - Optimising transistors and currents





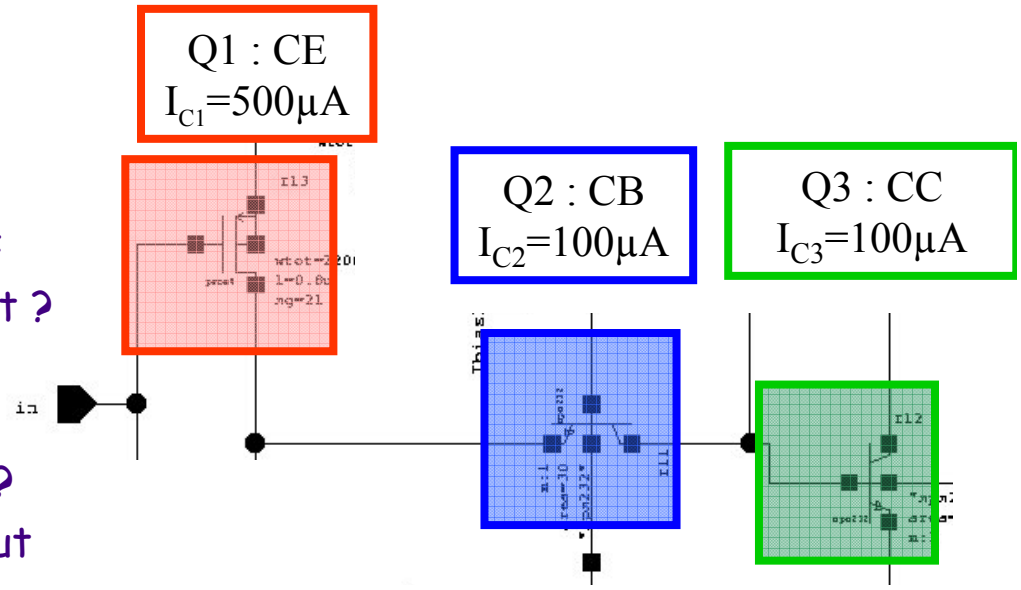
Schematic of a OP620 opamp ©BurrBrown



Charge preamp ©Radeka 68

Example : designing a charge preamp (2)

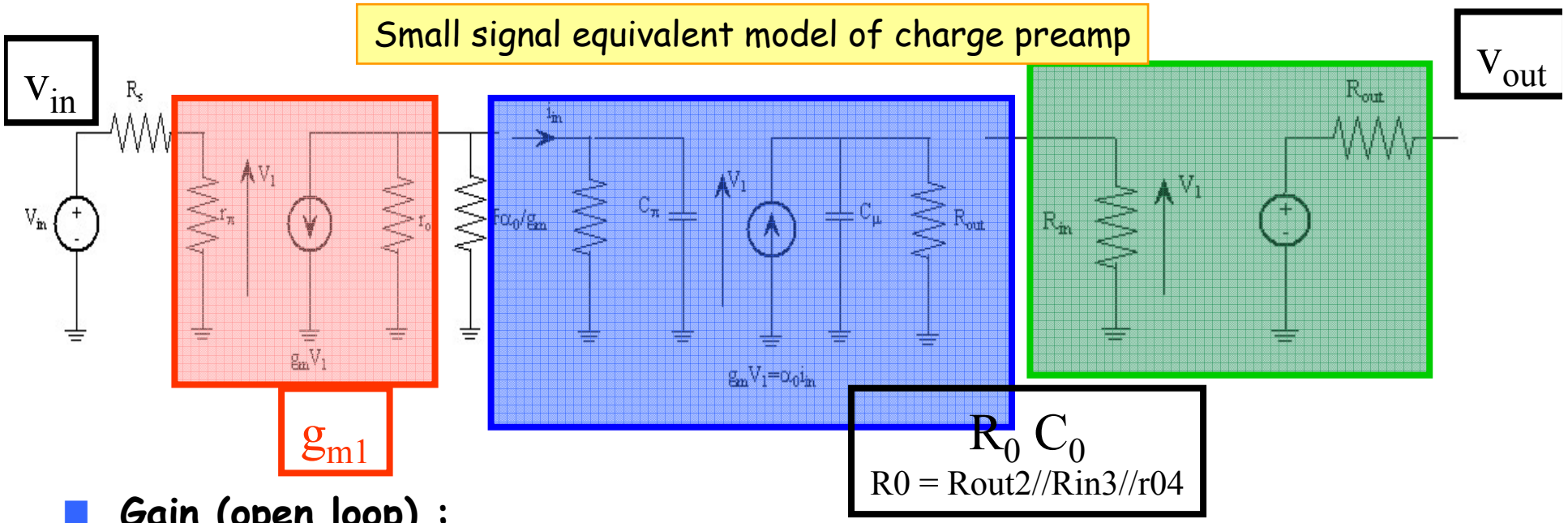
- **Simplified schematic**
- **Optimising components**
  - What transistors (PMOS, NPN ?)
  - What bias current ?
  - What transistor size ?
  - What is the noise contributions of each component, how to minimize it ?
  - What parameters determine the stability ?
  - Waht is the saturation behaviour ?
  - How vary signal and noise with input capacitance ?
  - How to maximise the output voltage swing ?
  - What the sensitivity to power supplies, temperature…



Simplified schematic of charge preamp

Example : designing a charge preamp (3)

- **Small signal equivalent model**
  - Transistors are reaplaced by hybrid π model
  - Allows to calculate open loop gain



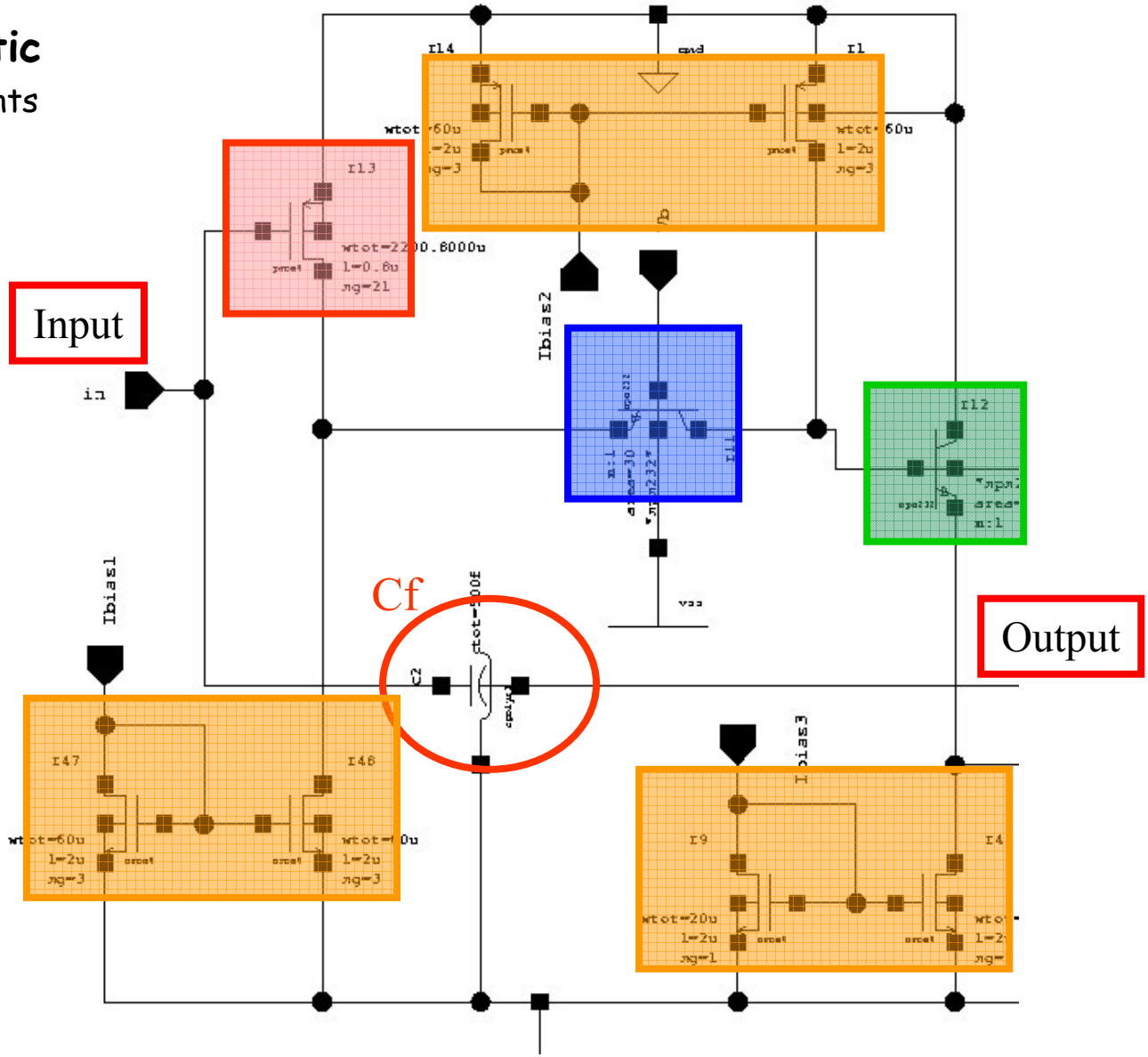
- **Gain (open loop) :**

$$v_{out}/v_{in} = - g_{m1} R_0 /(1 + j\omega R_0 C_0)$$

- *Ex : g_{m1}=20mA/V , R_0=500kΩ, C_0=1pF => G_0=10^4 ω_0=210^6 $G_0\omega_0$=$2\ 10^{10}$ = 3 GHz !*

Example : designing a charge preamp (4)

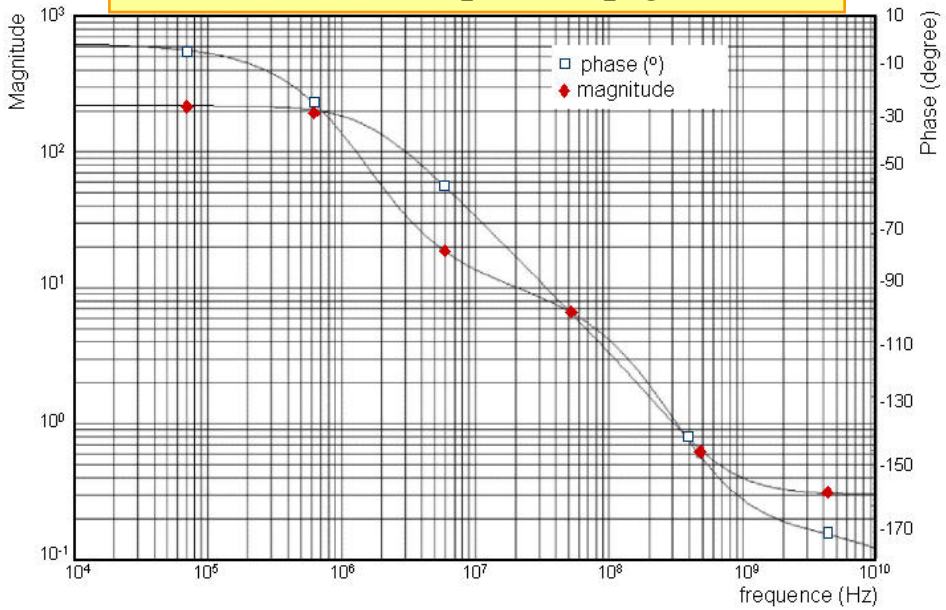
- **Complete schematic**
  - Adding bias elements



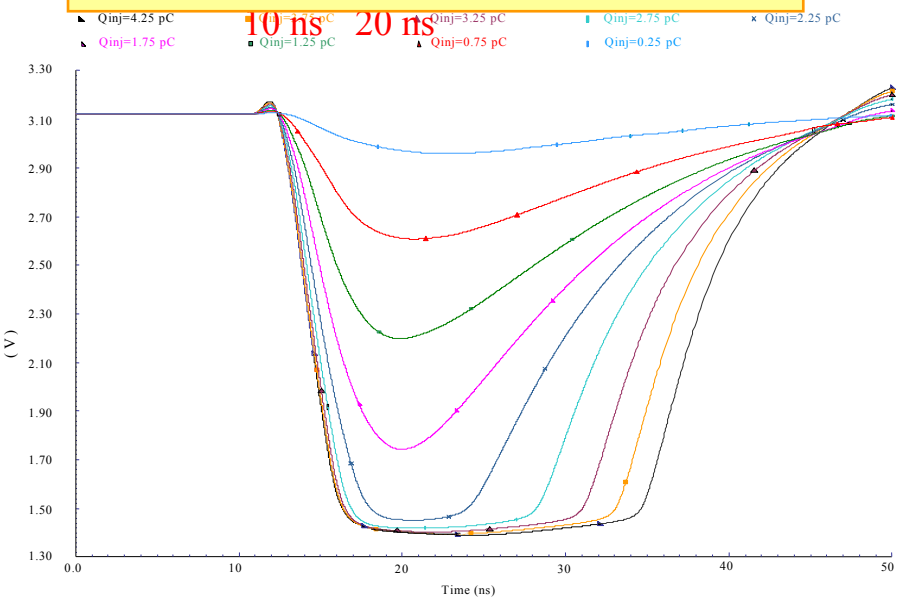
Example : designing a charge preamp (5)

- **Complete simulation**
  - Checking hand calculations against 2nd order effects
  - Testing extreme process parameters (« corner simulations »)
  - Testing robustness (to power supplies, ntemperature…)

Simulated open loop gain



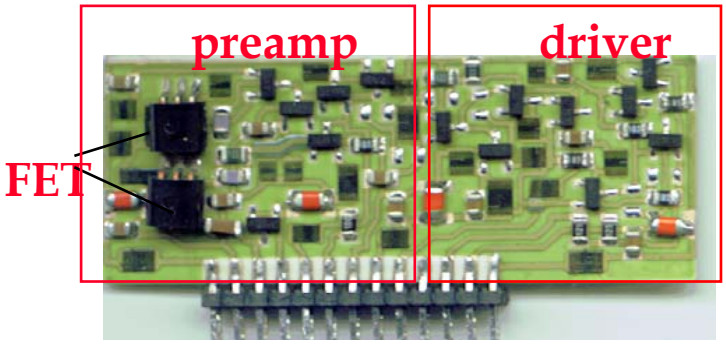
Saturation behaviour



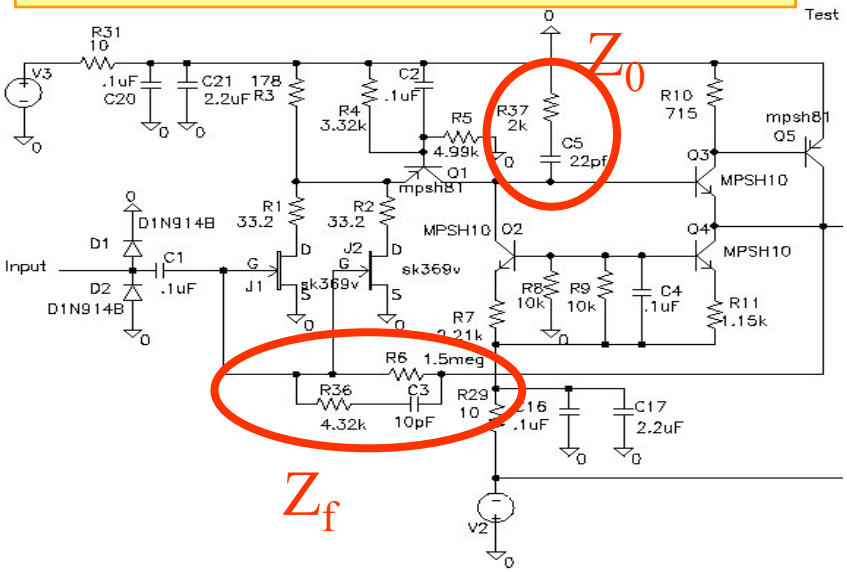
1 MHz

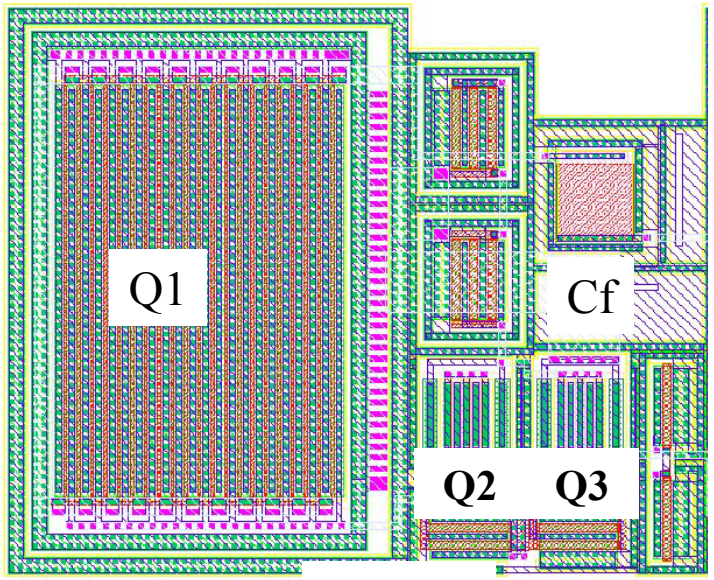
Practical realization

- Acces to microelectronics

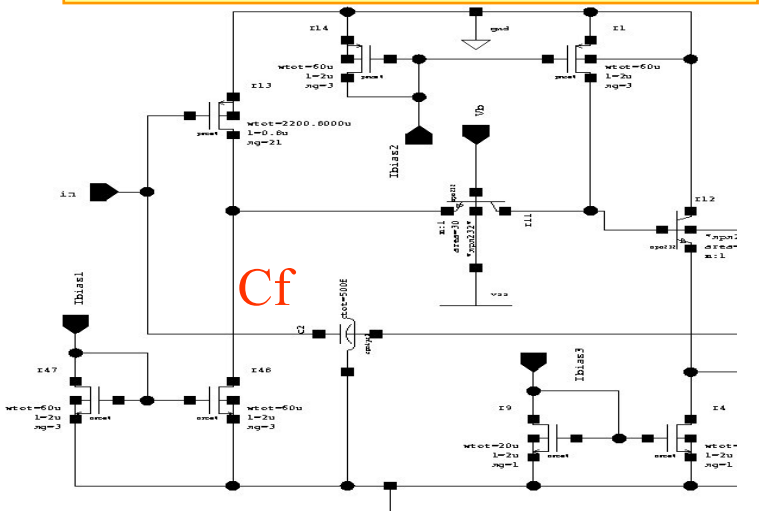


Charge preamp in SMC hybrid techno



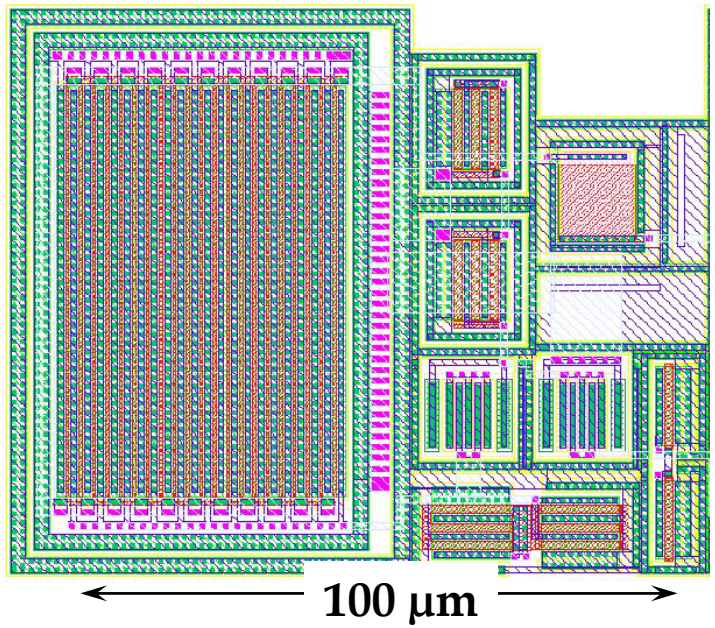


Charge preamp in 0.8µm BiCMOS



Example : designing a charge preamp (6)

- **Layout**
  - Each component is drawn
  - They are interconnected by metal layers



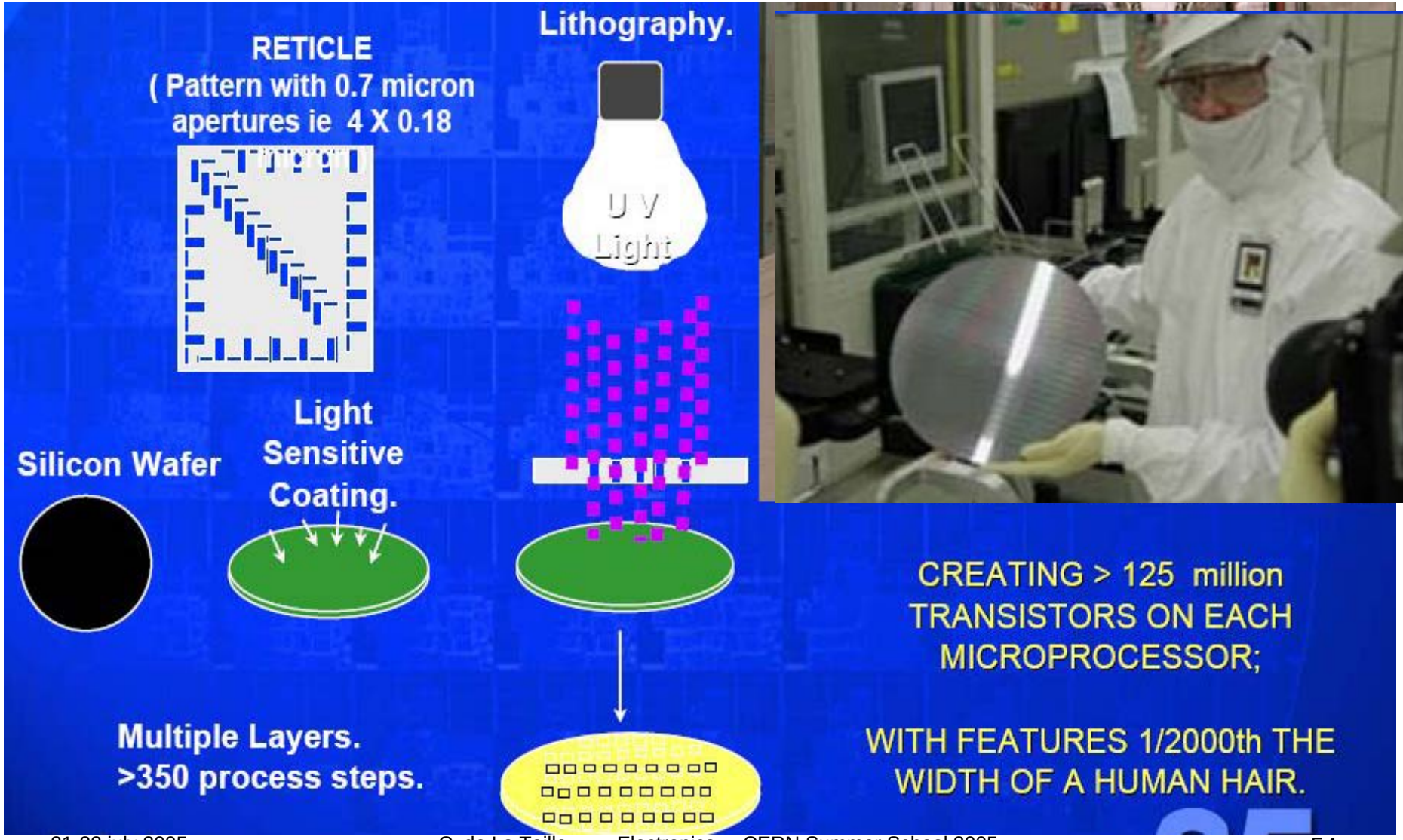
- **Checks**
  - DRC : checking drawing rules (isolation, minimal dimensions…)
  - ERC : extracting the corresponding electrical schematic
  - LVS (layout vs schematic) : comparing extracted schematic and original design
  - Simulating extracted schematic with parasitic elements

- **Generating GDS2 file**
  - Fabrication masks : « reticule »

Processing of ASICs

© Intel

- From Sand to ICs…



Course 3 : Electronics in High Energy physics, evolution of technologies and examples

CERN Summer school 2005

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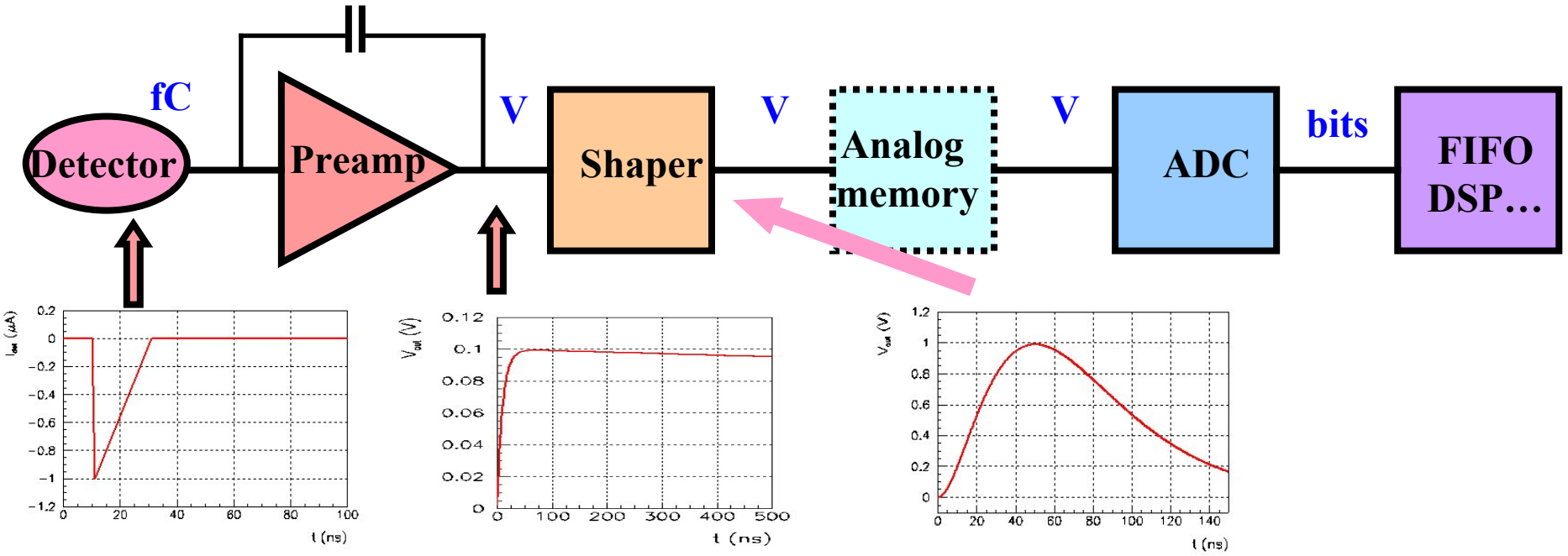
LABORATOIRE DE L'ACCÉLÉRATEUR LINÉAIRE

CENTRE NATIONAL DE LA RECHERCHE SCIENTIFIQUE

Overview of readout electronics

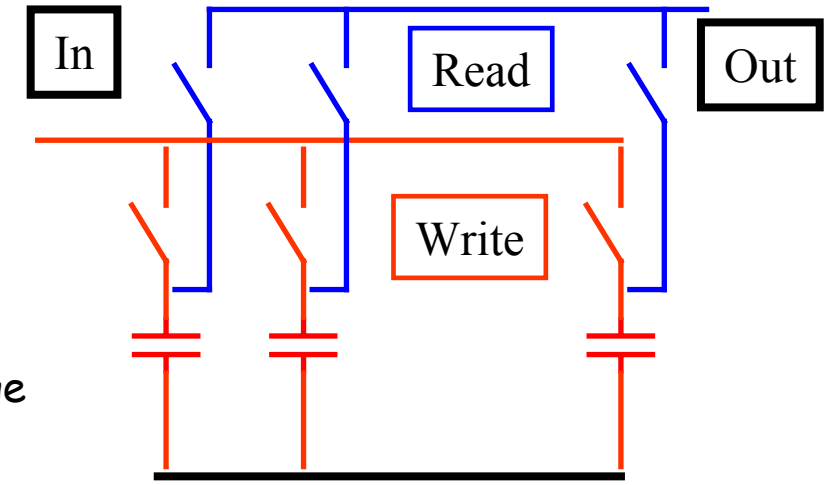
- Most front-ends follow a similar architecture



- Very small signals (fC) -> need amplification
- Measurement of amplitude and/or time (ADCs, discris, TDCs)
- Several thousands to millions of channels

Analog memories

- **Switched Capacitor Arrays (SCAs)**
  - Store signal on capacitors (~pF)
  - Fast write (~ GHz)
  - Slower read (~10MHz)
  - Dynamic range : 10-13 bits
  - depth : 100-2000 caps
  - Unsensitive to cap absolute value (voltage write, voltage read)
  - Low power
  - Possible loss in signal integrity (droop, leakage current)

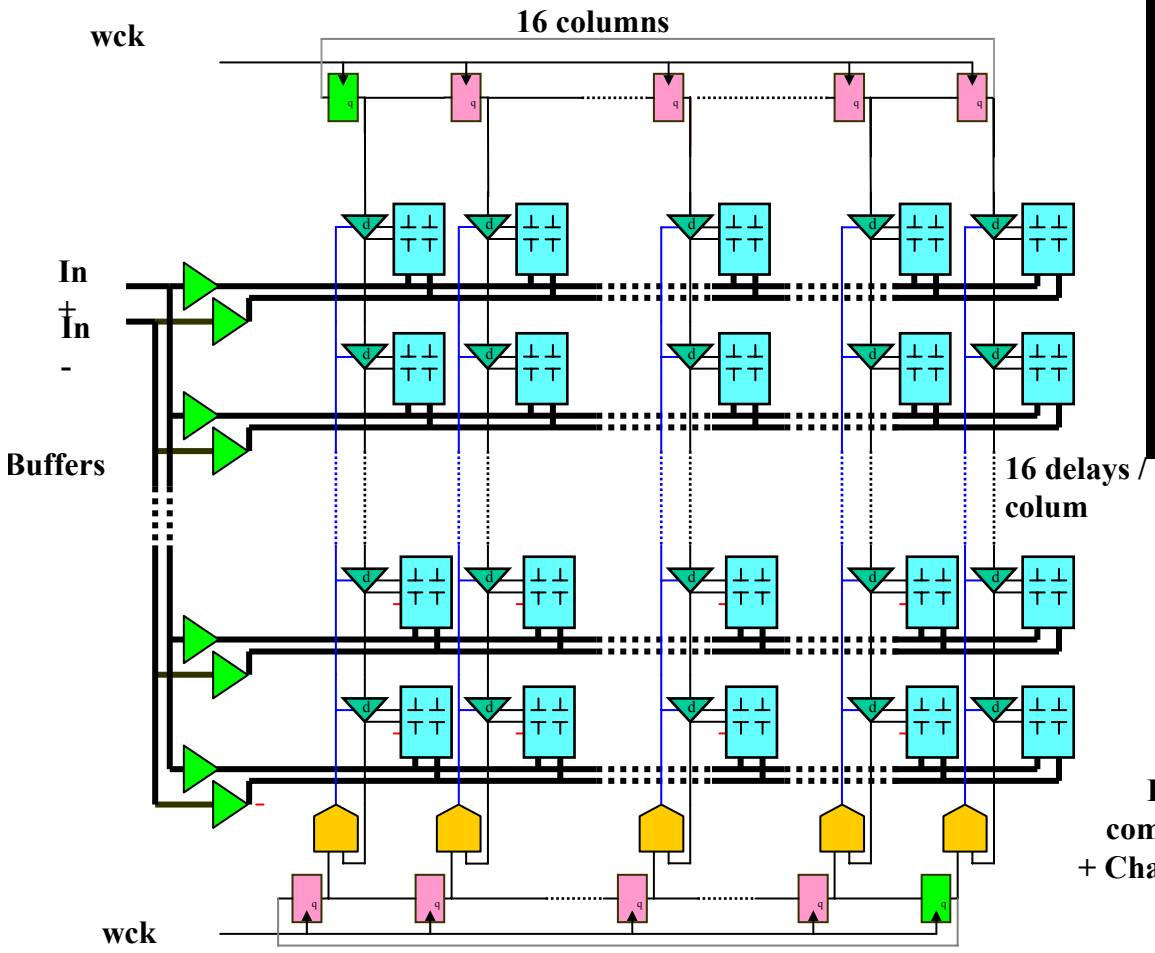


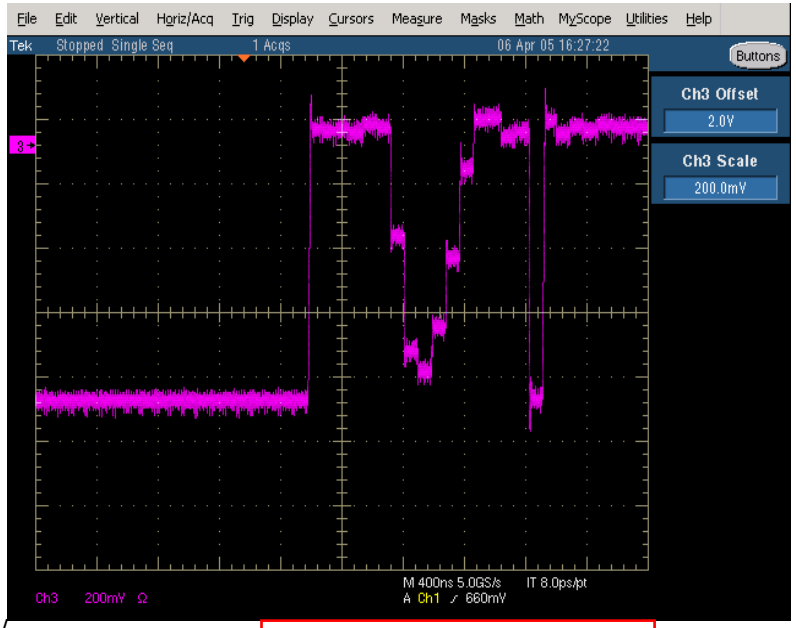
Principle of a « voltage-write, voltage-read » analog memory

- **The base of 90% of digital oscilloscopes !**

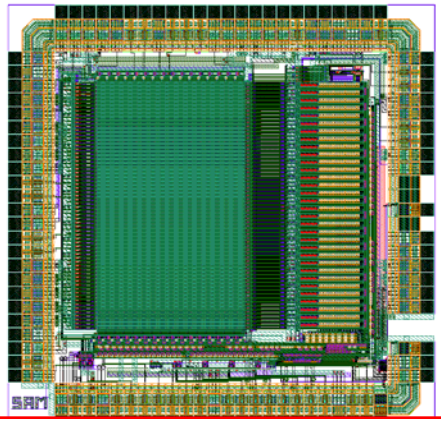
Example : SAM for HESS2

- **Swift Analog Memory**
  - 3 Gsample/s >10 bits





2 ns pulse in SAM0



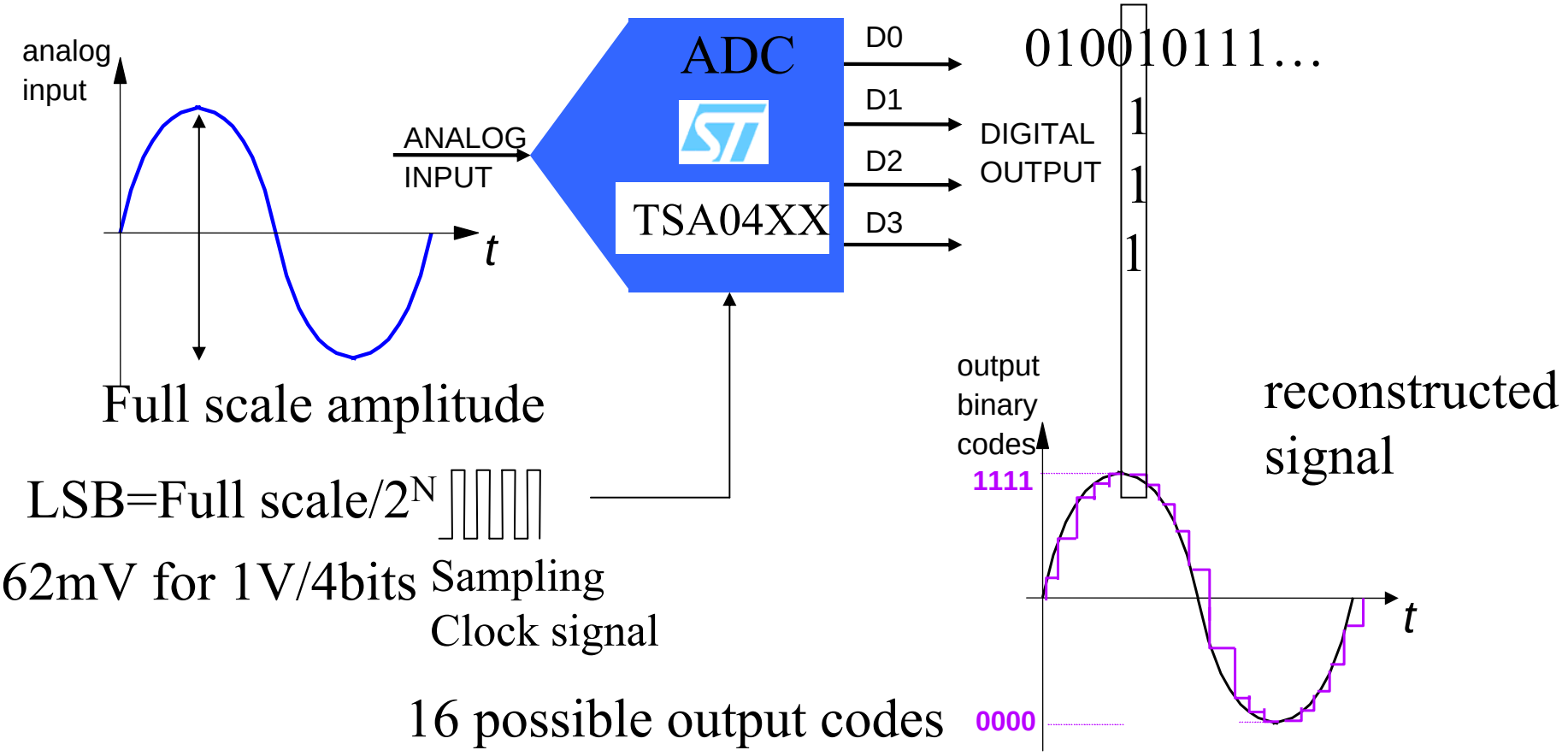
chip layout in 0.35µ CMOS

+ serial link for configuration set-up

Analog to Digital Converter (ADC)

[P. Dugoujon LEB8 Colmar 02]

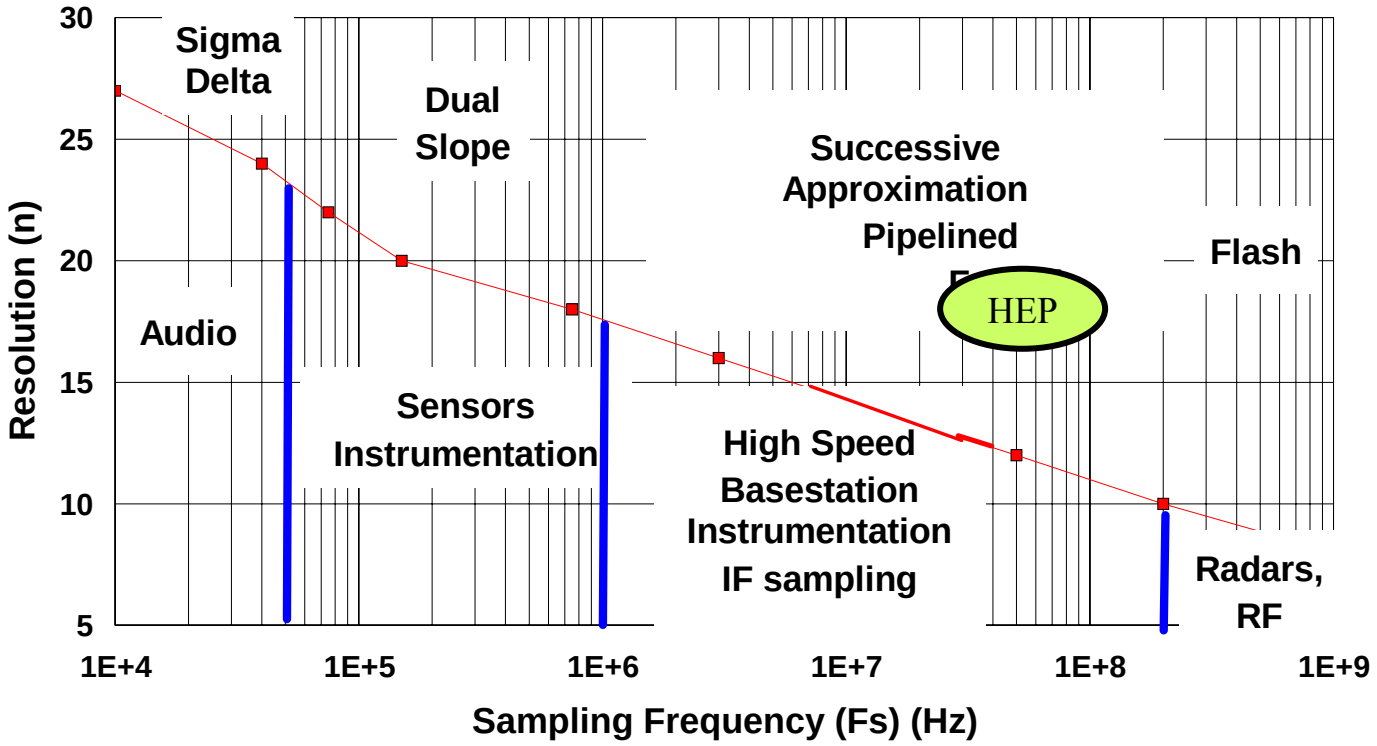
Ex:4 bits A/D converter.



ADCs : G.D.A.S.A.P.

- **The era of G.D.A.S.A.P. : « go digital as soon as possible »**
  - Spectacular evolution of ADCs : more bits, faster, less watts
  - Propelled by evolution of technologies and telecom
- **Has revolutionnized signal processing**
- ***A large effort starting to develop ADCs for HEP in the institutes***

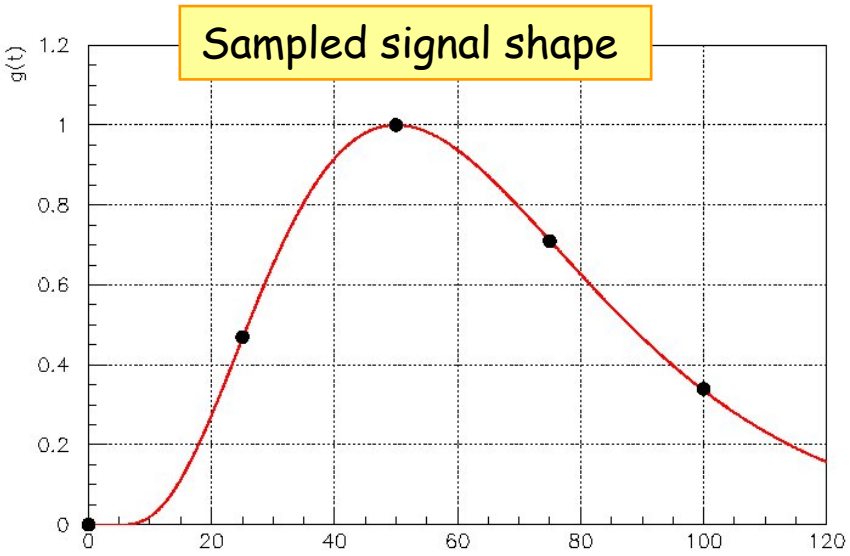
[L. Dugoujon LEB 2002]

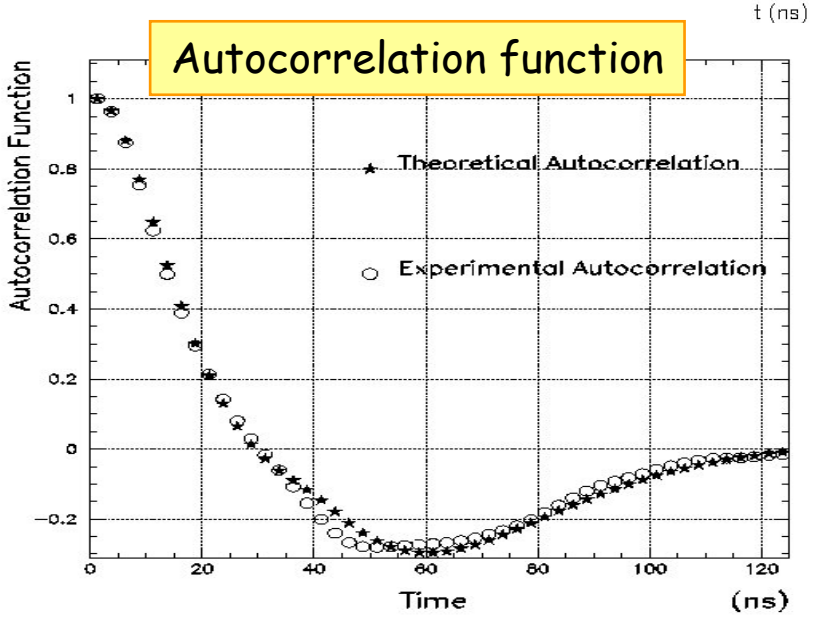


Resolution vs speed of ADCs in 2002
© L. Dugoujon STm

Digital filtering

- **Linear sums of sampled signal**
  - Finite Impulse Respopnse (FIR)
  - **made possible by fast ADCs (or analog memories)…**
- **Signal : $s(t)=Ag(t)+b$**
  - A : amplitude
  - $G(t)$: normalised signal shape
  - B : noise
  - Sampled signal : $s_i=Ag_i+b_i$
- **Filter : weighted sum $\Sigma\ a_i\ s_i$**
  - $a_i = \Sigma\ R^{-1}_{ij}\ g_i$
  - R = autocorrelation fonction
  - g_i = signal shape
    (0, 0.63, 1, 0.8, 0.47)
  - $S = \Sigma^{n}_{i=1}\ a_i s_i$

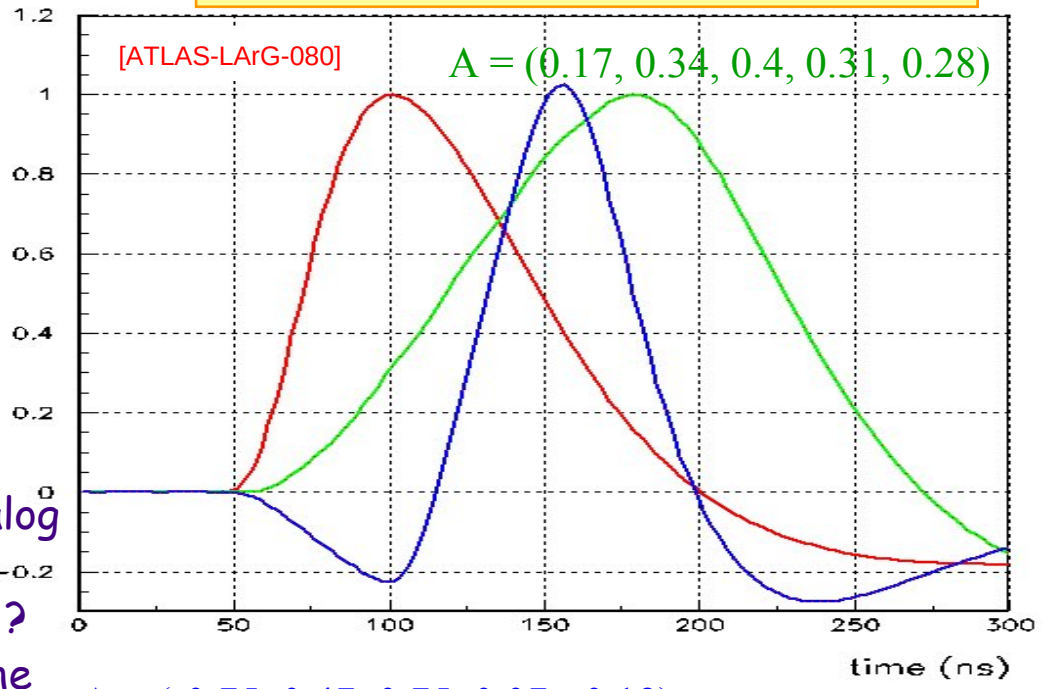




Exemple : ATLAS "multiple sampling"

- **Slowing down the signal**
  - Reduction of series noise
  - Similar to a simple integration
- **Accelererating the signal**
  - Reduction of pileup noise
  - Similar to a differentiation
- **Measuring the timing**
- **Some questions**
  - How does-it compare to an analog filter
  - How many samples are needed ?
  - What accuracy is needed on the waveform and on the autocorrelation ?
  - What analog shaping time is needed ?
  - Is the analog filter really useful ?

Signal before and after digital filtering

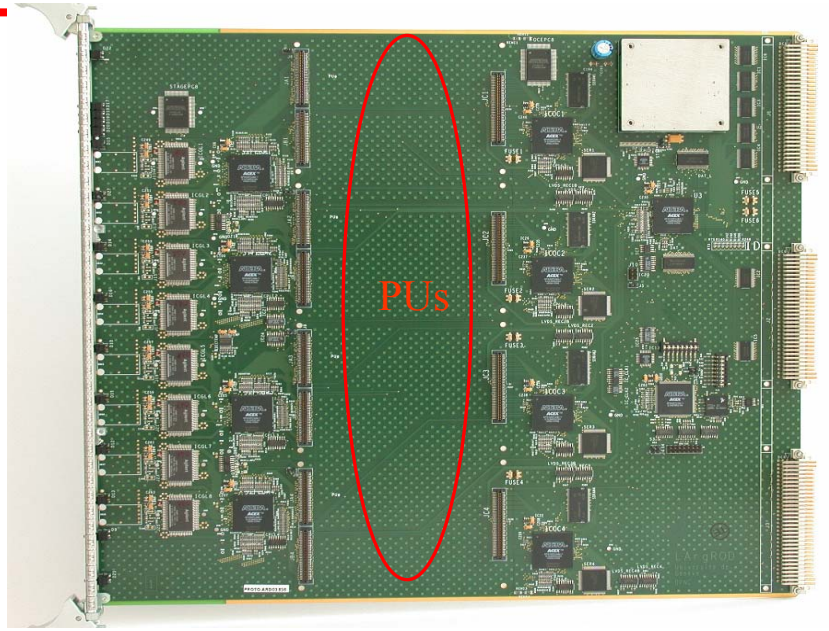


A = (-0.75, 0.47, 0.75, 0.07, -0.19)

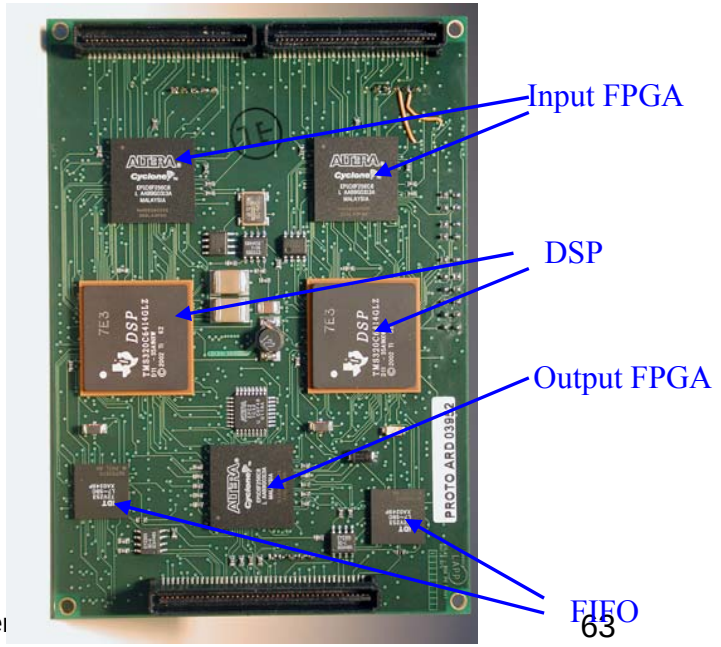
Digital data handling

- Example : ATLAS Read-out drivers

- ROD Motherboard (MB) architecture:
  - Custom ORx modules, GLink deserialisers
  - FPGAs re-route data to every other PU in initial "staging" mode
  - O/P data serialized and sent thru backplane to TM and then to L2/DAQ

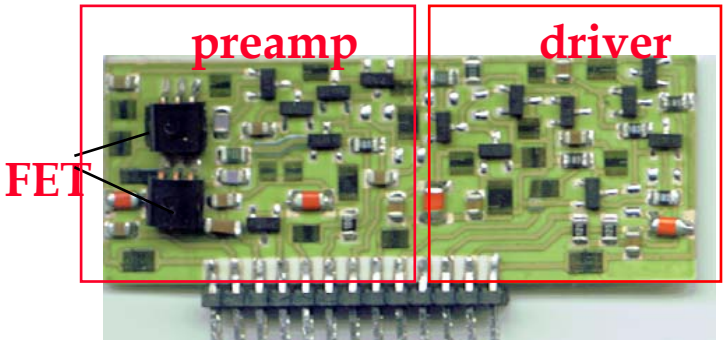


- Processing Unit (PU) architecture:
  - Two PUs per daughterboard
  - Cyclone I/P FPGA for data checking, reformatting
  - TMS DSP 720 MHz for processing (1 FEB @ 100 kHz)
  - FIFOs for O/P data interface to MB
  - O/P FPGA for VME interface, histo. readout

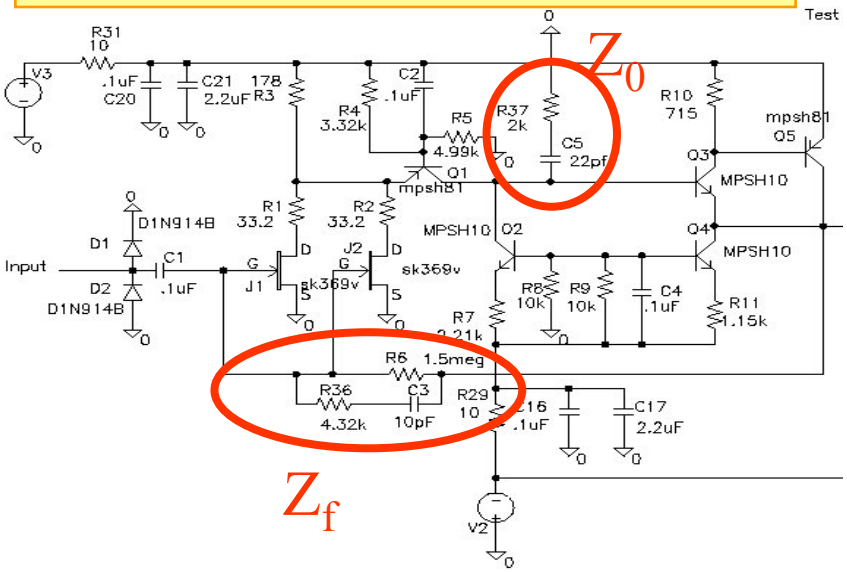


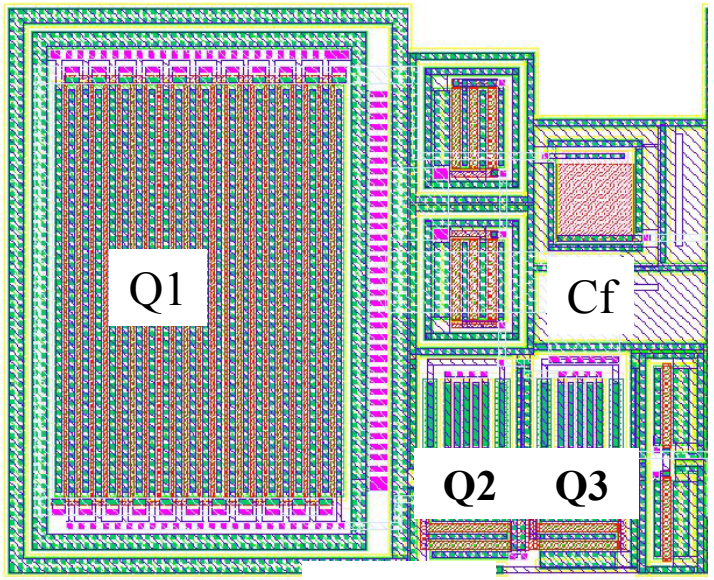
(R)evolution of analog electronics (1)

- Acces to microelectronics

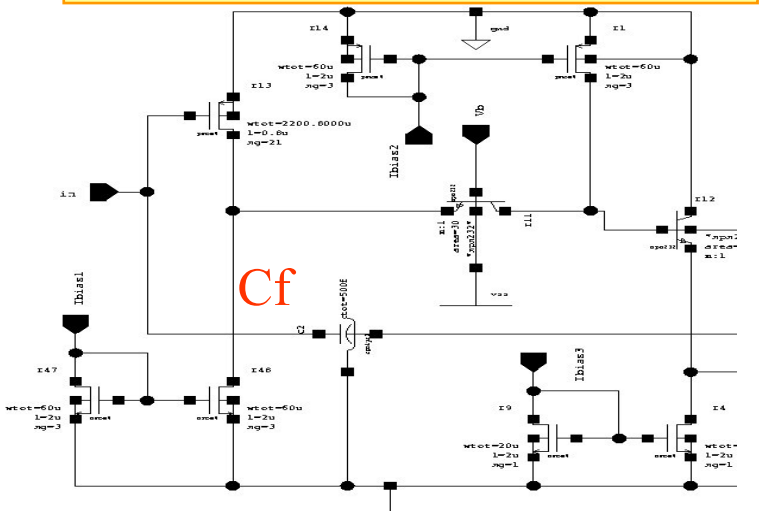


Charge preamp in SMC hybrid techno





Charge preamp in 0.8µm BiCMOS

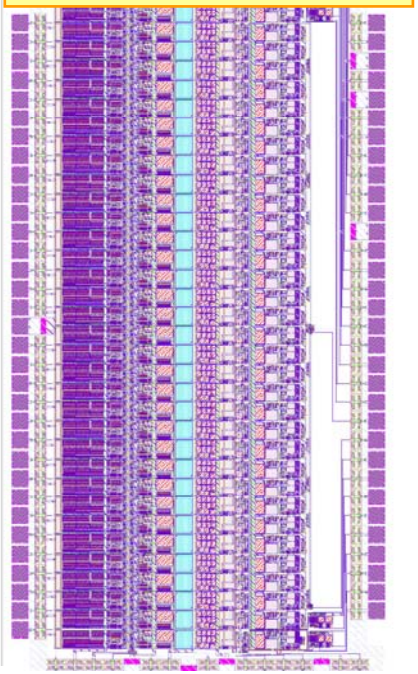


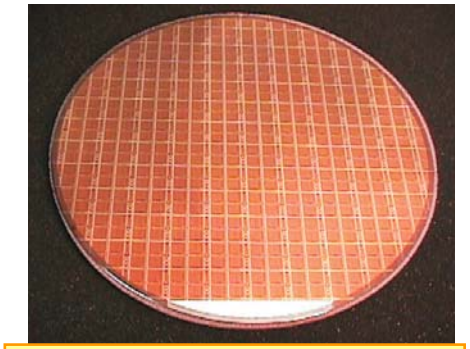
(R)evolution of analog electronics (2)

- **ASICs : Application Specific Integrated Circuits**
  - Access to foundries through multiproject runs (MPW)
  - Reduced development costs : 600-1000 €/mm^2 compared to dedicated runs (50-200 k€)
  - Full custom layout, at transistor level
  - mostly CMOS & BiCMOS

- **Very widespread in high Energy Physics**
  - High level of integration, limited essentially by power dissipation and parasitic couplings (EMC)
  - Better performance : reduction of parasitics
  - Better reliability (less connections)
  - But longer developpement time

Layout 32ch ASIC

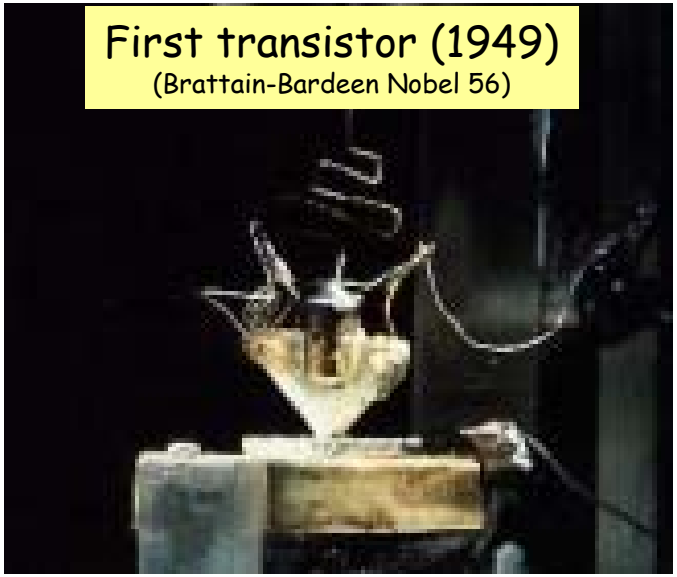




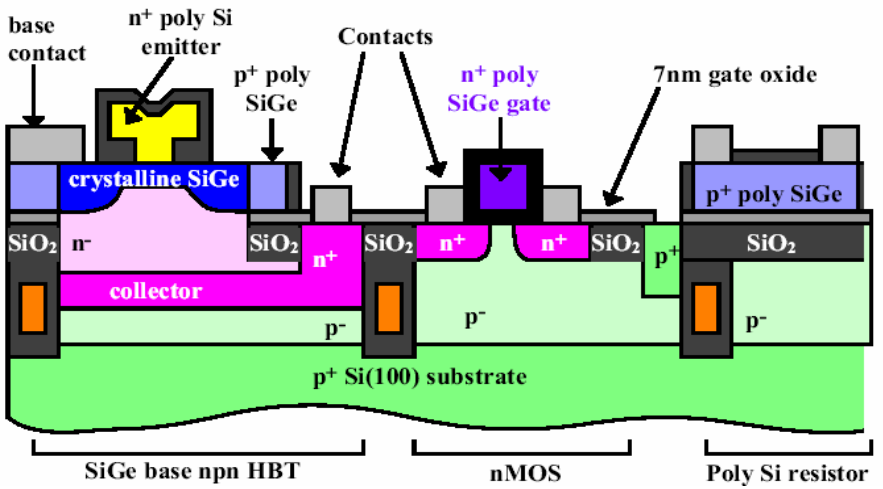
300 mm wafer (IBM)

Evolution of technologies

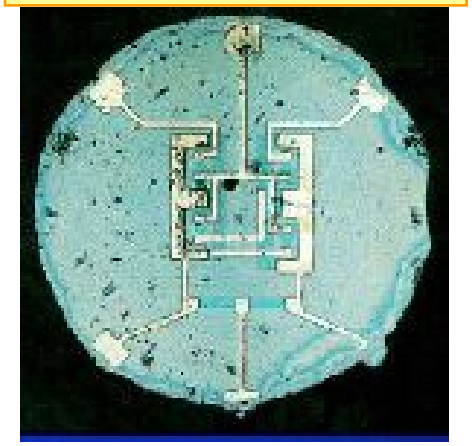
First transistor (1949)
(Brattain-Bardeen Nobel 56)



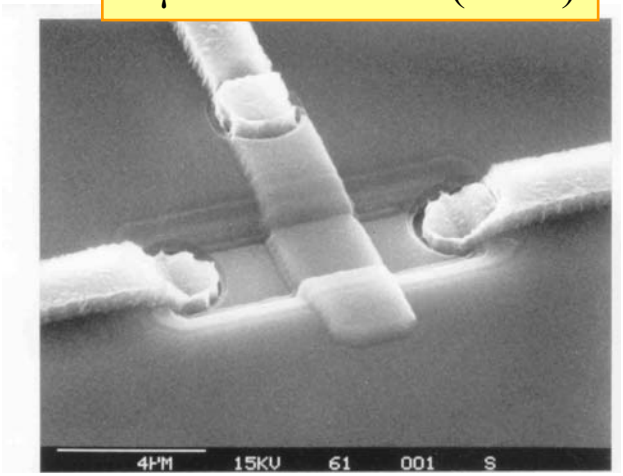
SiGe Bipolar in 0.35µm monolithic process



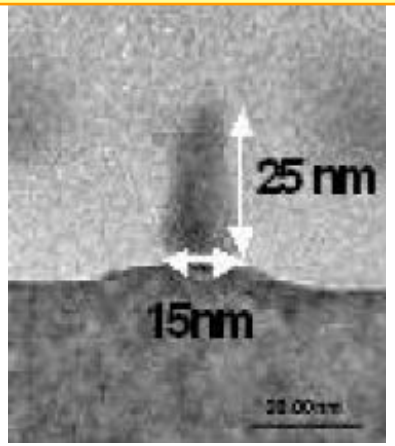
First planar IC (1961)



5 µm MOSFET (1985)

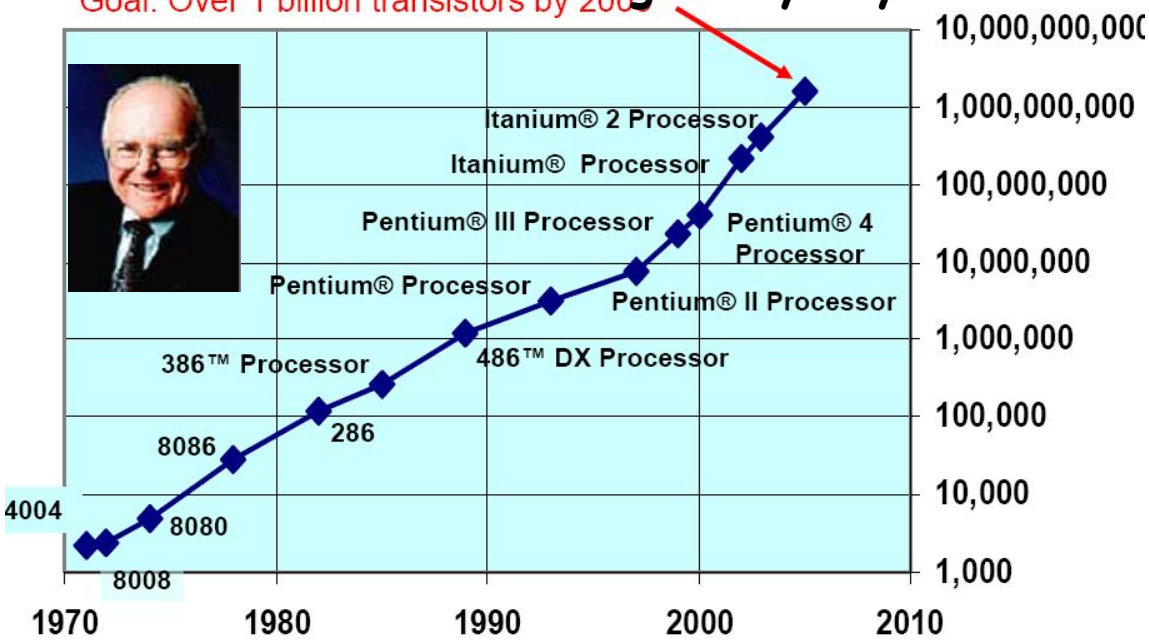


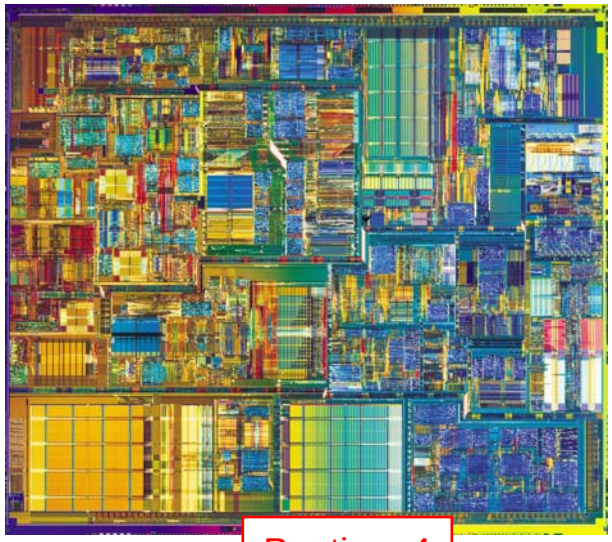
15 nm MOSFET (2005)



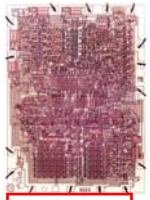
Evolution of CMOS technologies

- Moore's law : doubling every 2 years





Pentium 4



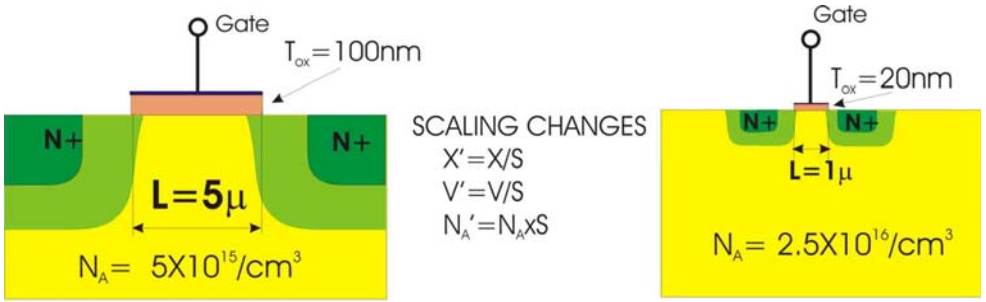
4004

Microprocesseur	4004	8086	i386	Pentium	Pentium 4
Année	1971	1978	1985	1993	2000
Nb. Bits	4	16	32	64	64
Horloge (Hz)	108k	10M	33M	66M	1.5G
Mémoire adressable (bytes)	640	1M	16M	4G	64G
Technologie (µm)	10	3	1	0.8	0.18
Nb transistors	2300	29000	275000	3.1M	42M
Tension alim (V)	12	5	5	5/3.3	1.3 interne

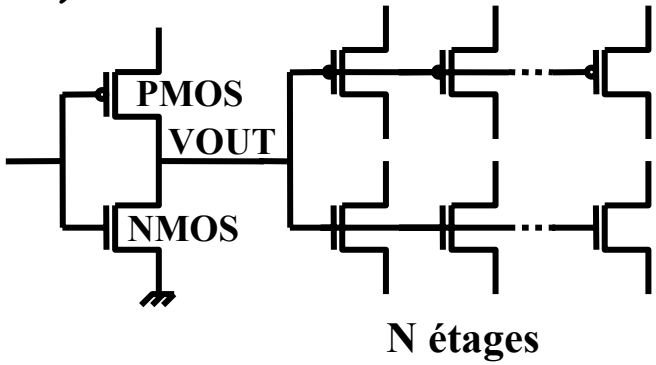
CMOS scaling

[P. Jarron LEB8 Colmar 02]

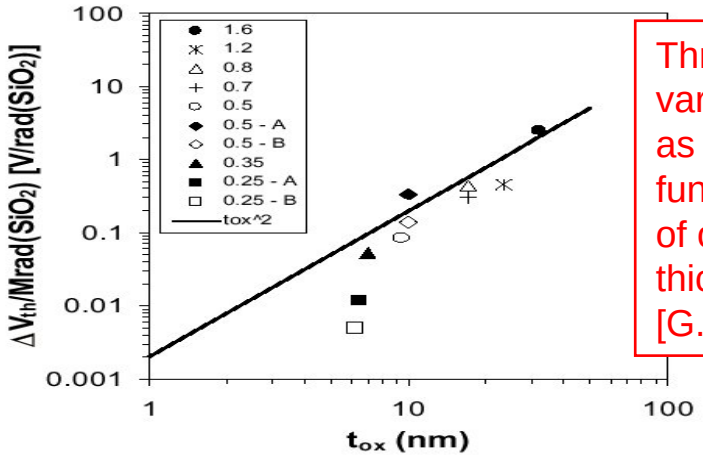
- **Reduction of dimensions**
  - « Quasi-constant voltage scaling »
  - Decrease of W,L,tox
  - (partial) decrease of V_{DD} et V_T



- **Improvement of speed in $1/L^2$**
  - Improvement of transconductance (as W/L) and reduction of cpacitors (as WL)



$$\frac{dV_{OUT}}{dt} = \frac{I_{DS0}}{C} \propto \frac{\frac{W}{L}}{WL} = \frac{1}{L^2}$$

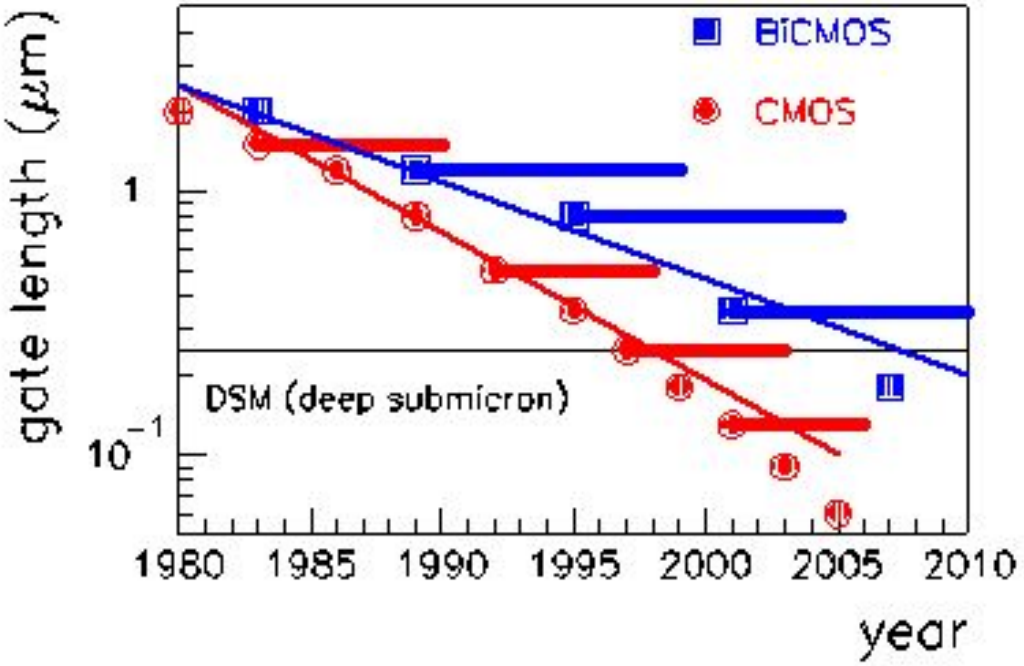


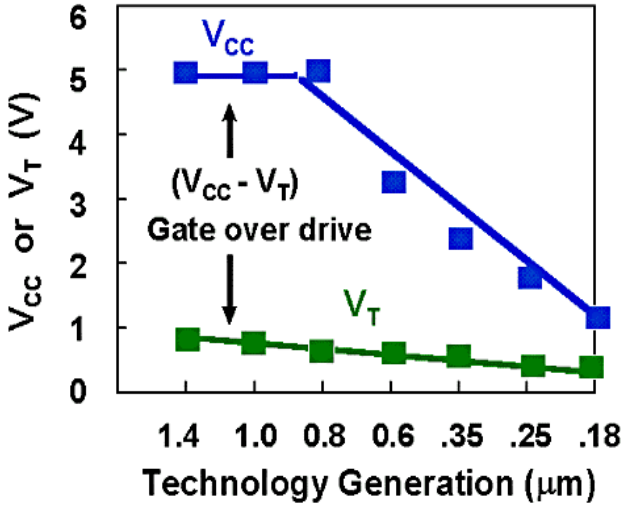
Threshold variation as a function of oxide thickness [G. Anelli]

- **Radiation hardness in bonus !**
  - Less trapping in gate oxide

Evolution of CMOS technologies (2)

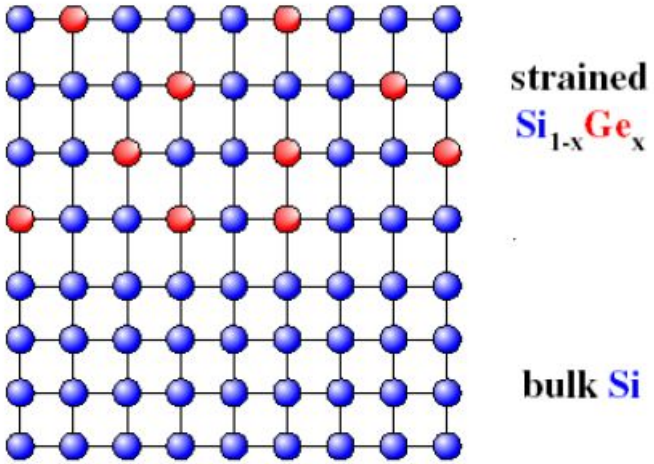
- **Differences between analog/mixed signall and digital technologies**
  - Very fast evolution of digital technologies (faster design migration)
  - More « perene » analog technologies (SiGe, BiCMOS…) (driven by mobile telecom and automotive)
  - A visible split occuring
- **More difficult analog design in low voltage**
  - « no more headroom for signals »

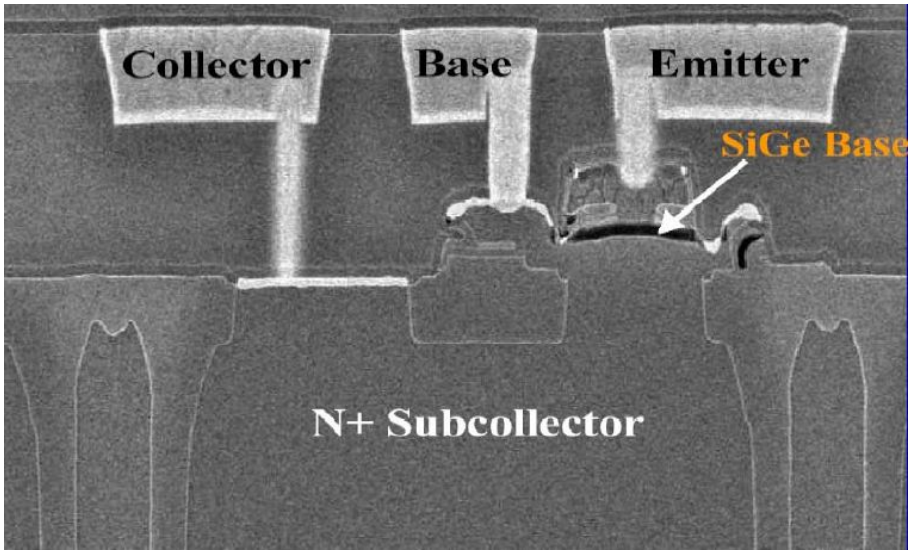


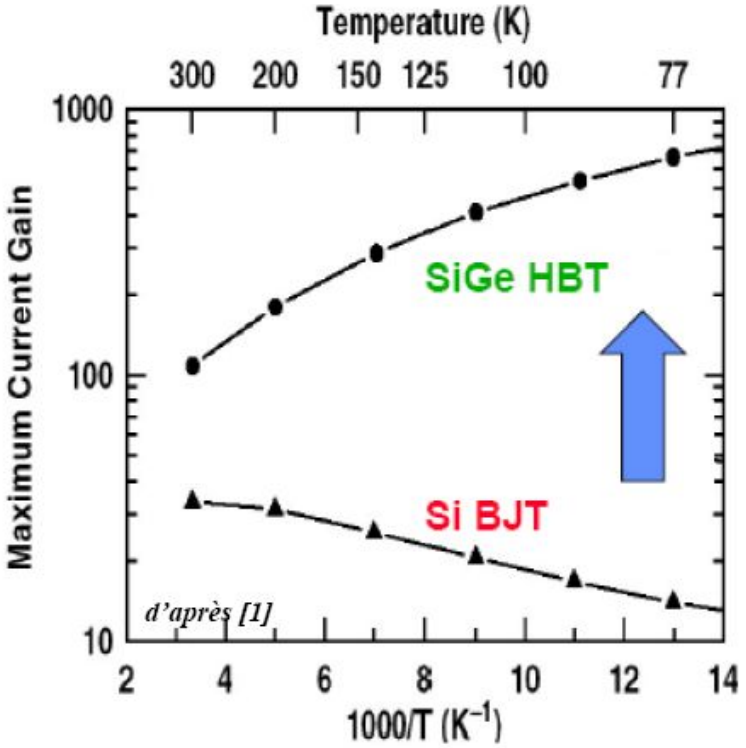


SiGe technology

- **Faster bipolar transistors for RF telecom**
  - Better mobility and FT
  - Better current gain (beta)
  - Better Early voltage
  - Interesting improvement at low T
  - Compact CMOS (0.25 or 0.35µm) for mixed-signal design

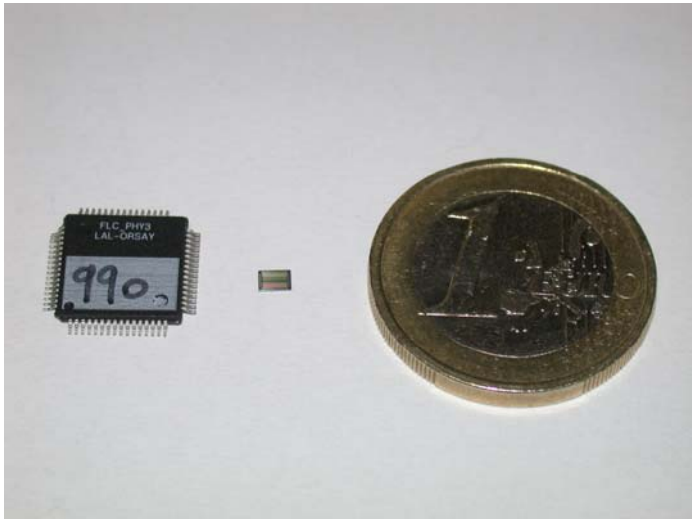






Cost of ASICs

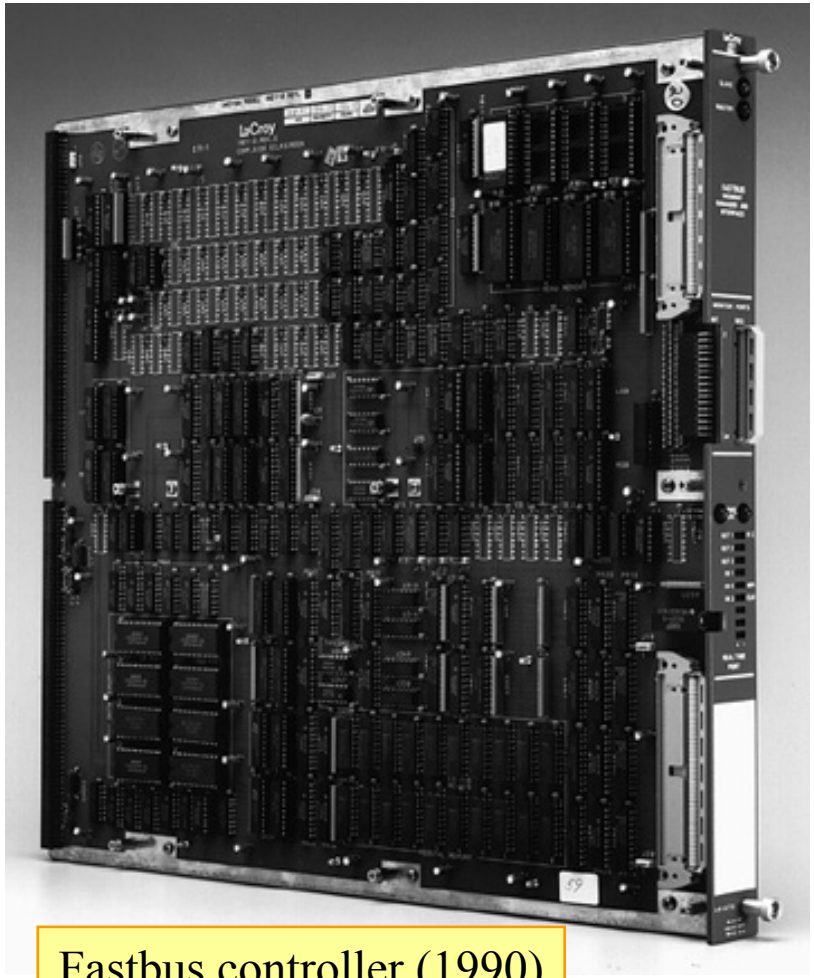
©K. Torki



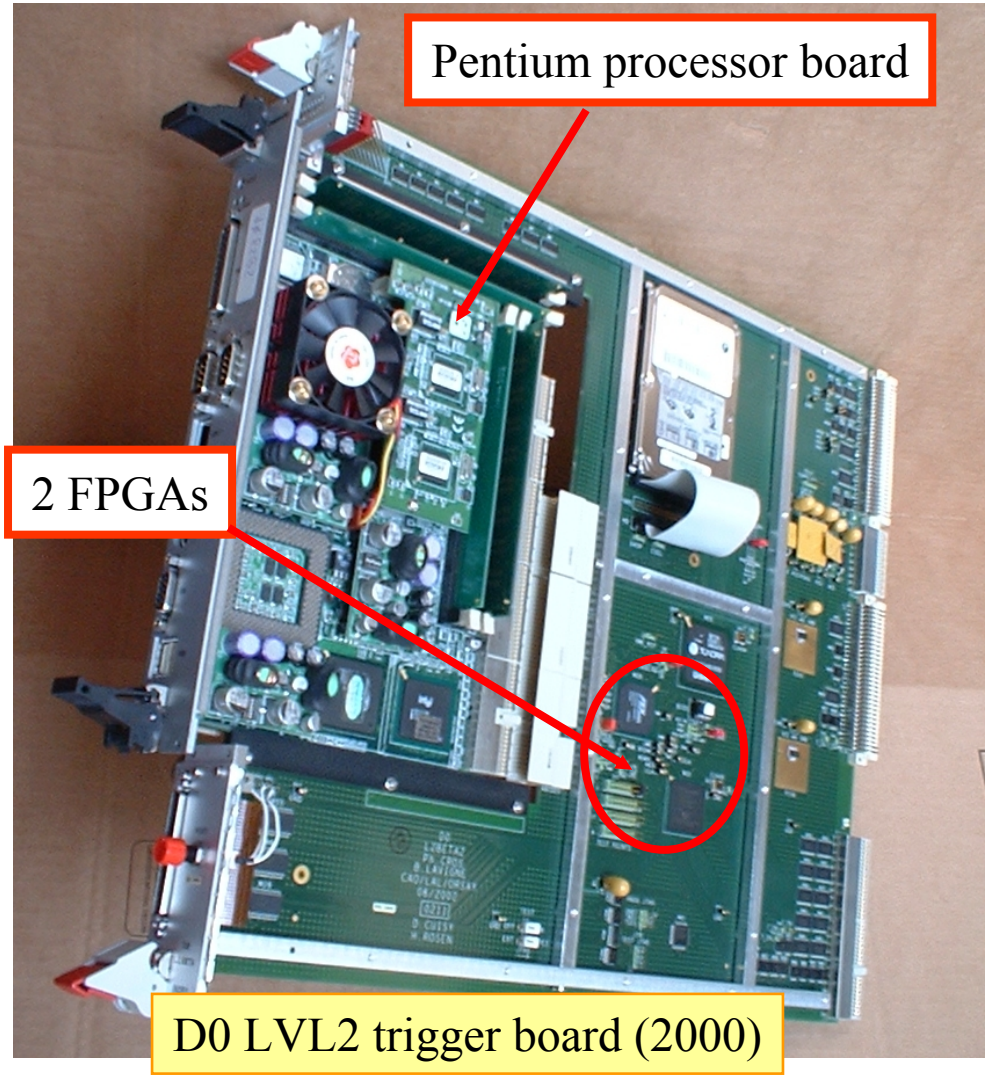
- **MPW (multi-project wafers)**
  - CMOS 0.35µm (AMS) : 650 €/mm2
  - BiCMOS SiGe 0.35 µm (AMS) : 900 €/mm2
  - CMOS 0.13µ (STm) : 2500 €/mm2
  - CMOS 90 nm (STm) : 5000 €/mm2
  - Usually a few 10 to 100 pieces in a MPW run
- **Production runs**
  - Masks : 91 k€ (CMOS 0.35µm)
  - 8" wafers : 4 k€, useful area : 25 000 mm2 = several thousands of chips
- **Packaging**
  - Ceramic : 20-30€/chip
  - Plastic : 2k€ + 1-2 €/chip
- **Example : chip 10mm2 16 channels**
  - 100 chips (MPW) : 120€/chip, 7€/channel
  - 10 000 chips (4wafers) : 12€/chip < 1€/channel

(R)evolution of digital electronics (1)

- From stacks of circuits to FPGAs : progammable gate arrays



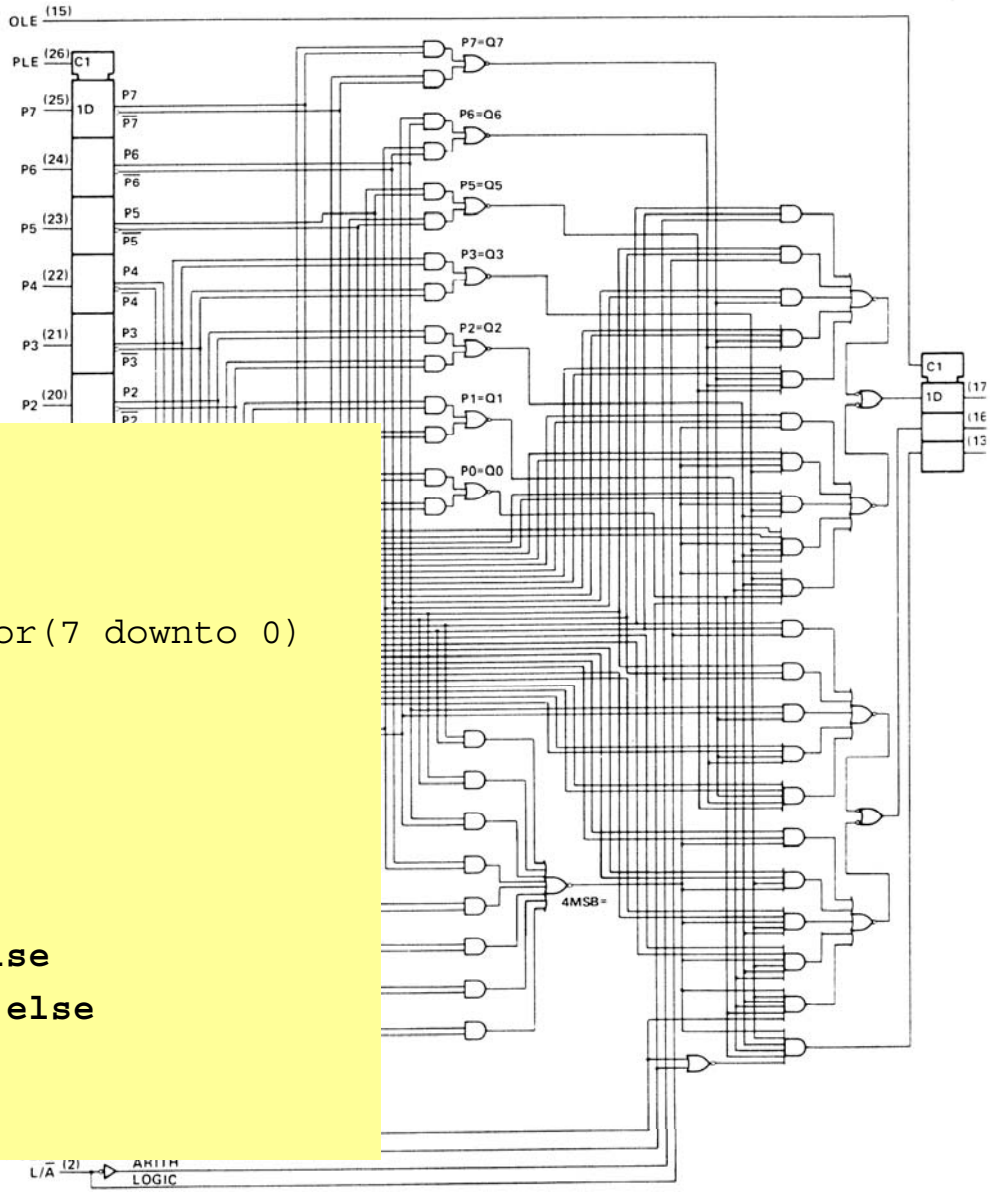
Fastbus controller (1990)



D0 LVL2 trigger board (2000)

Evolution of digital electronics (2)

- **Schematic -> High level languages** (Verilog, VHDL)
  - Example 8 bit comparator
  - 74LS866



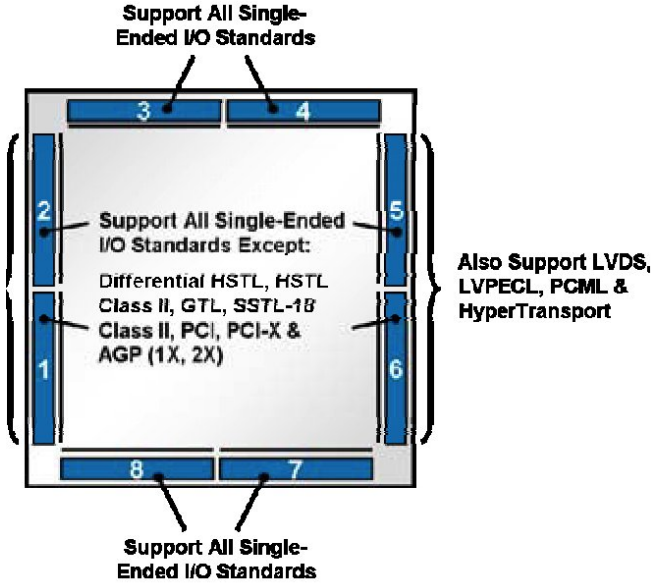
- **VHDL comparator :**

```
entity comparator_8 is
port (   raz : in std_logic;
         val1,val2 : in std_logic_vector(7 downto 0)
         result : out std_logic
       );
end entity comparator_8;
architecure archi_& of comparator_8 is
begin
   result <=      '0' when raz = '0' else
                  '1' when val1 > val2 else
                  '0'
end architecture archi_1;
```

(R)evolution of digital electronics (3)

- **Reduction of digital logic levels**
  - 1980 : TTL : 0-5 V
  - 2000 : LVDS : Low Voltage (± 400 mV) Differential Swing
  - Better signal integrity (EMC)
  - Reduction of power supplies 5V -> 3.3V -> 2.5V -> 1.2V

- **Components : the revolution of FPGAs :**
  - = Field Programmable Arrays (Altera©, Xilinx©)
  - 4-40 millions gates (55M in a Pentium4)
  - RISC 32bits processors
  - 10 Mbits resident memory
  - 2000 pins 1300 I/O (inputs/outputs)
  - 300 MHz operation



FPGAs as blackhole of digital electronics ?

©JP Cachemiche

RISC processors

IP standard interfaces (Ethernet, USB,PCI..)

Matching networks

Clocks & PLLs

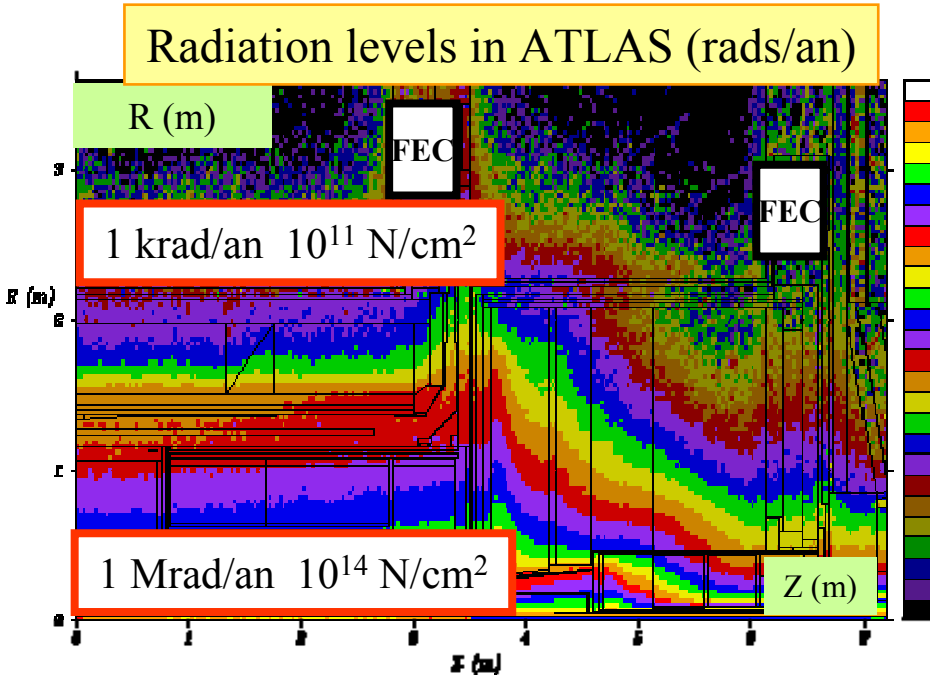
DSP blocks, arithmetics

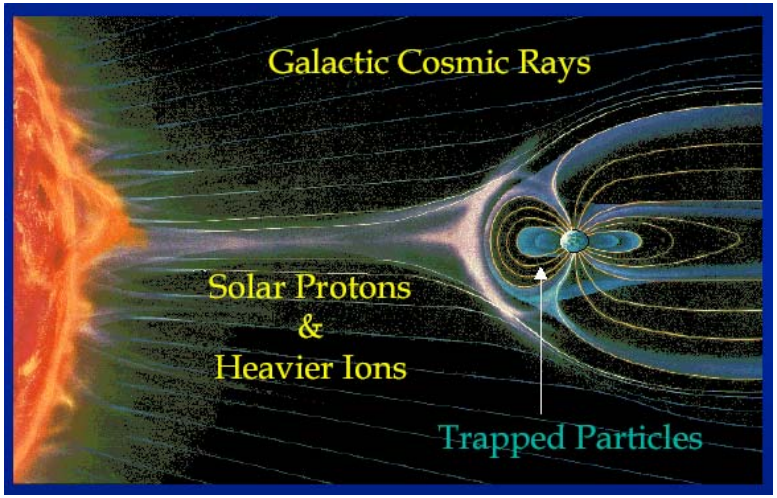
Memories & FIFOs

Bus interfaces (GTL, LVDS…)

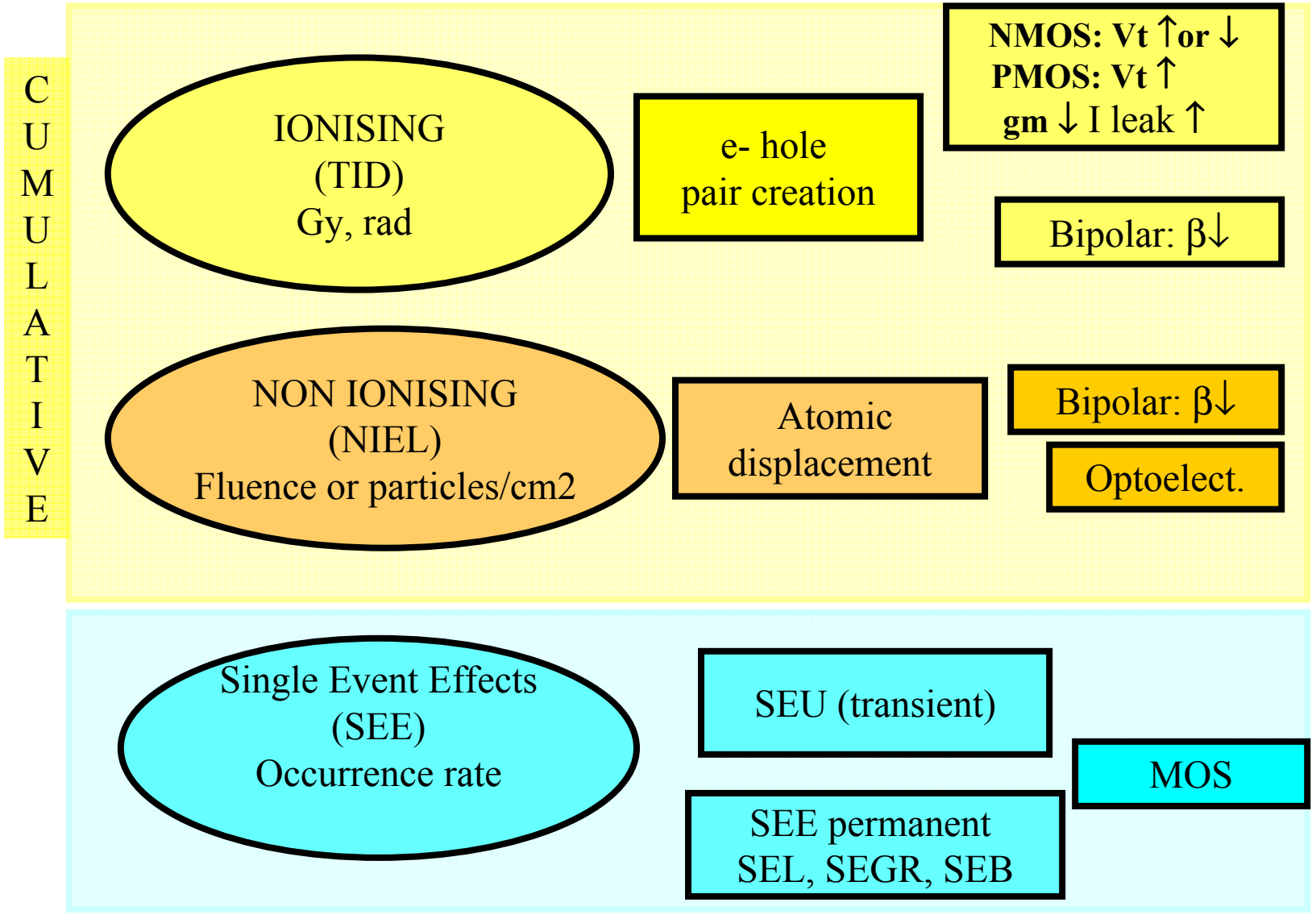
Effect of radiations on components

- **TID : total ionising dose effects**
  - Charge trapping in gate oxide
  - Alleviated in thin oxides (Deep SubMicron DSM)
  - Radiation tolerant layout techniques designed by CERN RD49 in 0.25µm
- **NIEL : non ionising energy loss**
  - Cristal damage with neutrons
  - Beta drop in bipolar transistors
- **SEU : Single Event Effect**
  - Effect of large ionising impact : local charge deposition on critical nodes
  - SEU : single event Upset = bit flip
  - SEL : single Event Latchup : thyristor setting -> destructive !





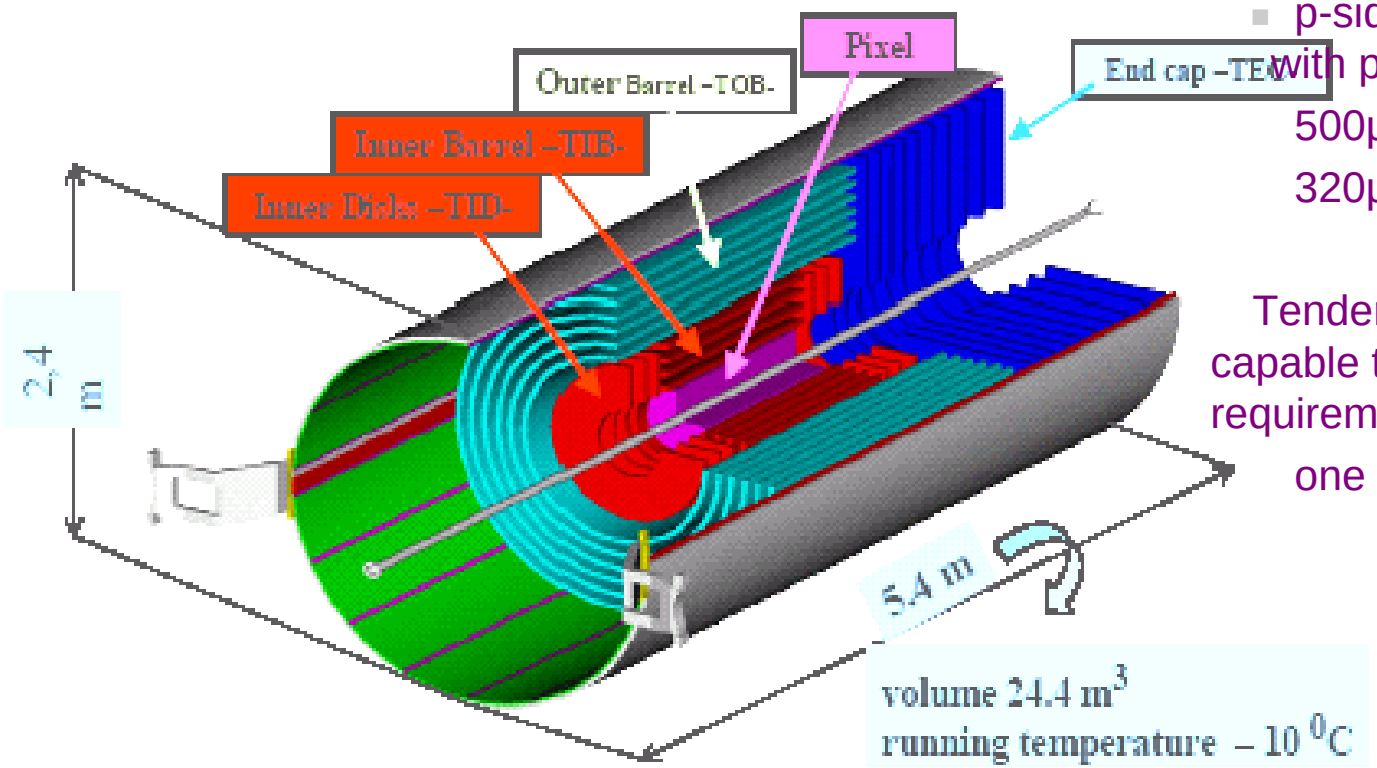
Summary of radiation effects on components



[N. Seguin-Moreau Cargèse 2004]

Silicon Tracker

- **Main sub-systems: Microstrip Tracker and Pixel Detector**
  - Microstrip Tracker comprises 3 (topological) regions
  - ~210 m^2 of silicon, 10M channels
  - 75000 FE chips, 40000 optical links



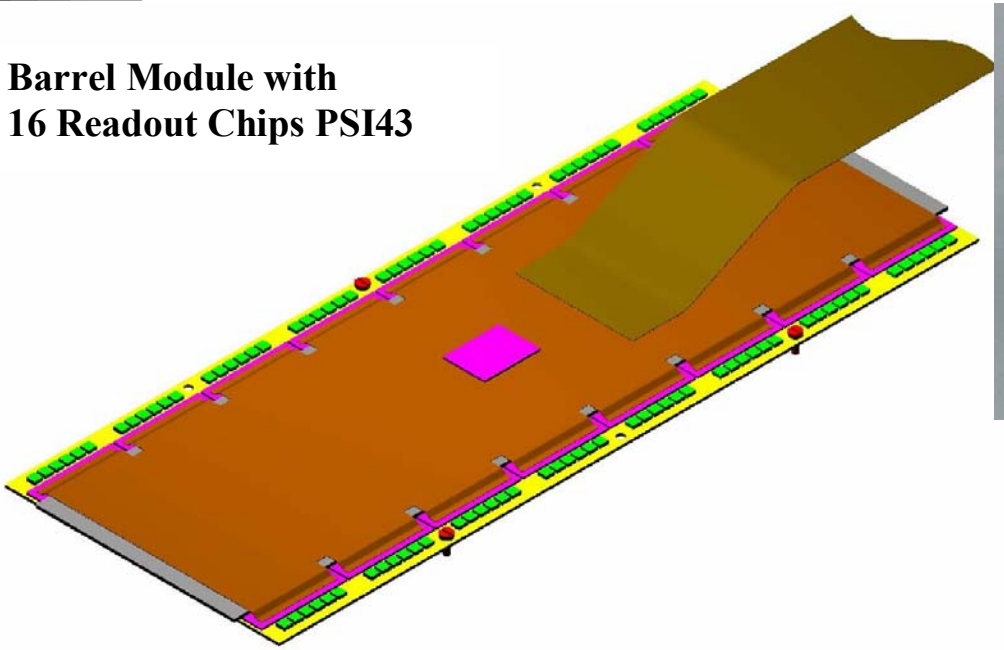
- Silicon sensors
  - p-side readout, AC coupled, with poly-Si bias resistors
    - 500µm 19100 units, 8 designs
    - 320µm 6450 units, 8 designs

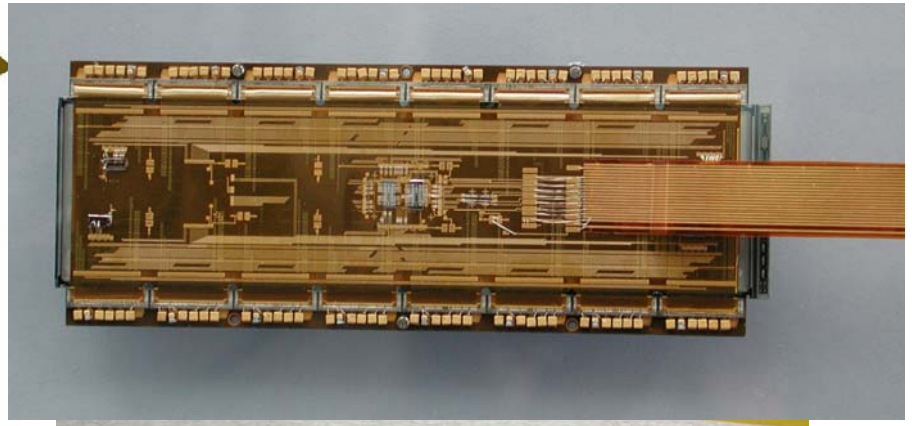
Tender required companies capable to deliver >50% of requirement

one succeeded…

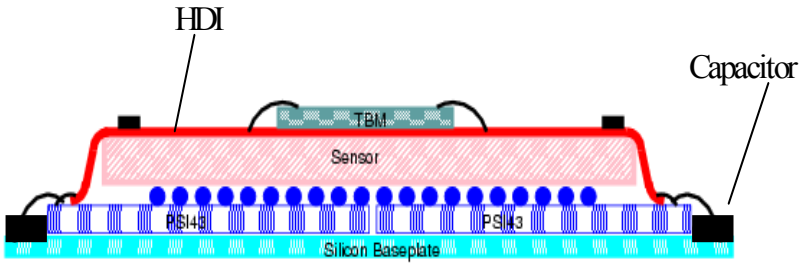
CMS Pixels

Barrel Module with
16 Readout Chips PSI43





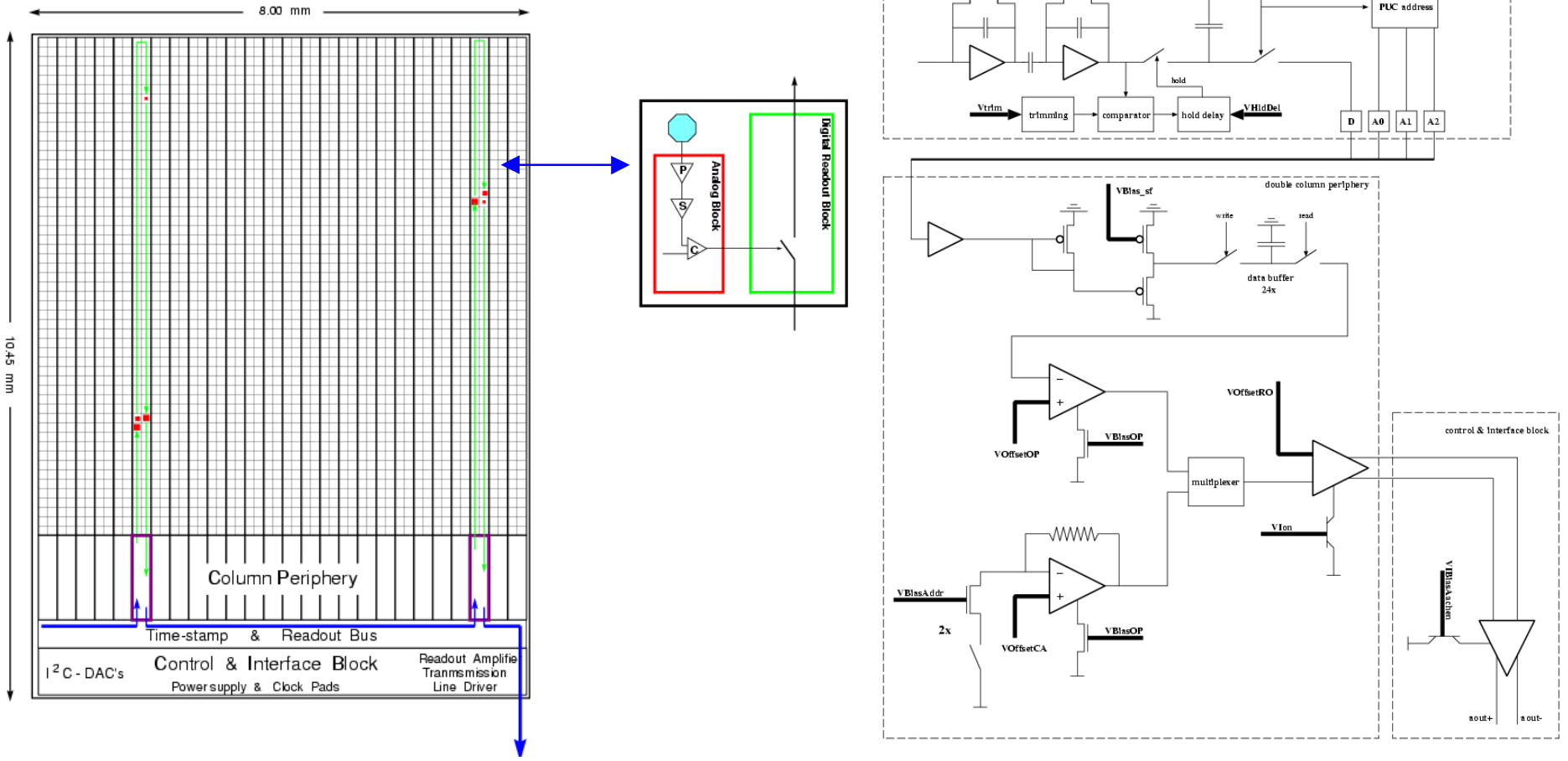
Layer	Radius [mm]	# Modules	Area [m^2]	Fluence [MHz/cm^2]
1	41-45	128	0.15	25
2	70-74	224	0.25	13
3	107-112	352	0.38	8



CMS pixel readout chip

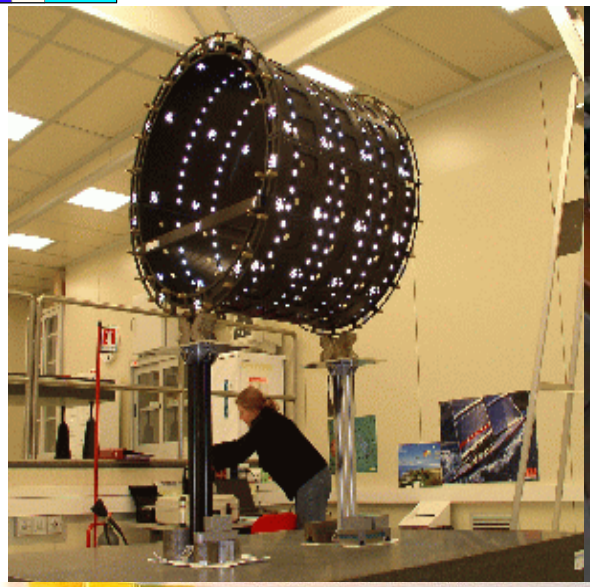
- 52 x 53 pixels, organised in 26 double column
- Pixel size: 150 x 150µm
- Column Drain Architecture

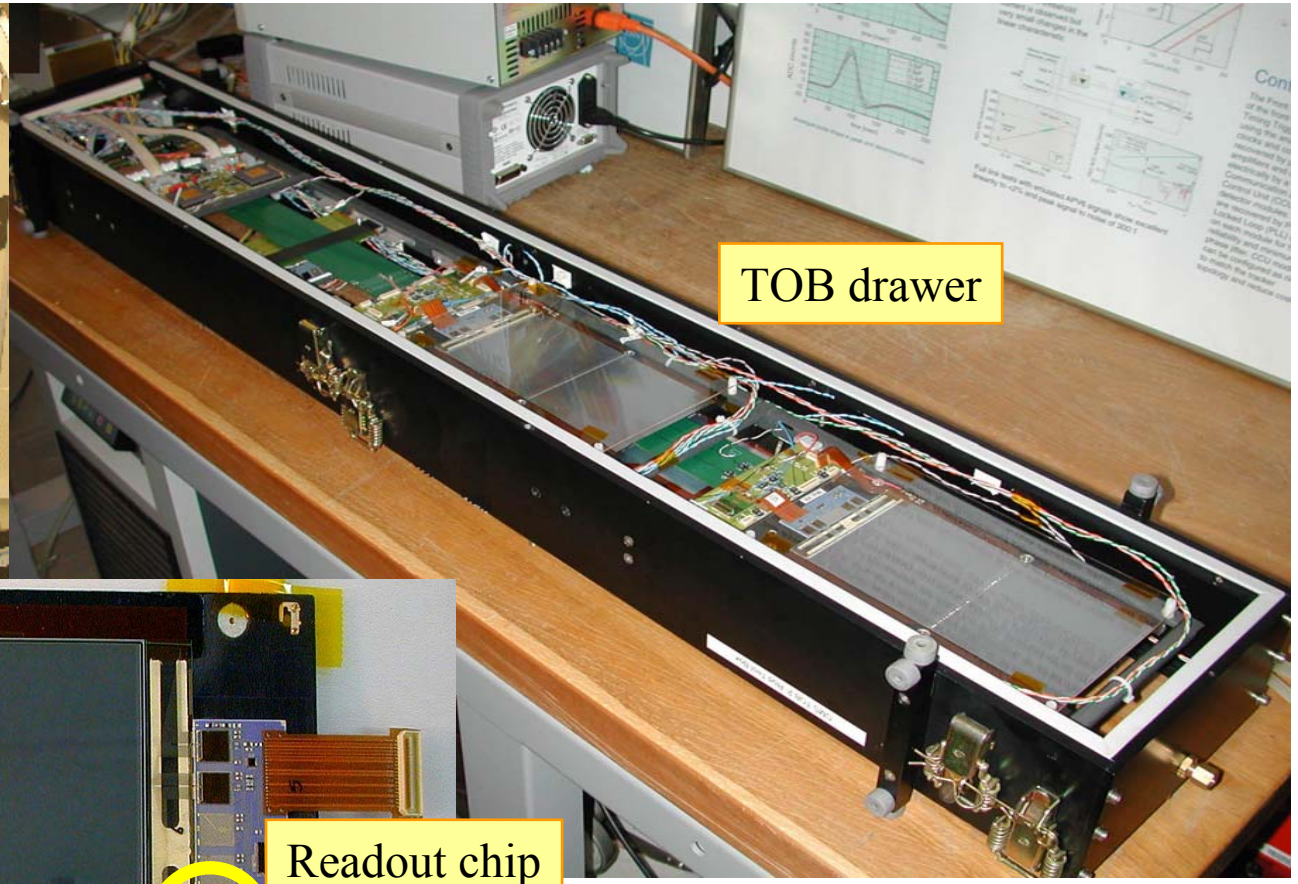
- 2 stage preamp with adjustable feedback
- adjustable comparator threshold, global and local trim
- sample/hold with programmable hold delay
- adjustable range and scale of pixel address and double column address

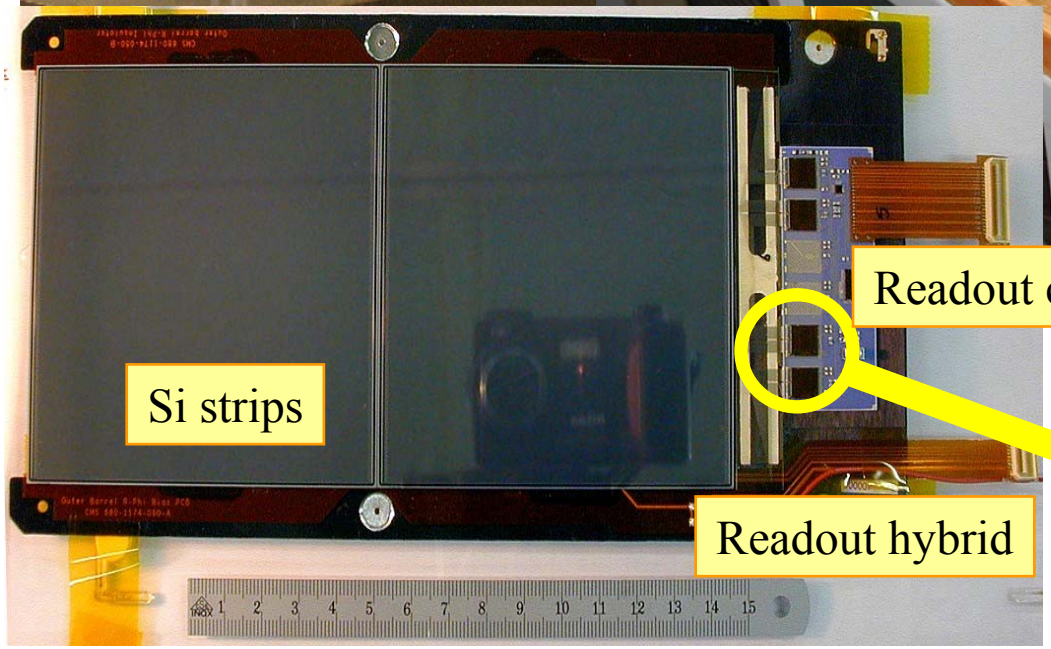


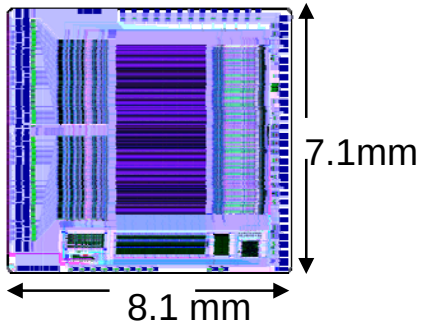
CMS micro strips

[U. Goerlach LEB8 Colmar 02]

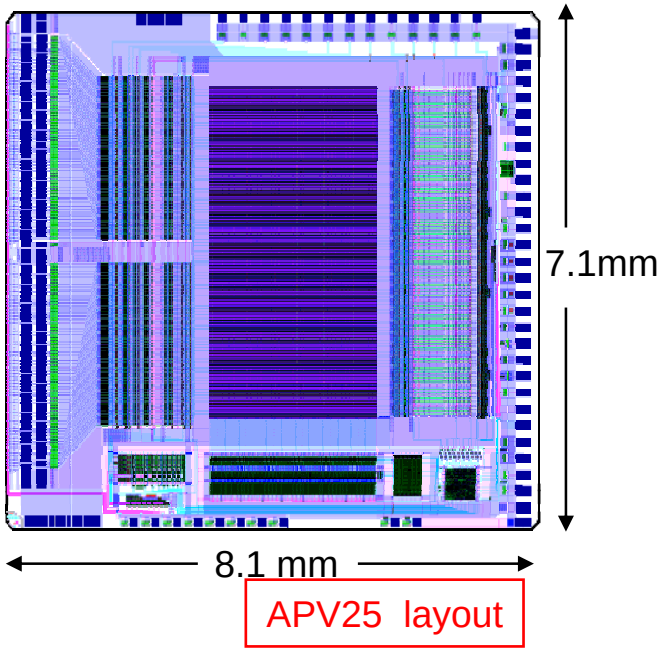








CMS strip readout ASIC : APV25



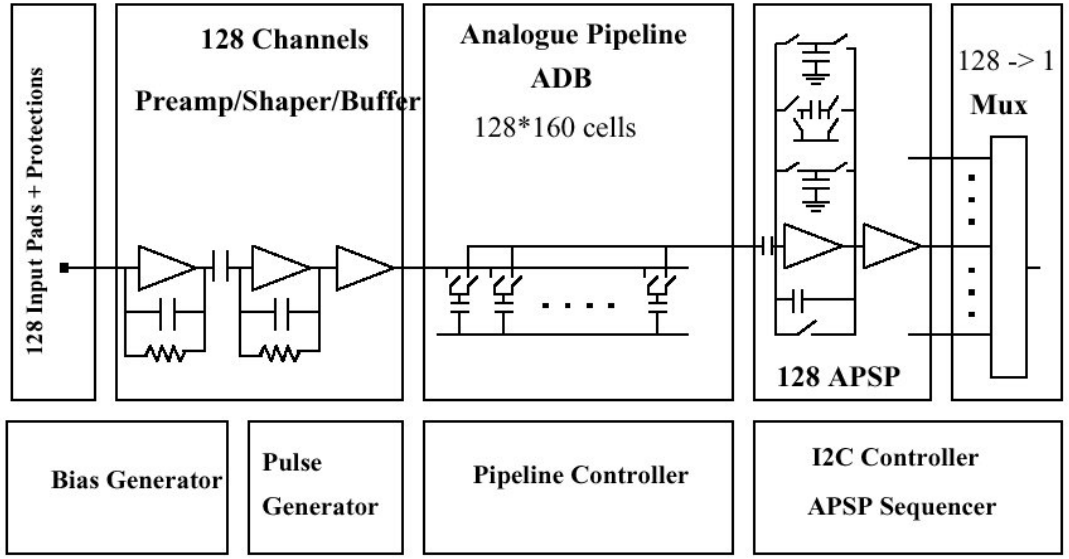
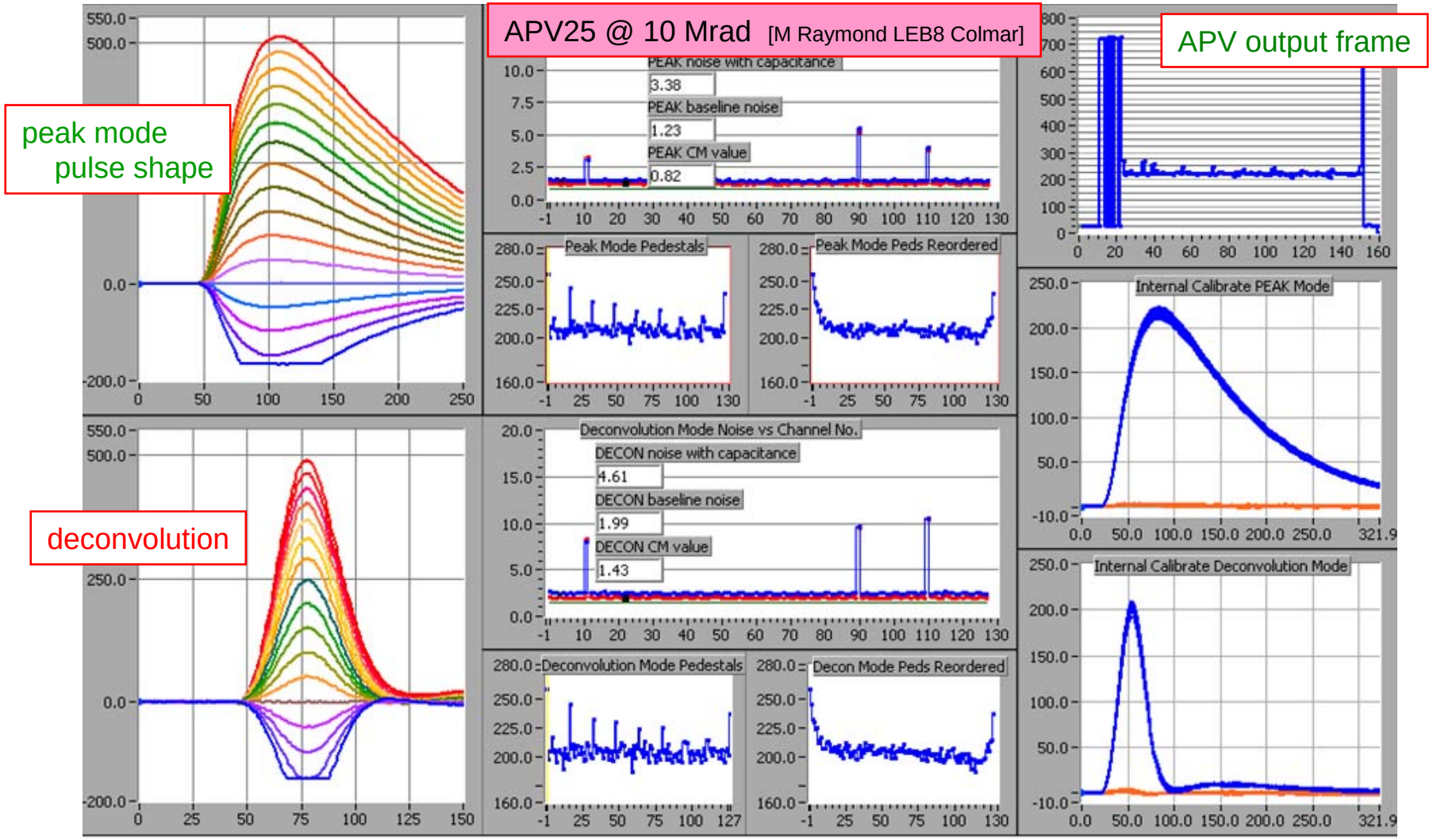


Fig. 1. APVD block diagram.

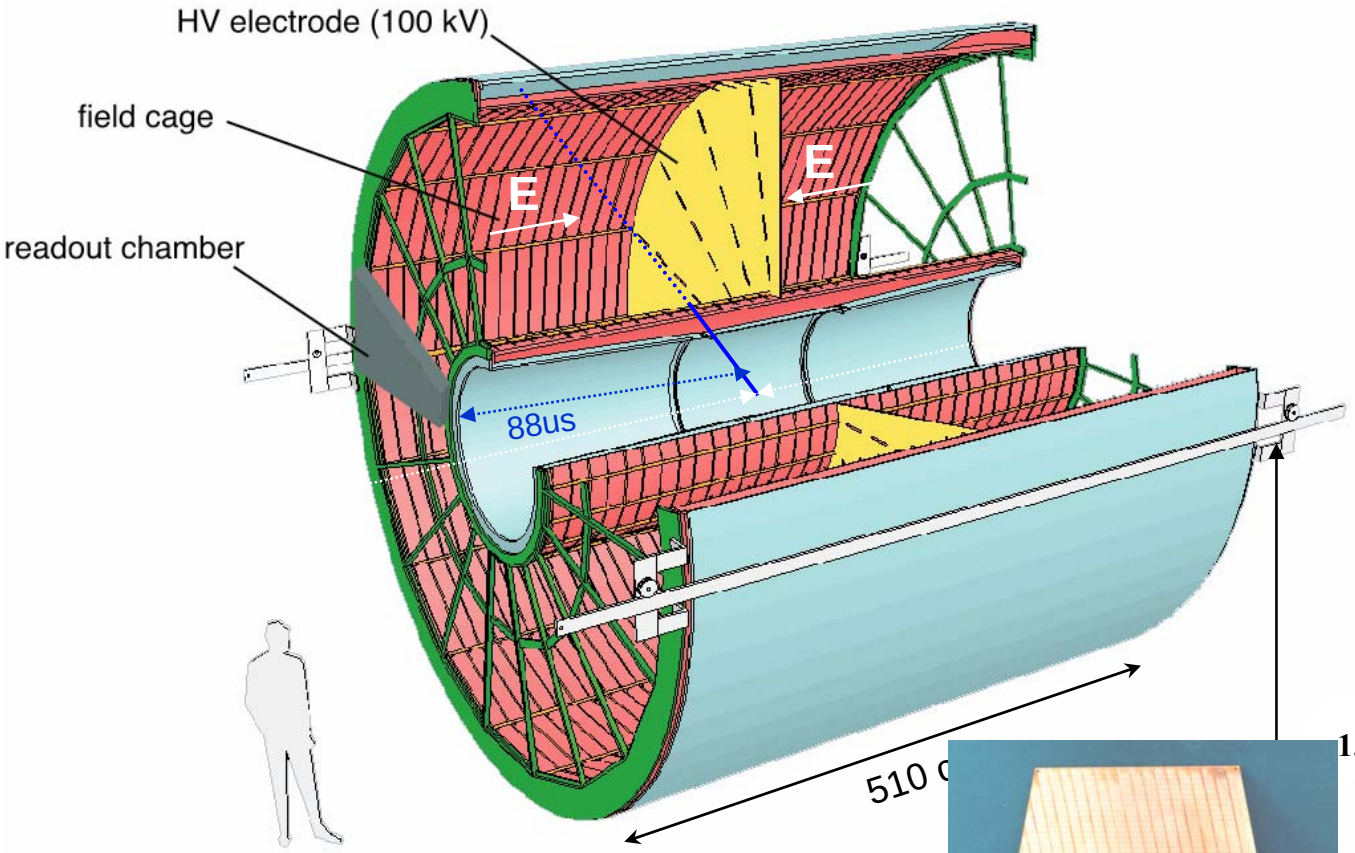
- **Very high level of integration**
  - 128 preamps/shapers, 128*160 analog pipelines
  - Mode peak & déconvolution, multiplexe'd output, internal calibration …
- **Performance**
  - Dynamic range ±13 MIP, low dissipation (2μW/ch), Low noise : ~200e-
- **Rad hard design**
  - 0.25μ technology, withstands 50 Mrads

APV25 performance

[M Raymond LEB8 Colmar 02]

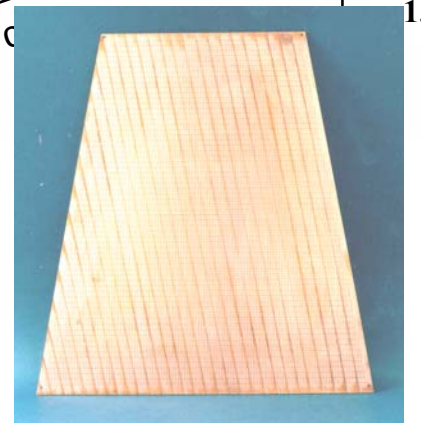


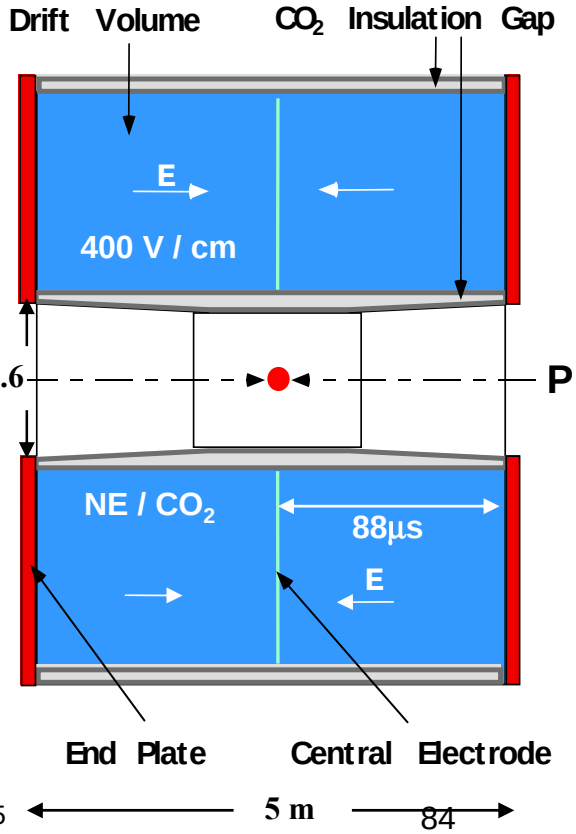
Gazeous detectors : ALICE TPC layout



GAS VOLUME
88 m^3

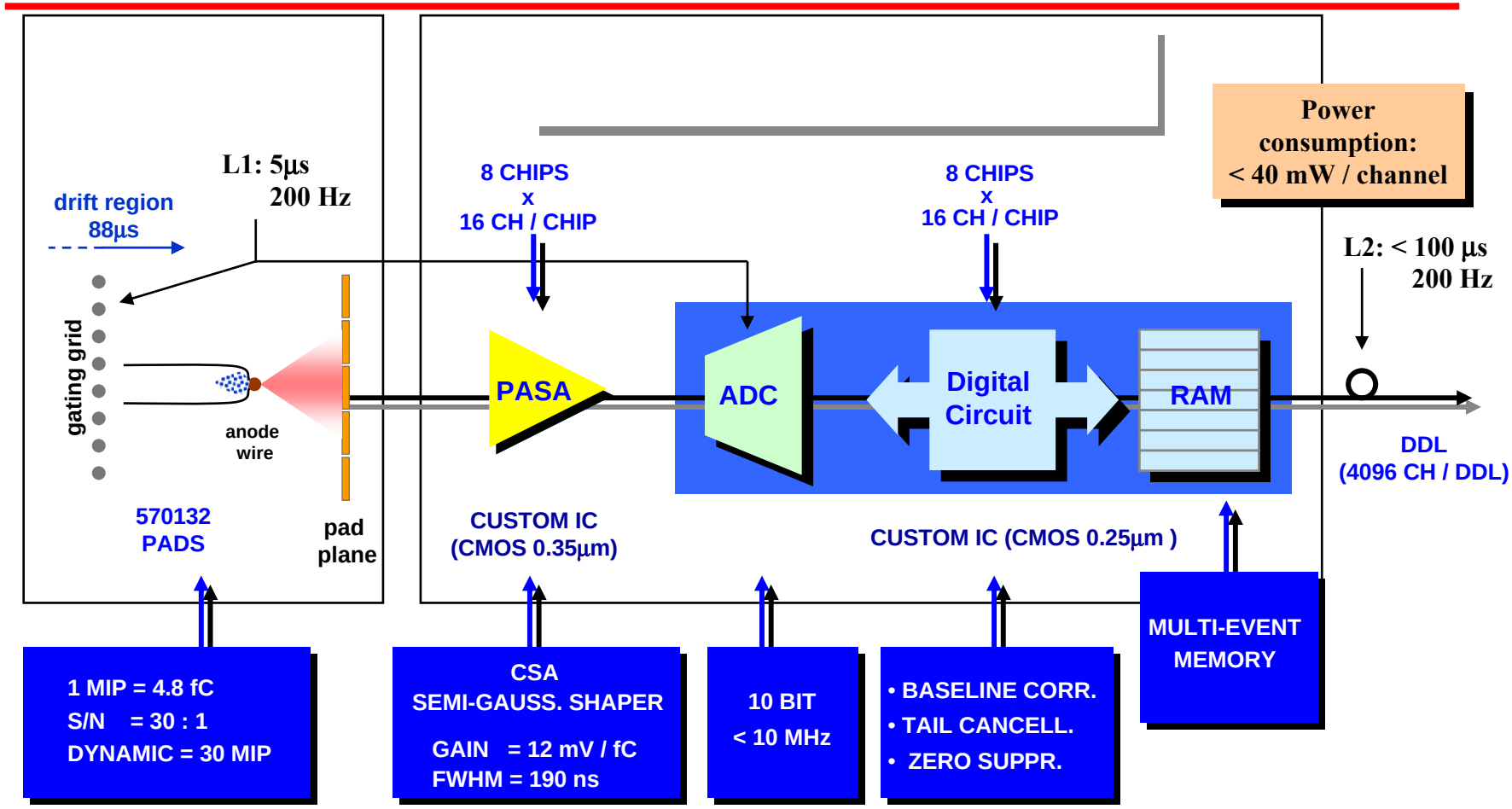
DRIFT GAS
0% Ne - 10%CO_2





Readout plane segmentation
18 trapezoidal sectors
each covering 20 degrees in azimuth

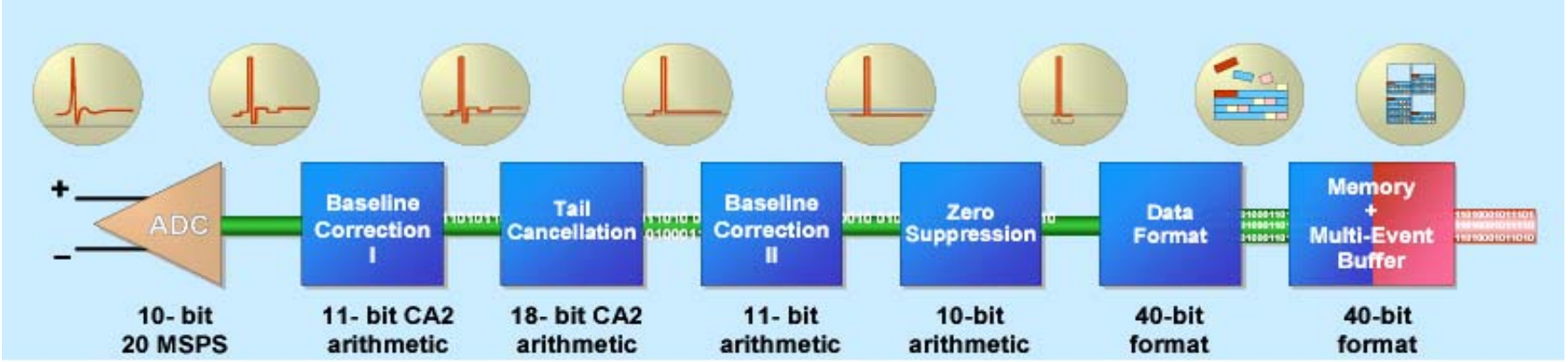
TPC: Electronics



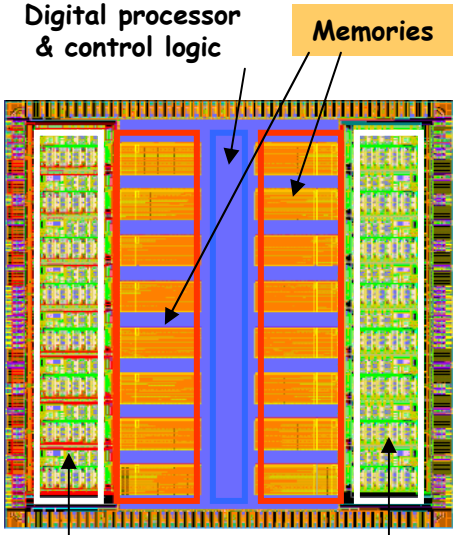
- **ALTRO: commercial ADC integrated with custom digital chip**
  - 0.25 micron technology (ST), 64 mm^2, 29 mW/ch, SEU protection

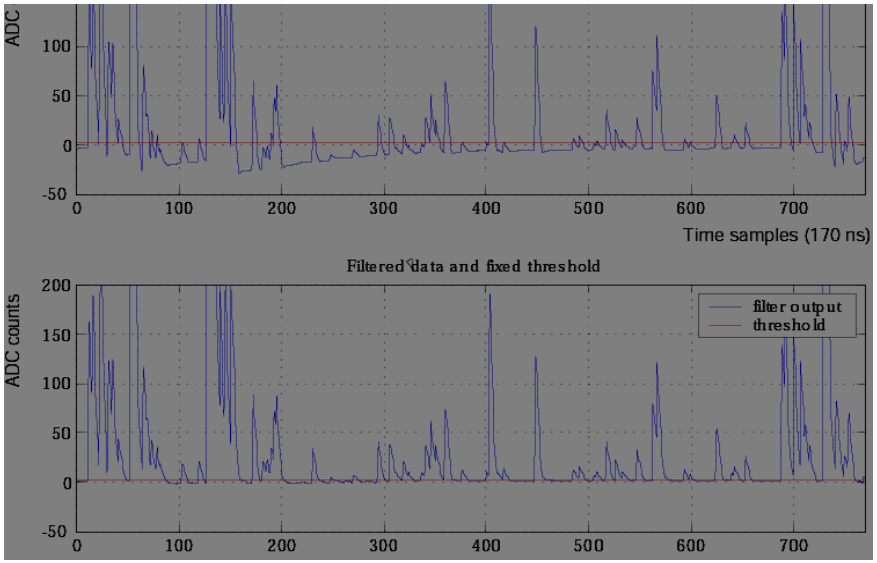
ALTRO chip ALICE TPC

[P. Jarron LEB8 Colmar 02]



- 8-ch ALTRO readout chip
  - 64 mm², 29mW/ch

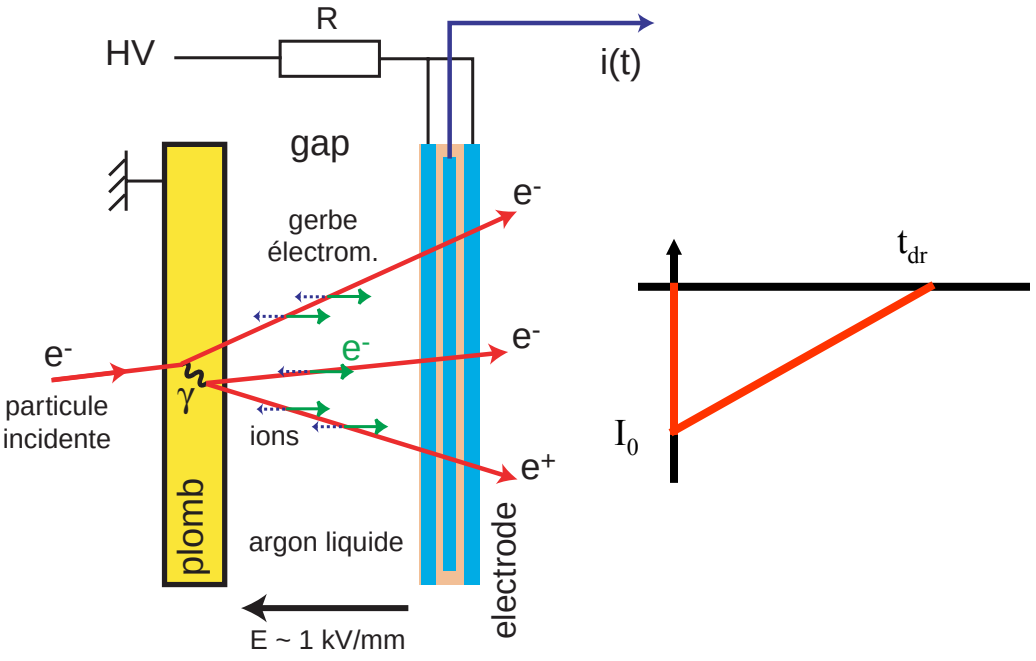


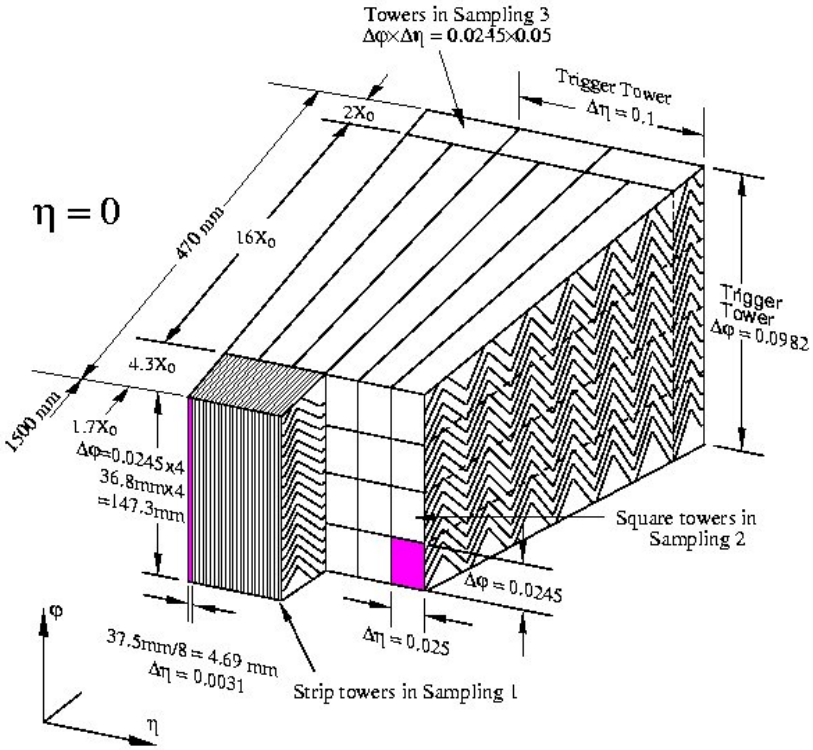


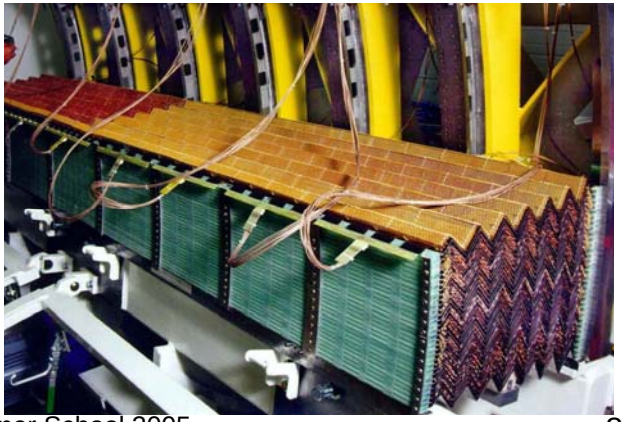
After L. Musa/CERN

ATLAS : LAr e.m. calorimeter [11]

- **Liquid argon « accordion » calorimeter**
- **Energy resolution : $10\%/\sqrt{E} \oplus 0.7\%$**
- **Segmentation : PS, Frt, Mid, Back**
  - Capacitance : 200 pF – 2 nF
- **Triangular ionisation signal**
  - I_0 = 2.5 $\mu A/GeV$ t_{dr}= 450 ns
  - I_0 proportionnal to particle energy



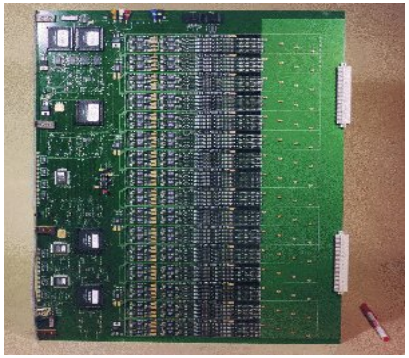


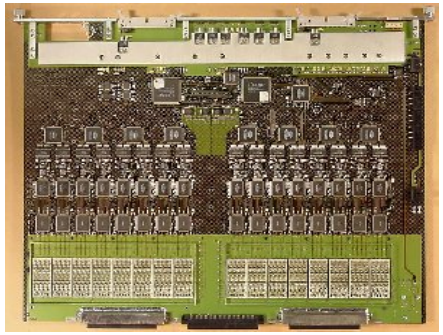


ATLAS Lar calorimeter readout

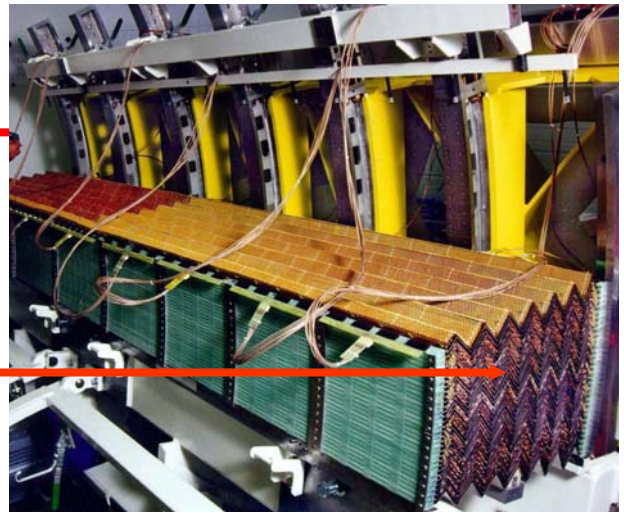
Calibration :
116 boards @ 128 ch

Front End Board (FEB) :
1524 boards @ 128 ch





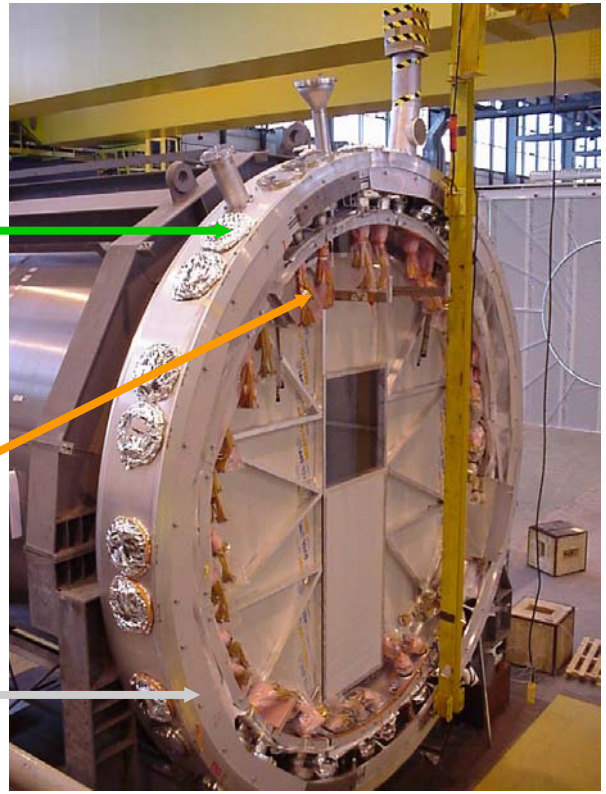
Electrodes



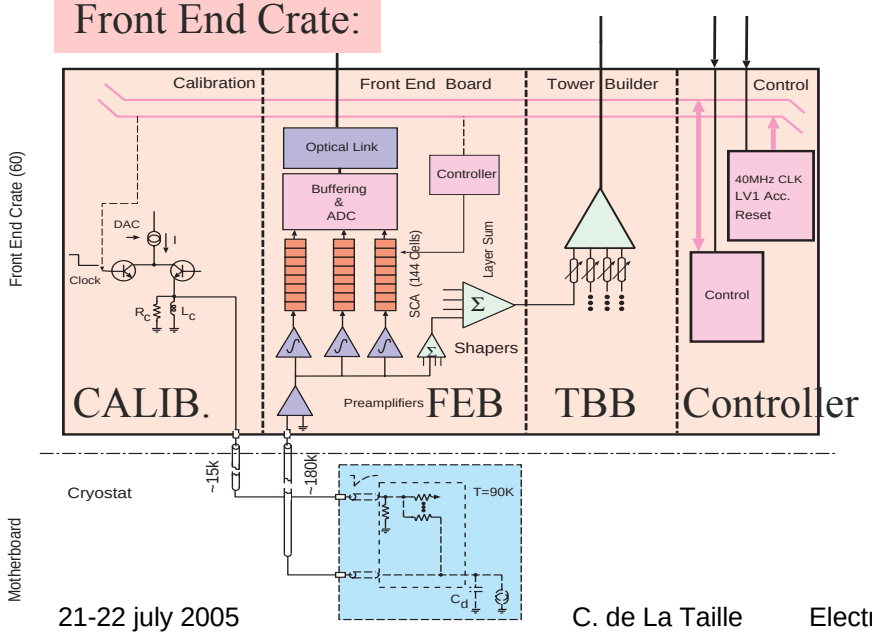
Cold to warm Feedthrough

Readout and Calib. signals

Cryostat

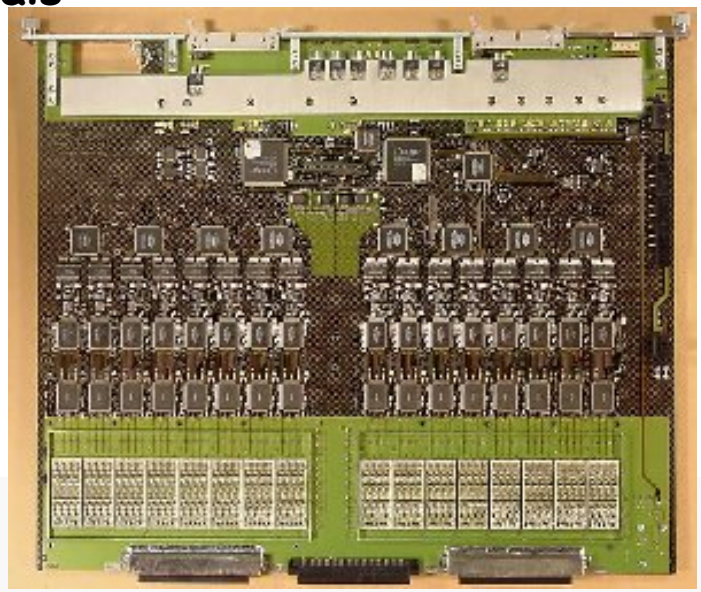


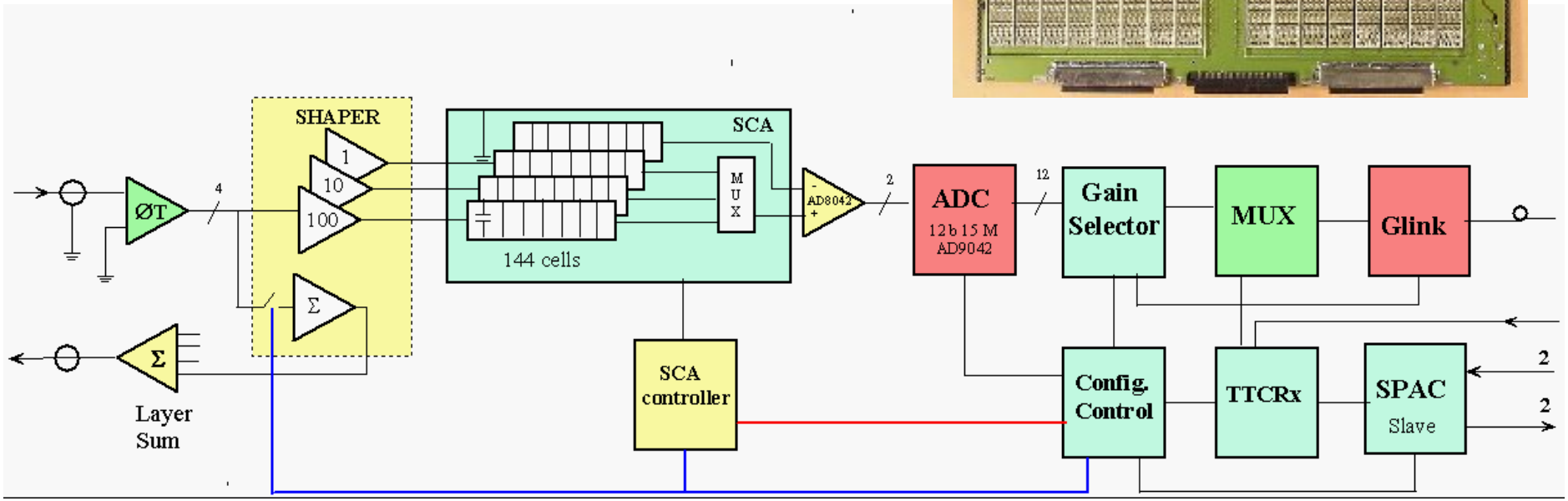
Front End Crate:



ATLAS LAr : Front End boards

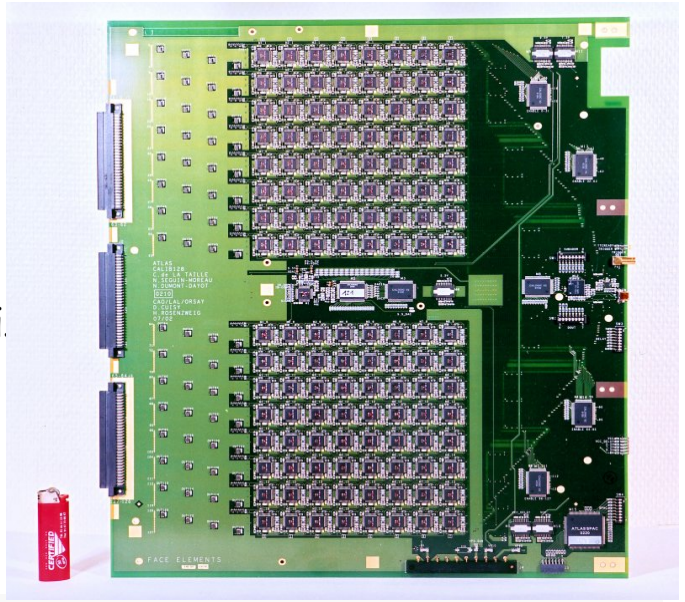
- **Amplify, shape, store and digitize Lar signals**
  - 16 bits dynamic range current preamps
  - Trigain (1-10-100) CRRC^2 shapers
  - 12 bits R/W analog memories
  - 10 different ASICs rad hard…

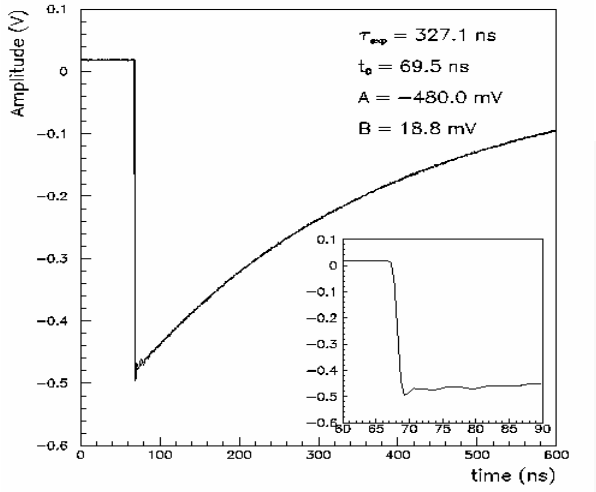


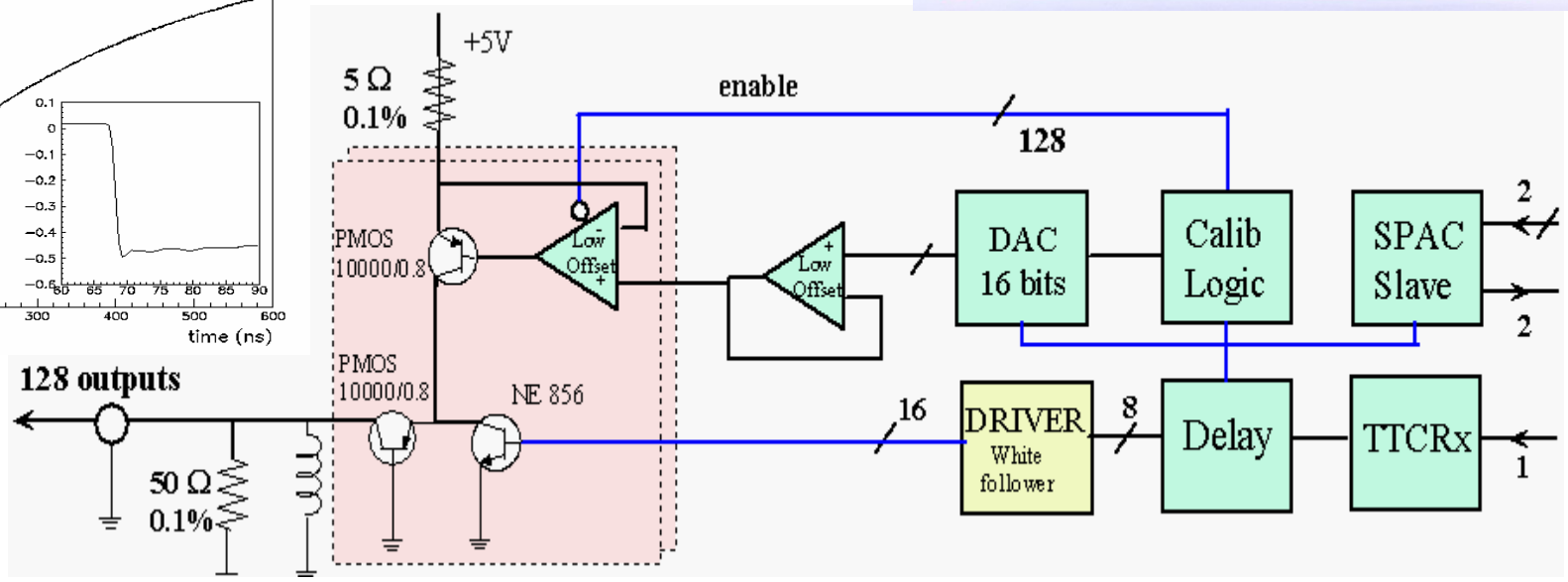


ATLAS LAr : calibration

- **Generate 0.2% accuracy calibration pulses**
  - 16 bits dynamic range : 50 μV – 5 V pulse
  - 1 ns risetime, 400 ns fall time
  - 0.1 % linearity
  - Injected inside LAr with 0.1% precision 1 kΩ resi

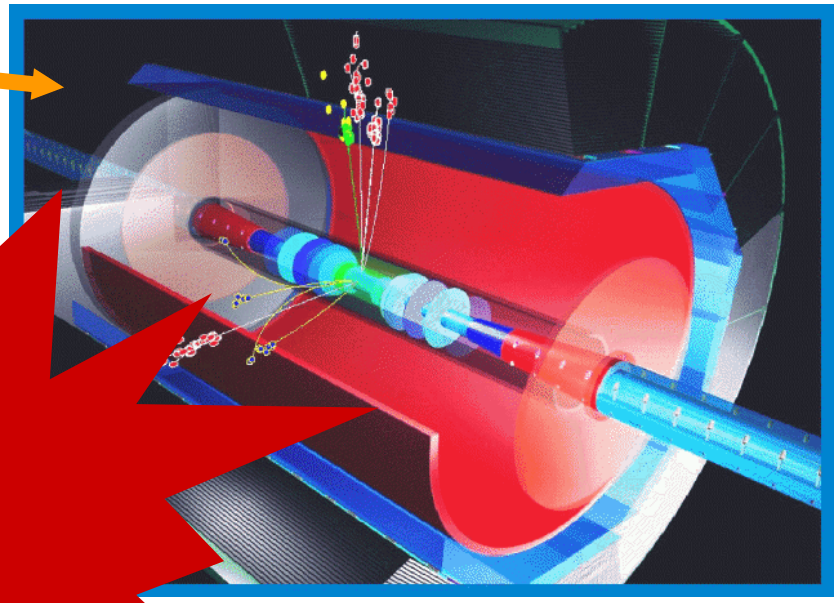




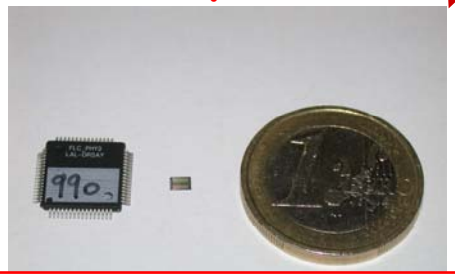


Future : ILC challenges for electronics

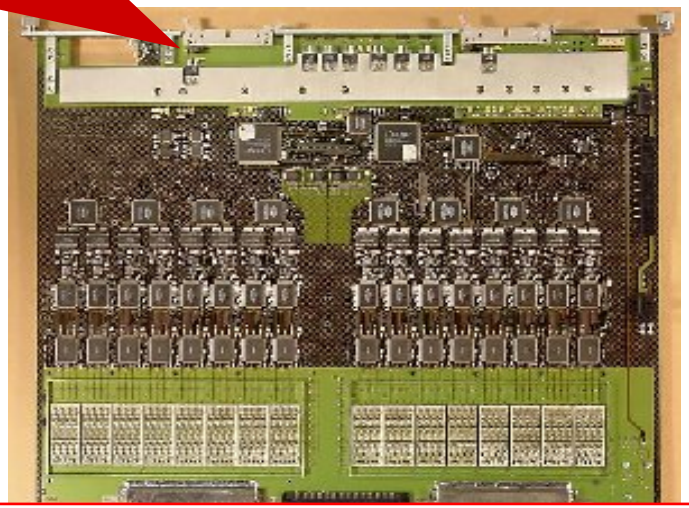
- **CALICE = W-Si Calorimeter**
  - Precision measurements : ~10%/√E
    - good linearity (‰ level)
    - Good inter-calibration (% level)
    - Low crosstalk (‰ level)
  - Large dynamic range (
    - 0.1 MIP -> 2 500 MIP
  - Auto-trigger on MIP
    - Low noise <<
  - Hermeticity : no roo
    - High leve
    - **Ultra-low pow**
  - 30 Mchannels
- **« Tracker electronics
  calorimetric performan »**



Ultra-low POWER is the KEY issue



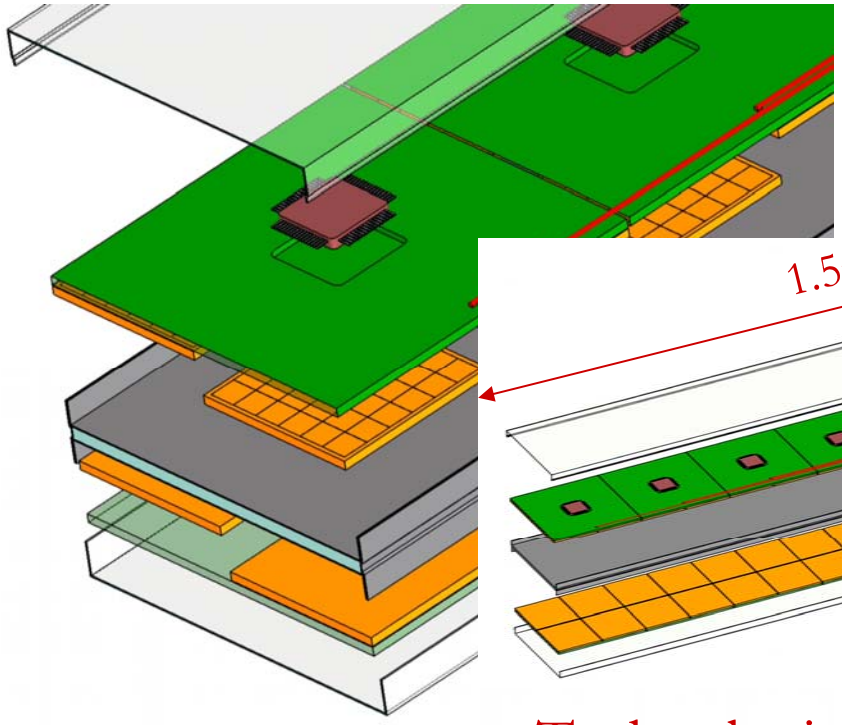
FLC_PHY3 18ch 10*10mm **5mW/ch**

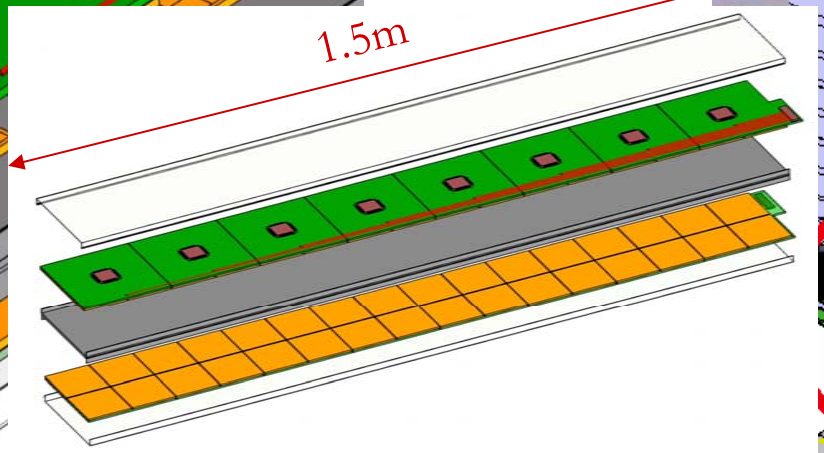


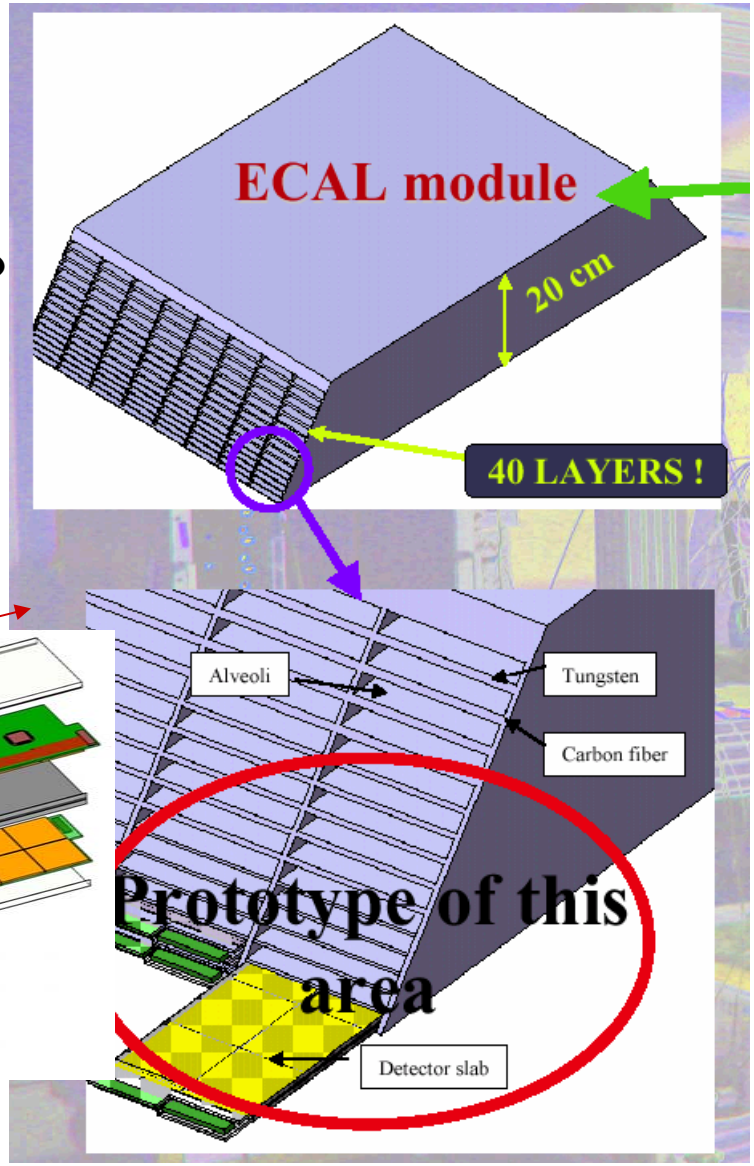
ATLAS LAr FEB 128ch 400*500mm **1 W/ch**

Future : calorimetry at ILC (201?)

- **Front-end ASICs embedded in detector**
- **All communications via edge**
  - 4,000 ch/slab, minimal room, access, power
  - Keep hermeticity
- **Data out (~Mbyte/s/slab) : optical, wireless ?**

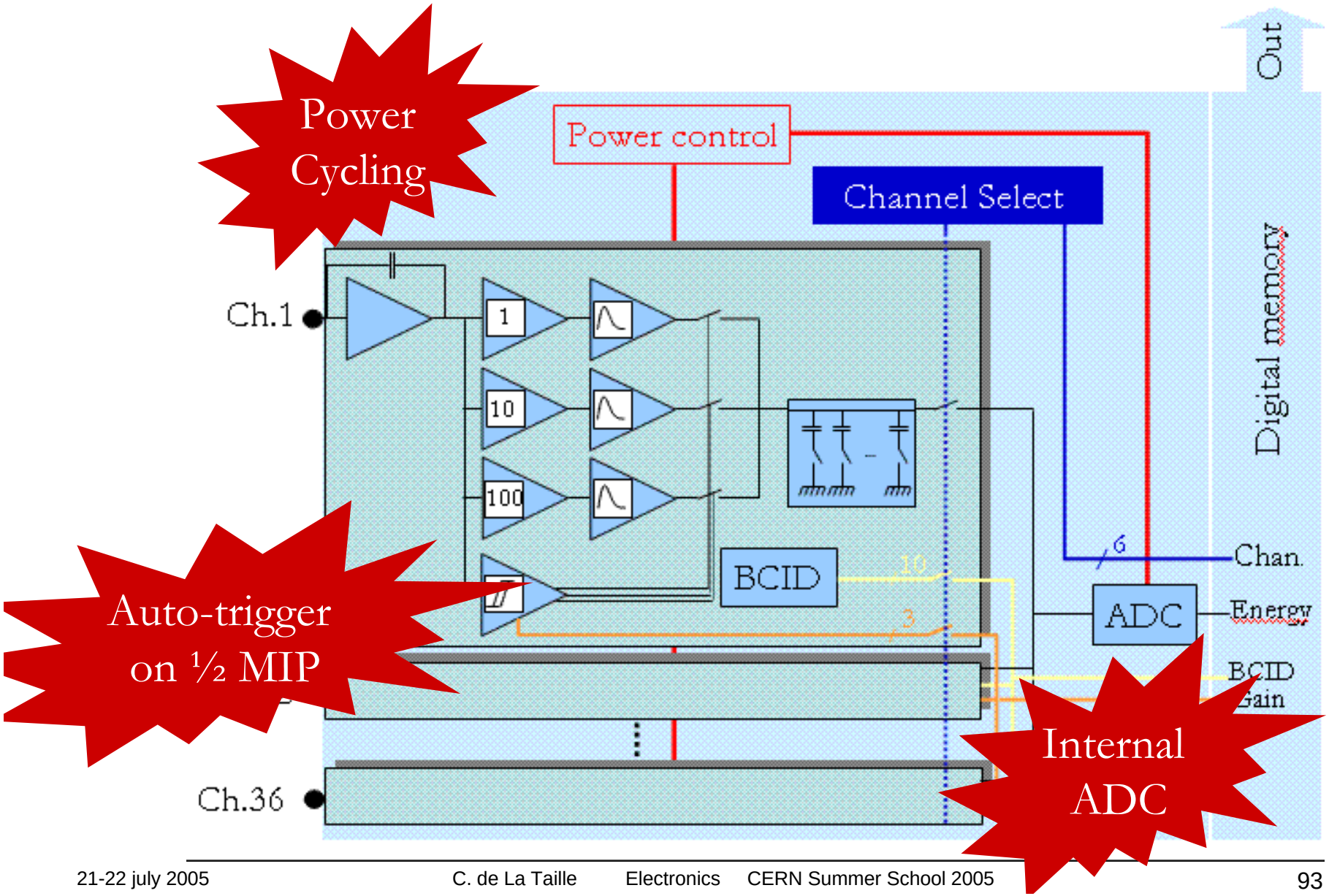






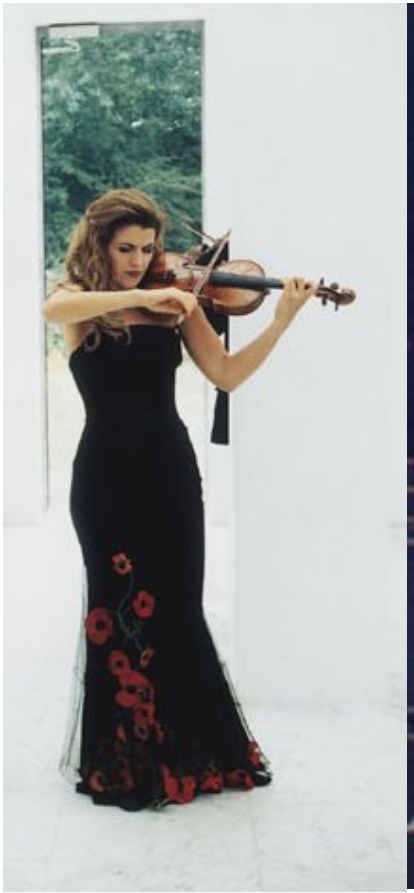
Technologic prototype

CALICE ECAL Front-End ASIC



Electromagnetic compatibility (EMC-EMI)

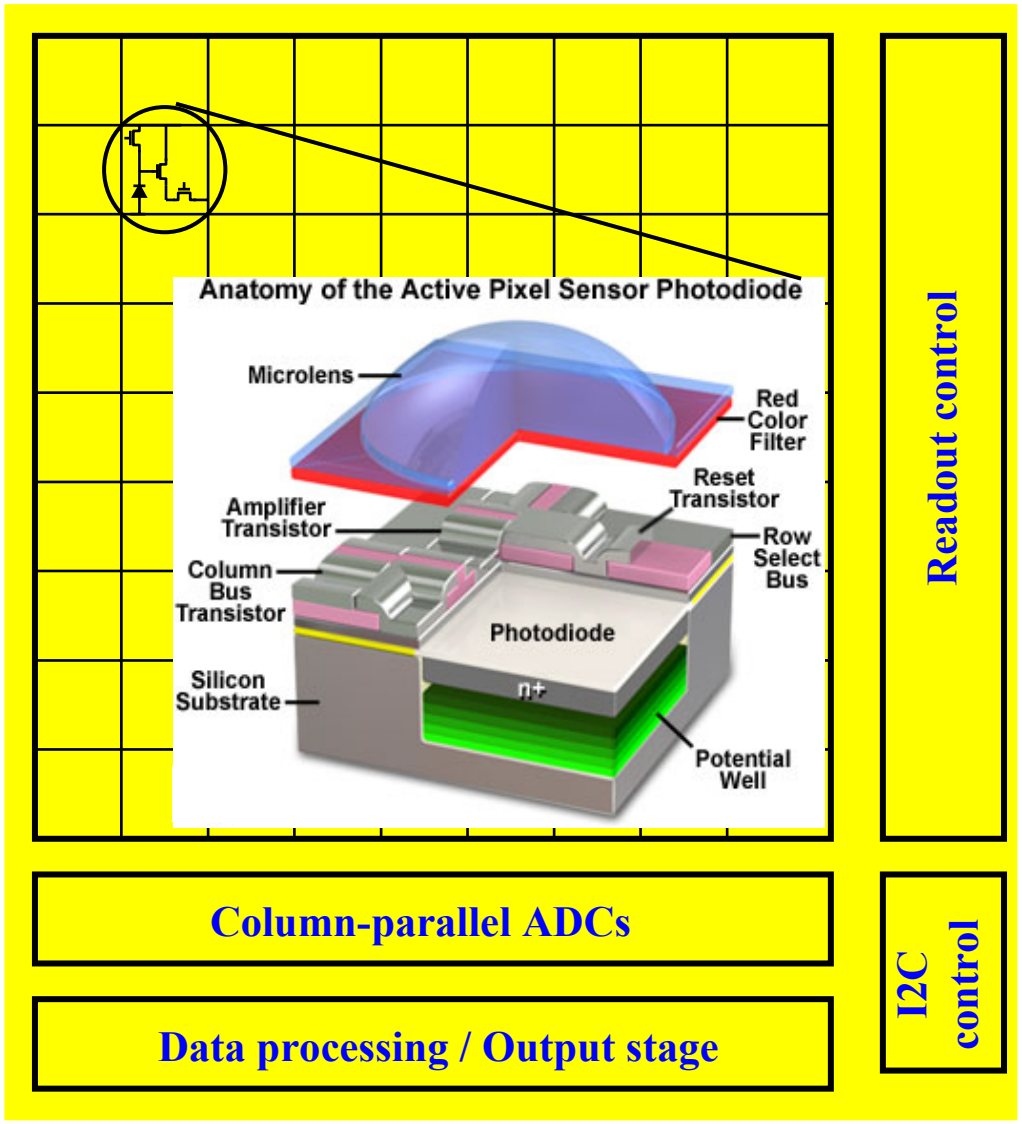
- **Coexistence analog-digital**
  - Capacitive, inductive and common-impedance couplings
  - A full lecture !
  - A good summary : there is no such thing as « ground », pay attention to current return



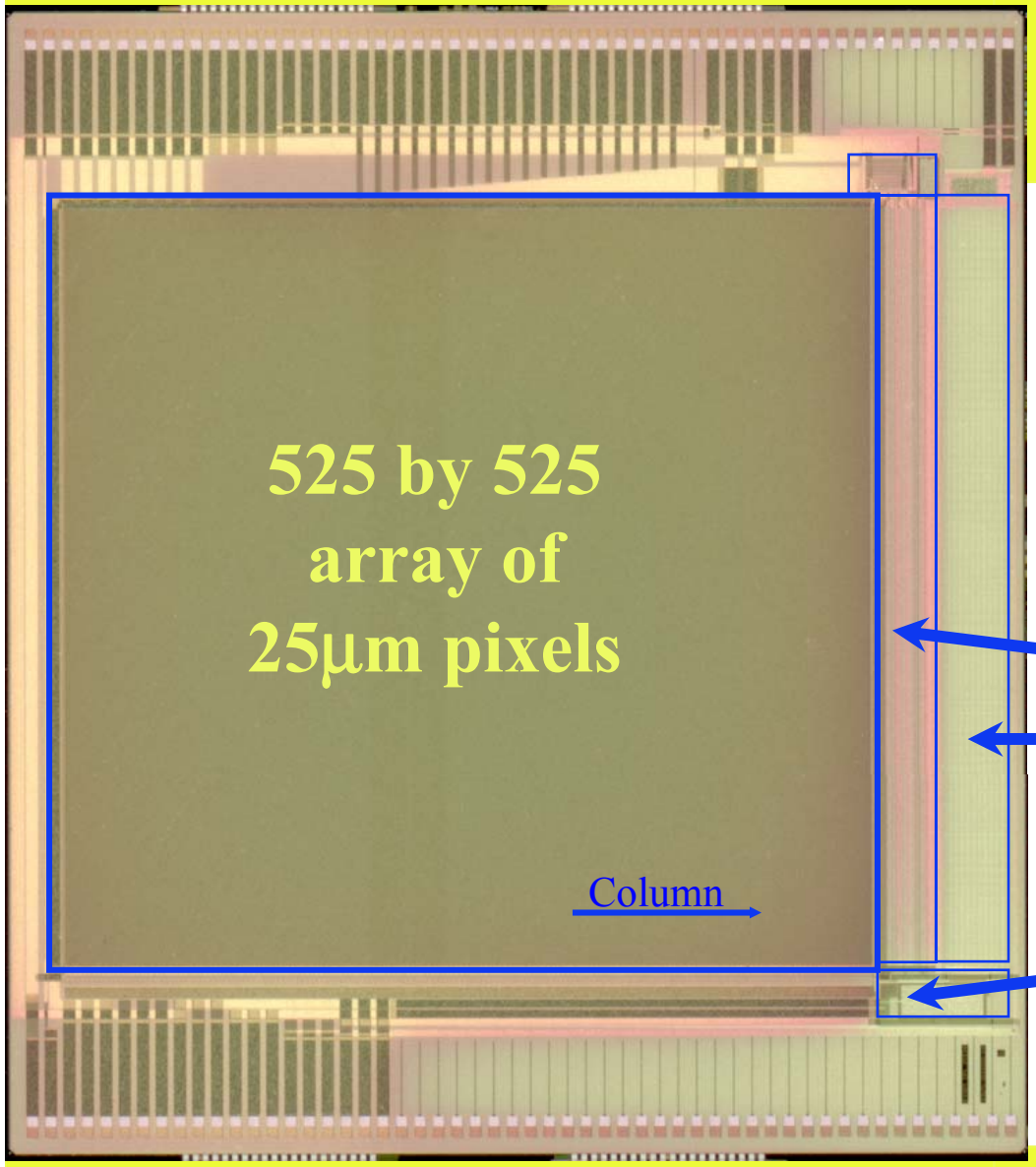
Future : detector integration (MAPS)

MAPS : monolithic active pixel sensors

- ✓ Standard CMOS technology
- ✓ all-in-one detector-connection-readout
- ✓ small size / greater integration
- ✓ low power consumption
- ✓ radiation resistance
- ✓ system-level cost / Increased functionality
- ✓ random access (Region-of-Interest ROI readout)
- ✓ increased speed (column- or pixel- parallel processing)
- ✓ ease of use for end users



integrating the detector (MAPS)



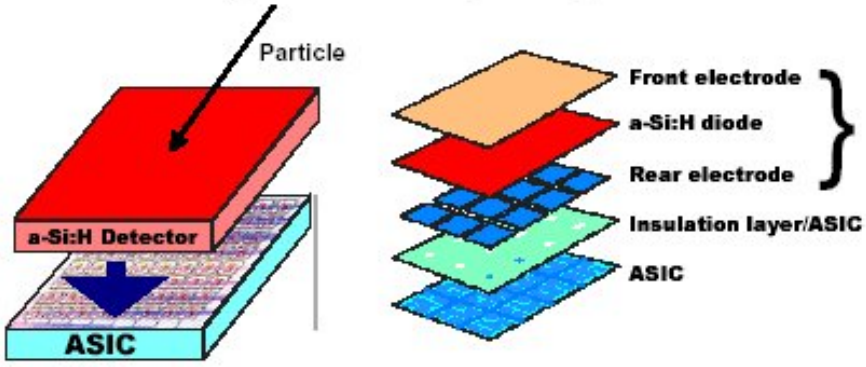
RAL Camera-on-a-chip

- 0.5 µm CMOS technology
- Design 1st time right
- Noise ≤ 50 electrons
- Power consumption: ≤300mW
- 3.3V Operation
- Readout control
- Readout speed: 10 Frames/Second
- Adjustable Gain Column Amplifiers
- **10 Bit ADC/Column**
- Alternative analogue output
- Parallel digital output
- I^2C control system
- Rad Tolerant Design, Triple

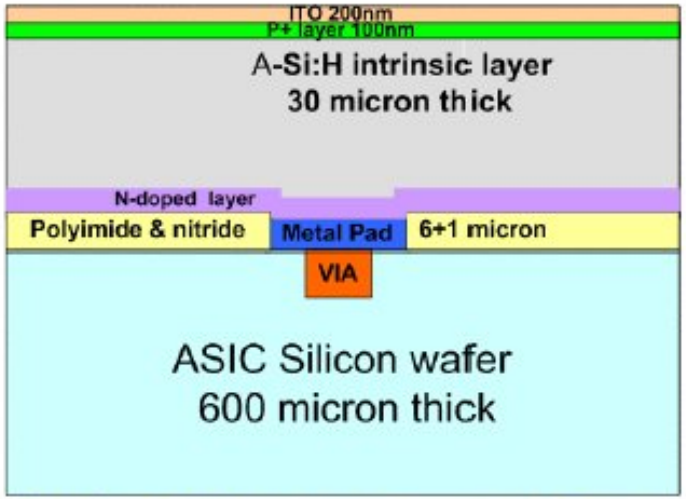
Future : detector integration (TFA)

TFA or above ASIC technology

- Emerging sensor technology for APS
  - Adapted for a-Si:H thick films
    - Bottom thin n-doped layer ~ 20 nm
    - Middle thick i-layer layer ~ 5-30 μm
    - Top thin p-doped layer ~ 40 nm
    - Indium Tin Oxide ITO ~ 100nm
  - Pixel segmentation of the n-i-p film
    - High resistivity n-layer



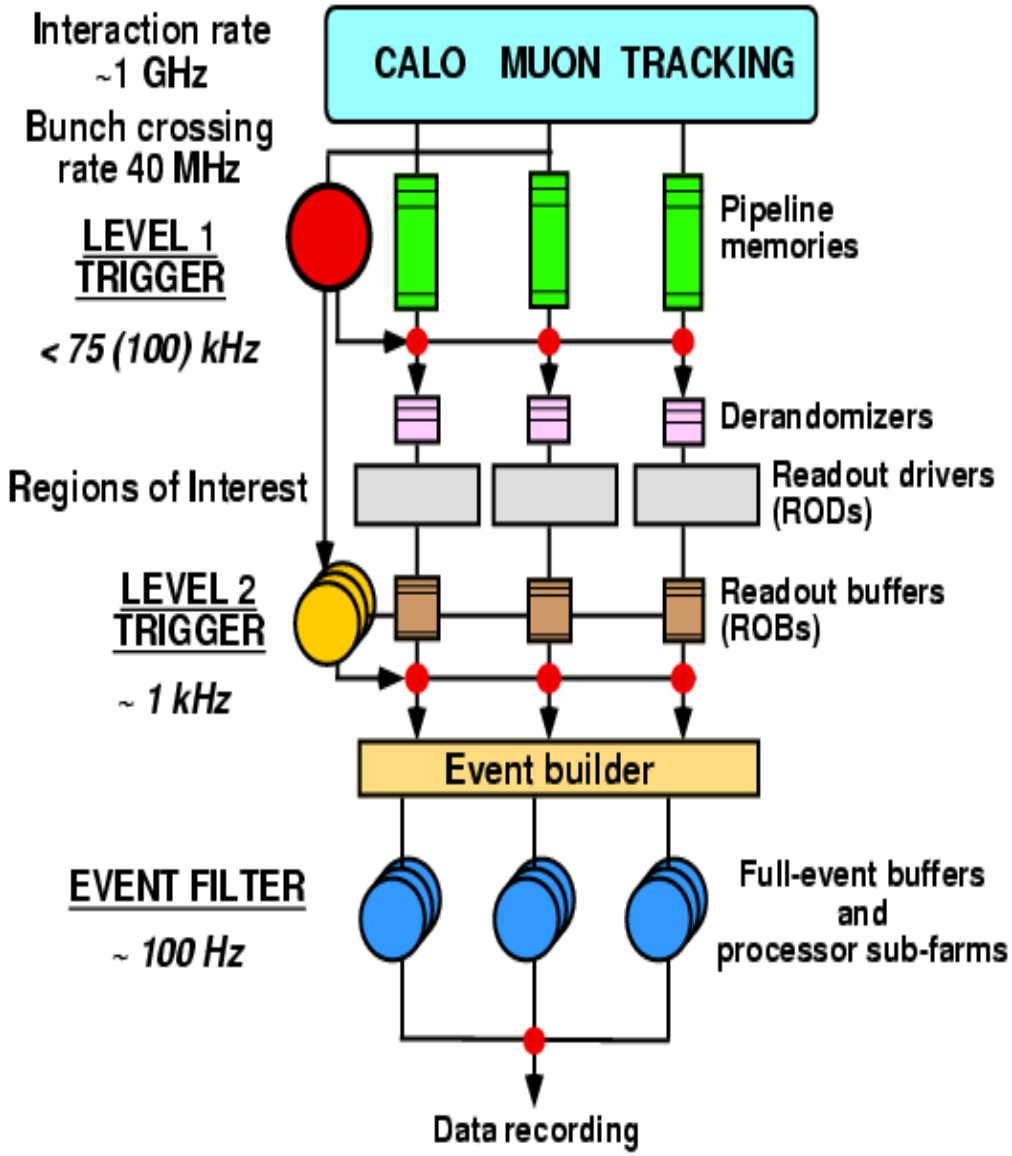
TFA Concept



Thick TFA cross section

Trigger

- **Sorting out the interesting events**
  - LVL1 : calo & muons
  - LVL2 : regions of interest
  - LVL3 : event filter
- **Discard 99.99999% of events…**
- **See lectures by P. Sphicas**



Conclusion

- **In High Energy Physics, electronics is**
  - Everywhere, from detector to control rooms
  - Essential for performance
  - Customized inside ASICs
  - Using (and pushing) state of the art technology

- **I hope the 3 lectures convinced you that**
  - It is easy to understand
  - It is sometimes an Art, but always accessible
  - It is interesting and even fun…