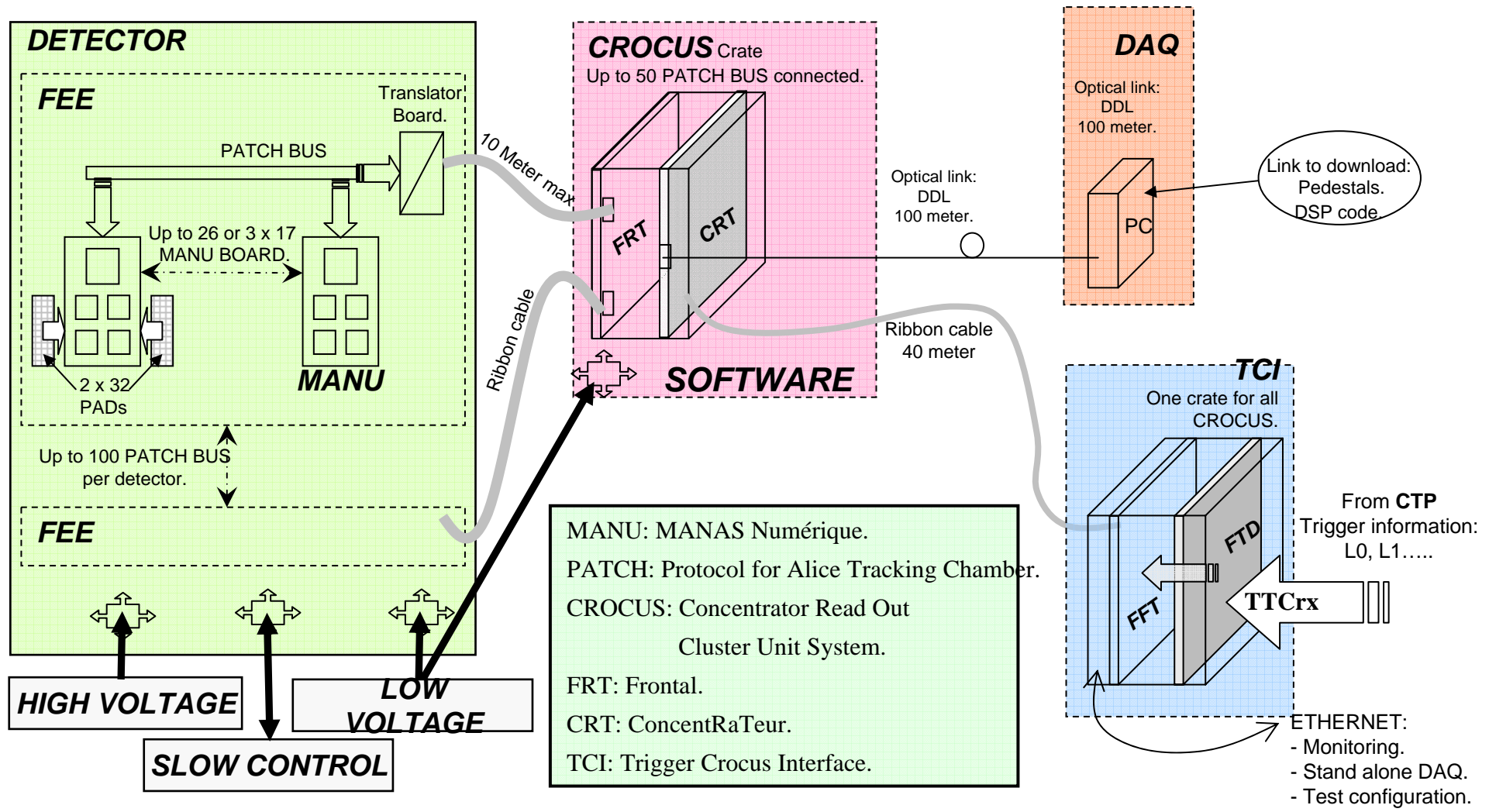
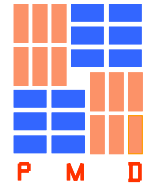




# ARCHITECTURE.

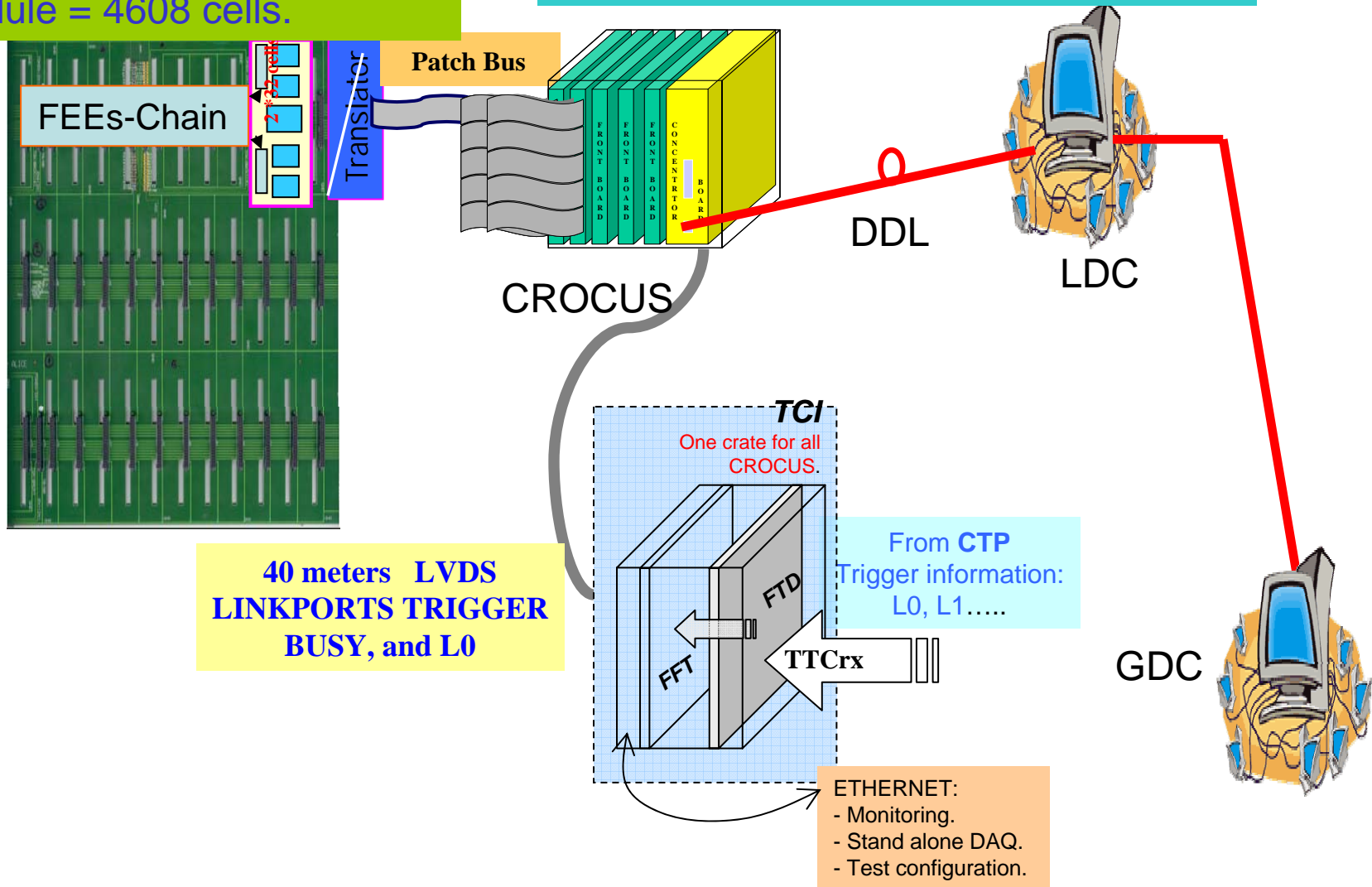


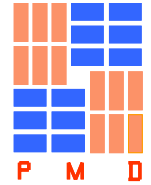


# PMD Readout Architecture

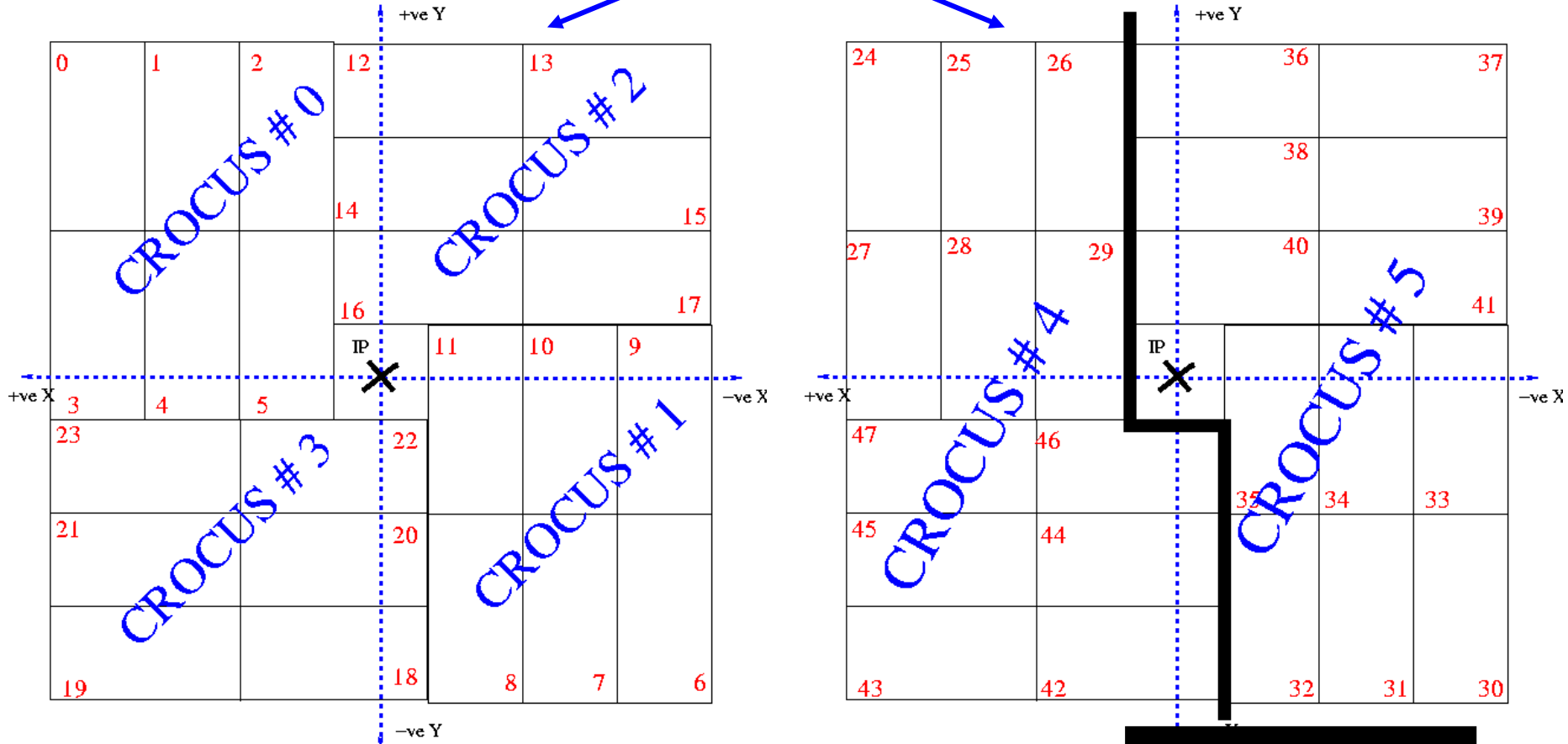
Total no of cells : 221184  
 Total no of Modules : 48  
 1 module = 4608 cells.

1 CROCUS - 50 Patch Buses  
 6 CROCUS – 300 Patch Buses





**PMD  
(Two planes)**



PRE-SHOWER PLANE - NUMBERS IN RED ARE MODULE NUMBERS

PRE-VETO PLANE - NUMBERS IN RED ARE MODULE NUMBERS

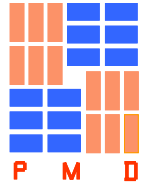
**Preshower**  
 > 24 modules  
 > 12 long type  
 > 12 short type

> 6 CROCUS  
 > 6 DDL  
 (4 PRESHOWER, 2 CPV)

**CPV**  
 > 24 modules  
 > 12 long type  
 > 12 short type



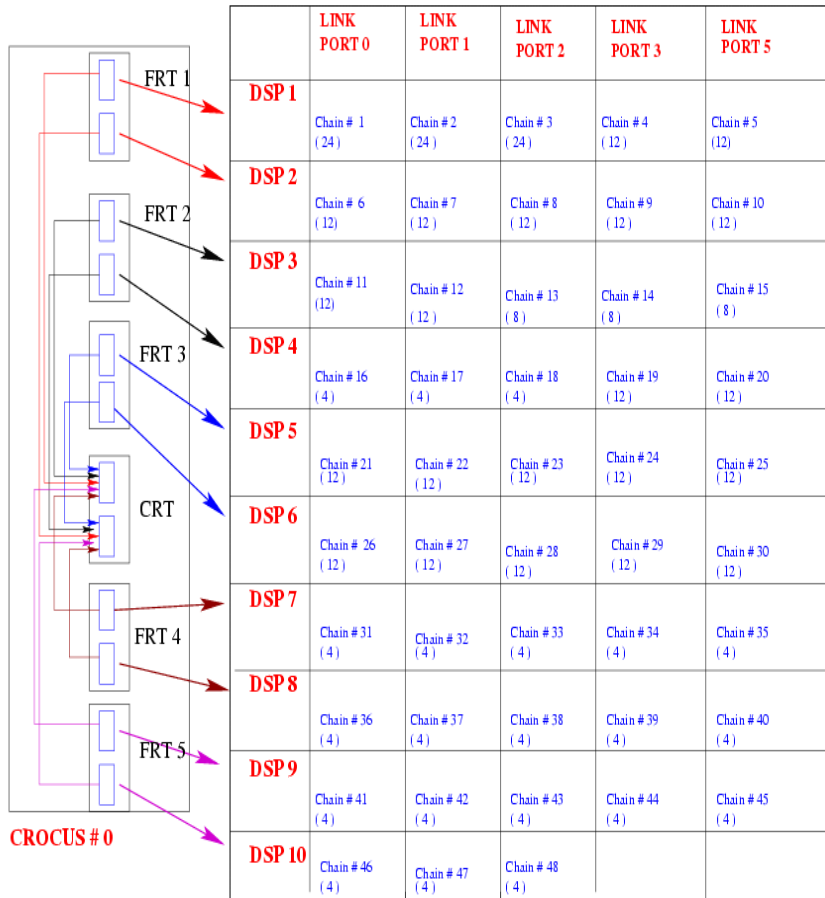
# CHAIN CONFIGURATION



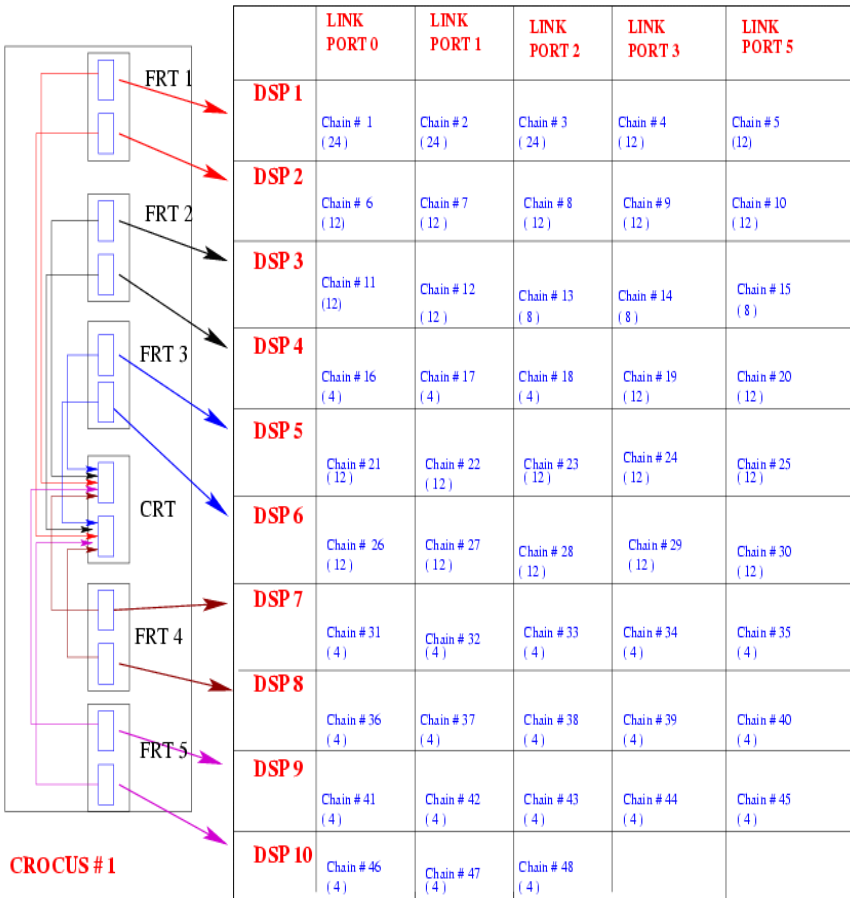
**CROCUS#0**  
➤ **48 chains**

**CROCUS#1**  
➤ **48 chains**

The No. of FEEs has been decided considering the occupancy in that zone

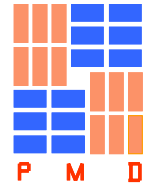


**P  
R  
E  
S  
E  
N  
T  
E  
R**



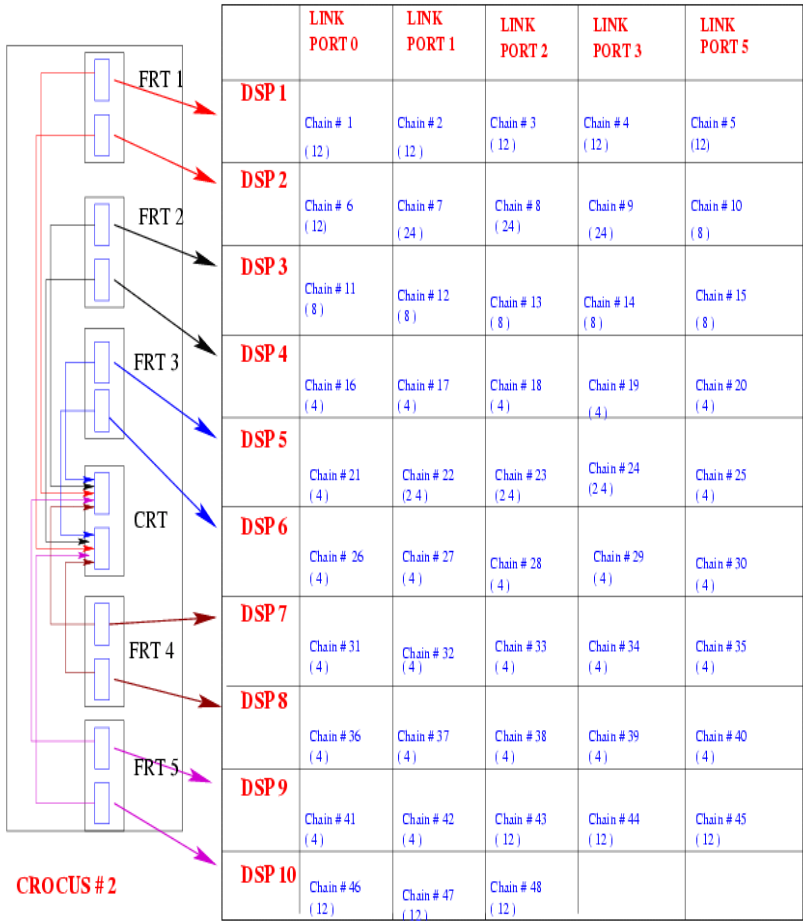


# CHAIN CONFIGURATION

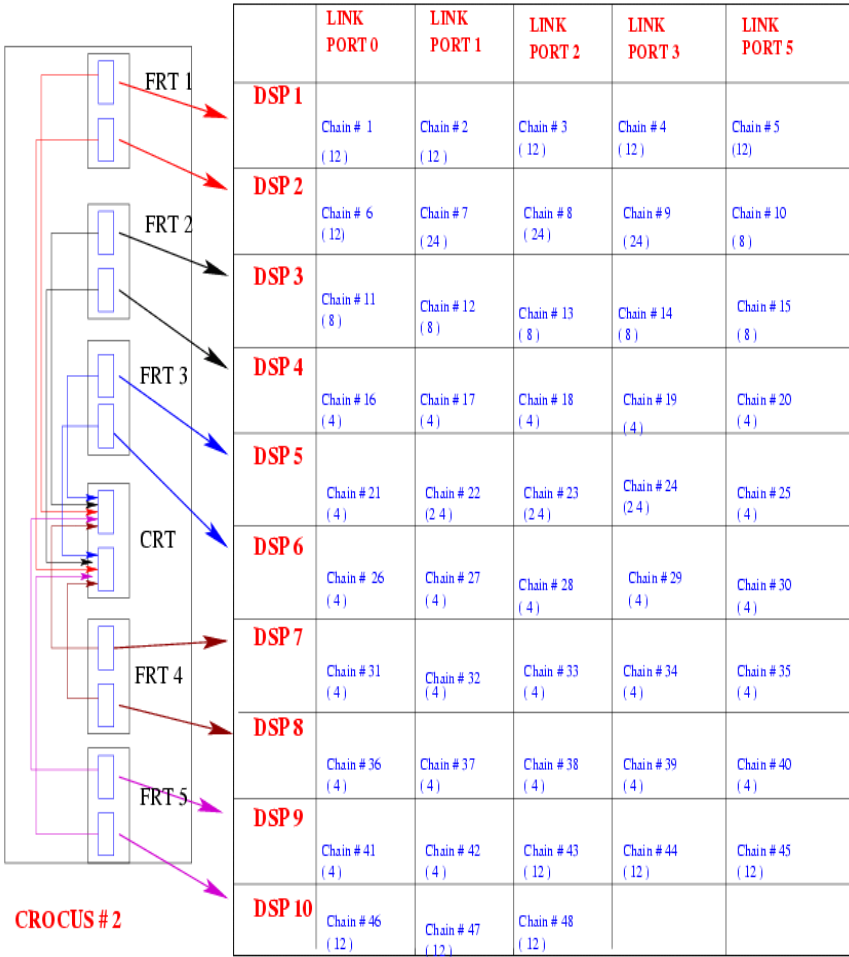


**CROCUS#2**  
➤ 48 chains

**CROCUS#3**  
➤ 48 chains

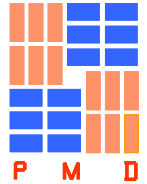


R E S T O R E



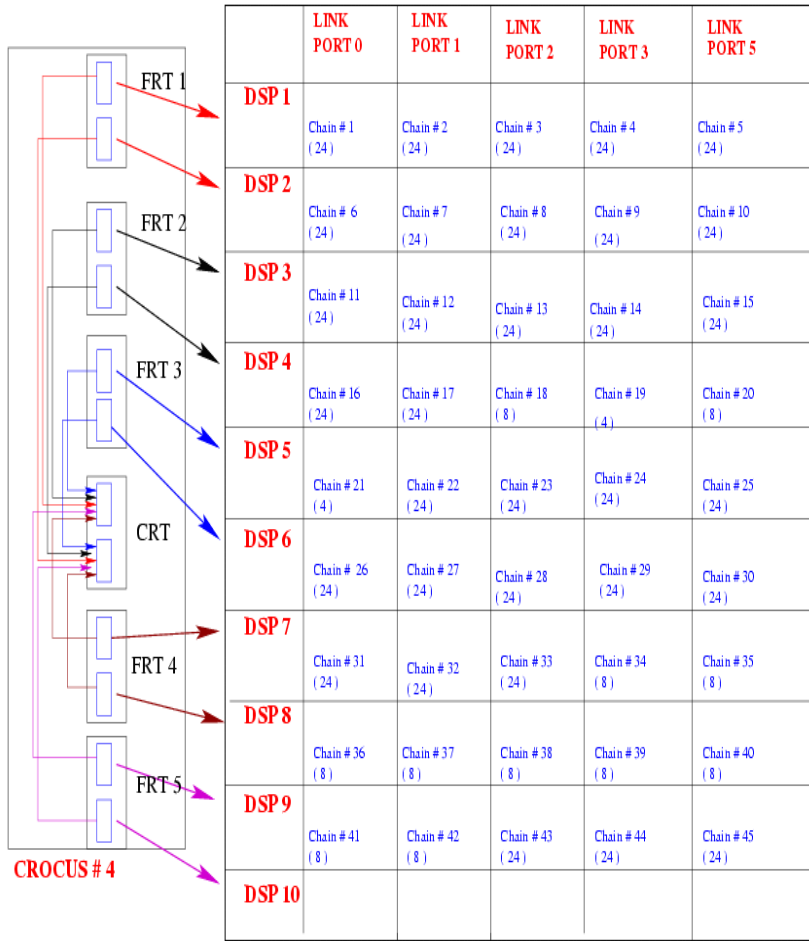


# CHAIN CONFIGURATION

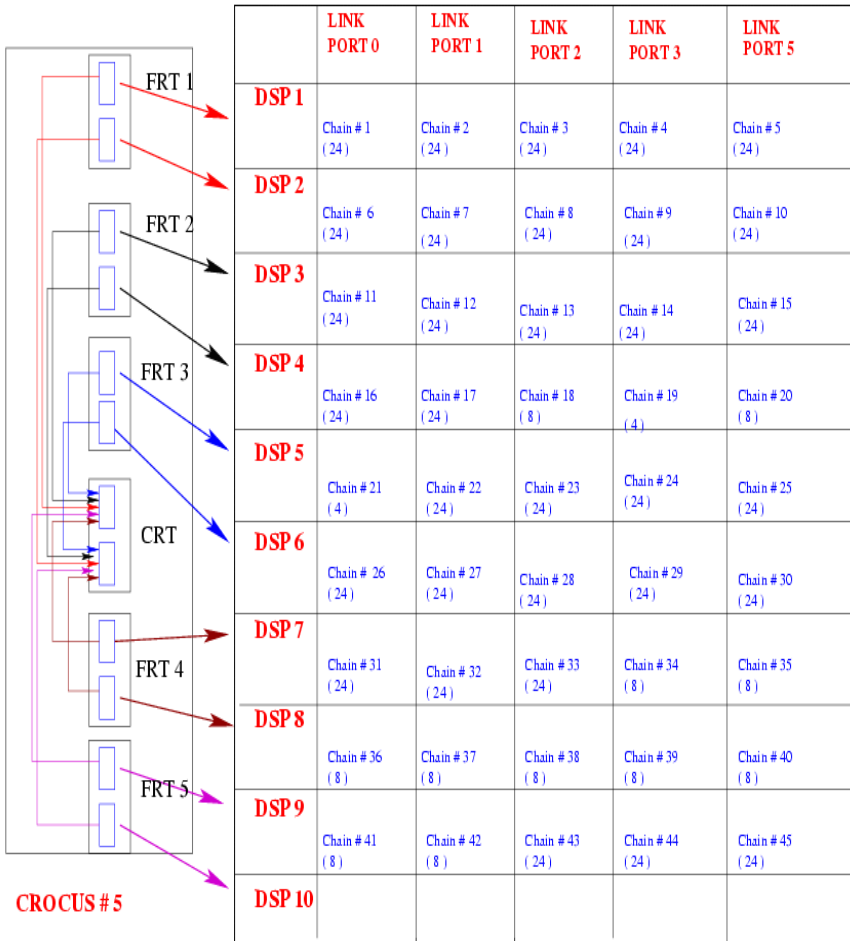


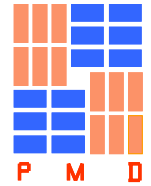
**CROCUS#4**  
➤ 45 chains

**CROCUS#5**  
➤ 45 chains

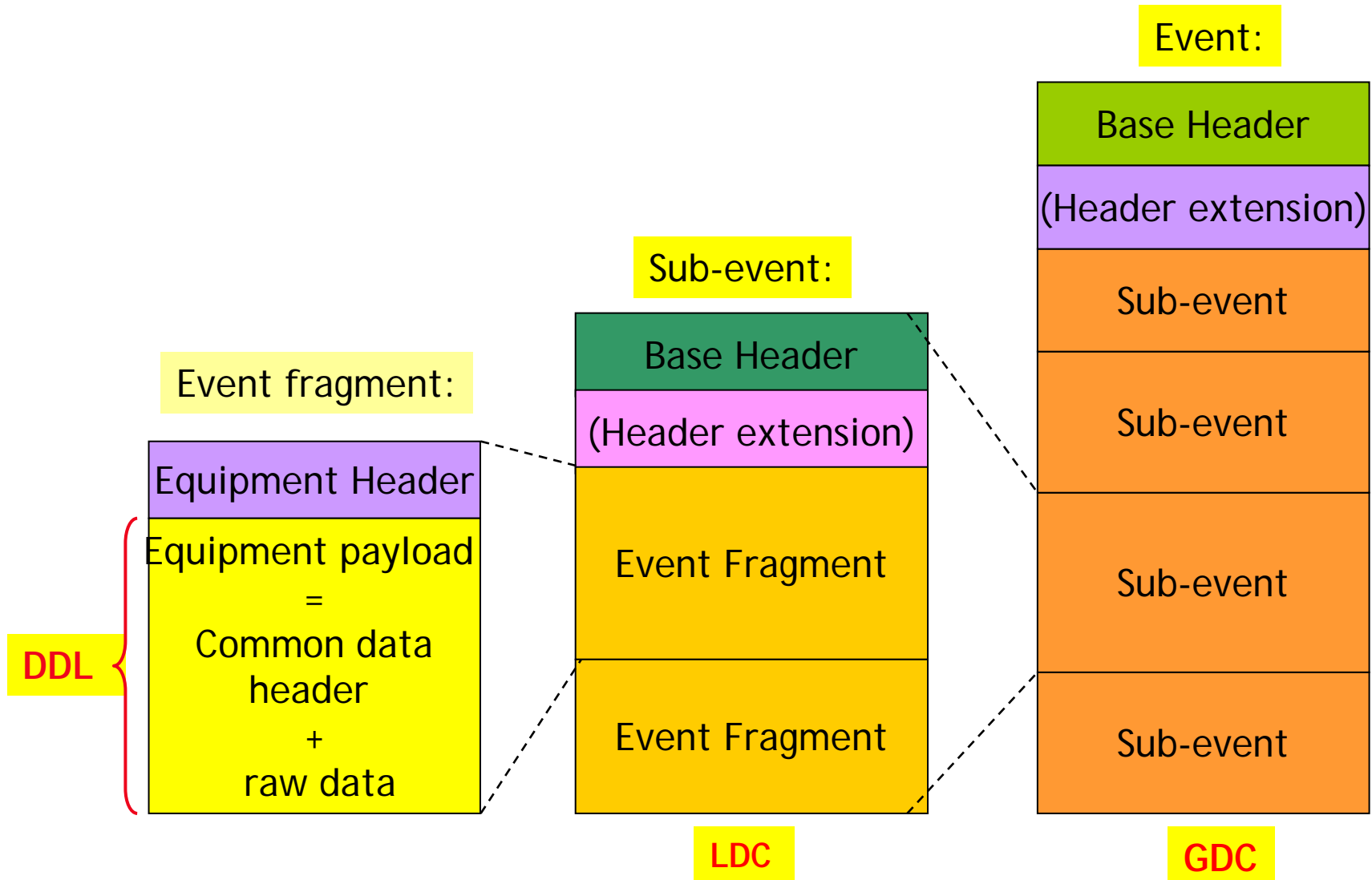


C  
P  
V



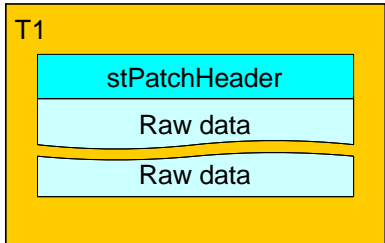
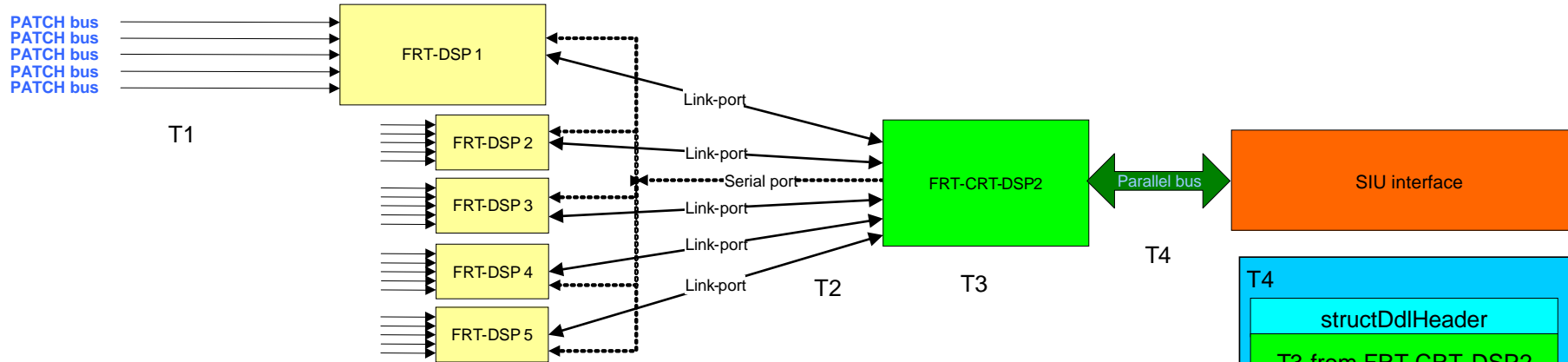
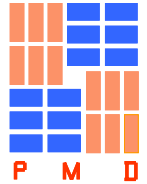


# Event Logic Structure





# DDL Data Format

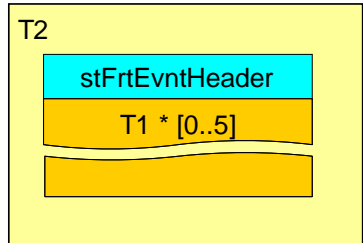


```

struct StPatchHeader {
  ui32 fuiPatchDataKey; // 0xB000000B
  ui32 fuiTotalLength;
  ui32 fuiRawDataLength;
  ui32 fuiPATCHID;
}

```

DDL TRAILERS 2 Words :  
0xD000000D

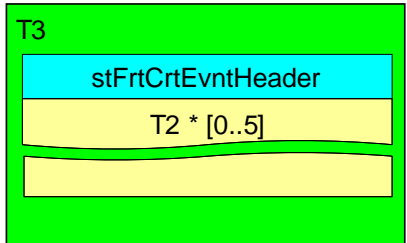


```

struct StFrtEventHeader {
  ui32 fuiFrtDataKey; // 0xF000000F
  ui32 fuiTotalLength;
  ui32 fuiRawDataLength;
  ui32 fuiDspID;
  ui32 fuiCrt1L1aTriggerCounter;
  ui32 fuiMiniEvtntdBunchCrossing;
  ui32 fuiFrtL1aTriggerCounter;
  ui32 fuiFrtL1rTriggerCounter;
  bool fbEvenPadded;
  ui32 fuiErr;
}

```

**Note:**  
If (bEvenPadded=true T3 block will terminate by junk32 bit word

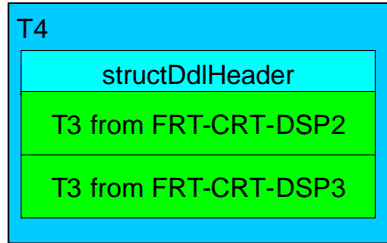


```

struct StFrtCrtEventHeader {
  ui32 fuiFrtCrtDataKey; // 0xFC0000FC Filled by FrtCrtEventDumper ( Frt-Crt 2&3 )
  ui32 fuiTotalLength; // Filled by FrtCrtEventDumper ( Frt-Crt 2&3 )
  ui32 fuiRawDataLength; // Filled by FrtCrtEventDumper ( Frt-Crt 2&3 )
  ui32 fuiFrtCrtDspID; // Filled by FrtCrtEventDumper ( Frt-Crt 2&3 )
  ui32 fuiCrtL0TriggerCounter; // Filled by DdlDumpingManager (Crt1)
  ui32 fuiMiniEvtntdBunchCrossing; // Filled by DdlDumpingManager (Crt1)
  ui32 fuiEvtntdBunchCrossing; // Filled by DdlDumpingManager (Crt1)
  ui32 fuiEvtntd2OrbitNumber; // Filled by DdlDumpingManager (Crt1)
  // ui32 fuiEvenPadding; // Filled by FrtCrtEventDumper ( Frt-Crt 2&3 )
};

```

**Note:**  
m\_uiEvenPadding is just used to make structFrtCrtEvtntHeader header size even  
m\_uiEvenPadding=0xDEADBEEF

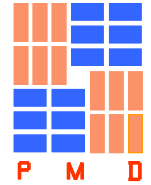


```

struct SDDLHeader {
  ui32 fui32BlockLengthInBytes;
  //-----
  ui32 fui8FormatVersion :8;
  ui32 fui8L1TriggerType :8;
  ui32 fui4Reserved1 :4;
  ui32 fui12Evtntd1BunchCrossing :12;
  //-----
  ui32 fui8Reserved2 :8;
  ui32 fui24Evtntd2OrbitNumber :24;
  //-----
  ui32 fui8BlockAttributes :8;
  ui32 fui24ParticipSubDetectors :24;
  //-----
  ui32 fui4Reserved3 :4;
  ui32 fui16StatusErrBits :16;
  ui32 fui12MiniEvtntdBunchCrossing :12;
  //-----
  ui32 fui32TriggerClassesLow;
  //-----
  ui32 fui4RoiLow :4;
  ui32 fui10Reserved4 :10;
  ui32 fui18TriggerClassesHigh :18;
  //-----
  ui32 fui12RoiHigh ;
}

```





# DATA WORD ( FEE )

MANAS Adr. 0

MANAS Adr. 1

MANAS Adr. 2

MANAS Adr. 3

0	0
0	1
1	0
1	1

**P = Parity bit ( 1 bit )**

**M = FEE board address ( 11 bits )**

**G = MANAS address ( 2 bits )**

**C = Channel number ( 4 bits )**

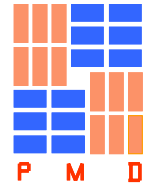
**D = Data ( 12 bits )**

typedef struct

```
{
  unsigned adc :12;
  unsigned channel :6;
  unsigned fee :11;
  unsigned unused :2;
  unsigned parity :1;
}PmdRawDataWord;
```

32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
P	0	0	M	M	M	M	M	M	M	M	M	M	M	G	G	C	C	C	C	D	D	D	D	D	D	D	D	D	D	D	D

**Output Word**

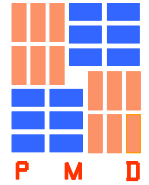


## DDL / Equipment ID scheme

Detector Id	Detector Name	DDL Offset	# of DDL	DDL Index	Connected to	Equipment Id
9	PMD	2304	6	0	CROCUS#0	2304
				1	CROCUS#1	2305
				2	CROCUS#2	2306
				3	CROCUS#3	2307
				4	CROCUS#4	2308
				5	CROCUS#5	2309



# Hardware mapping



## Idea is to convert

DDL No., patch Bus No., FEE No., Channel No. to the (x,y) coordinate

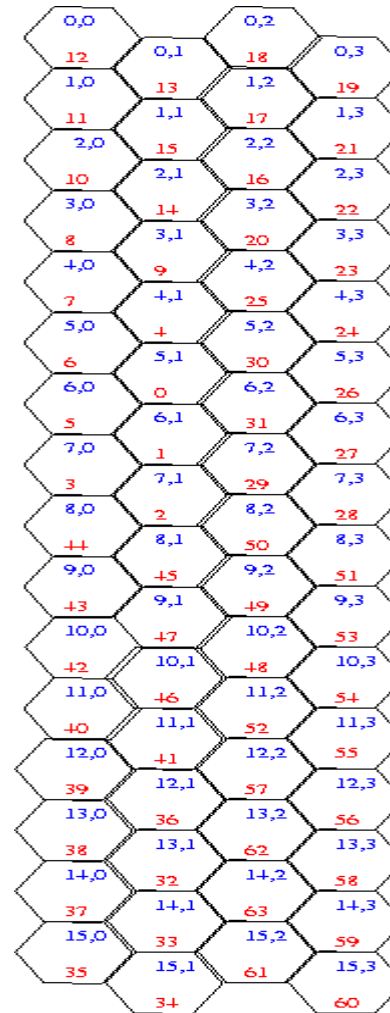
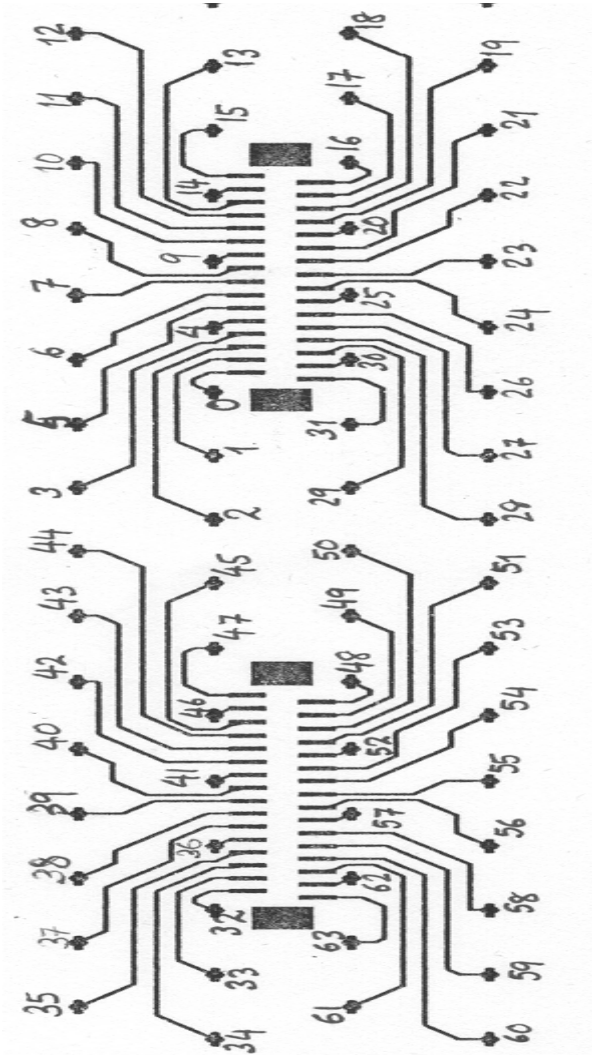
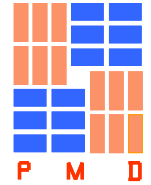
Done in 2 steps

1. DDL No., PATCH Bus No., FEE address give the physical location Of the FEE Board
2. FEE Board, Channel No give the (x,y) coordinate of the cell

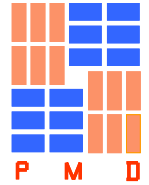




## Channel Number to (x,y) : Step 2.



This conversion is done  
Inside the program



## Status :

Hardware Mapping : done ( Committed to CVS)

Raw data reconstruction : in place (CVS), to be tested in this test beam

Raw data format : in place (CVS), to be tested in this test beam

Removal of gAlice : by 31<sup>st</sup> October, 2006

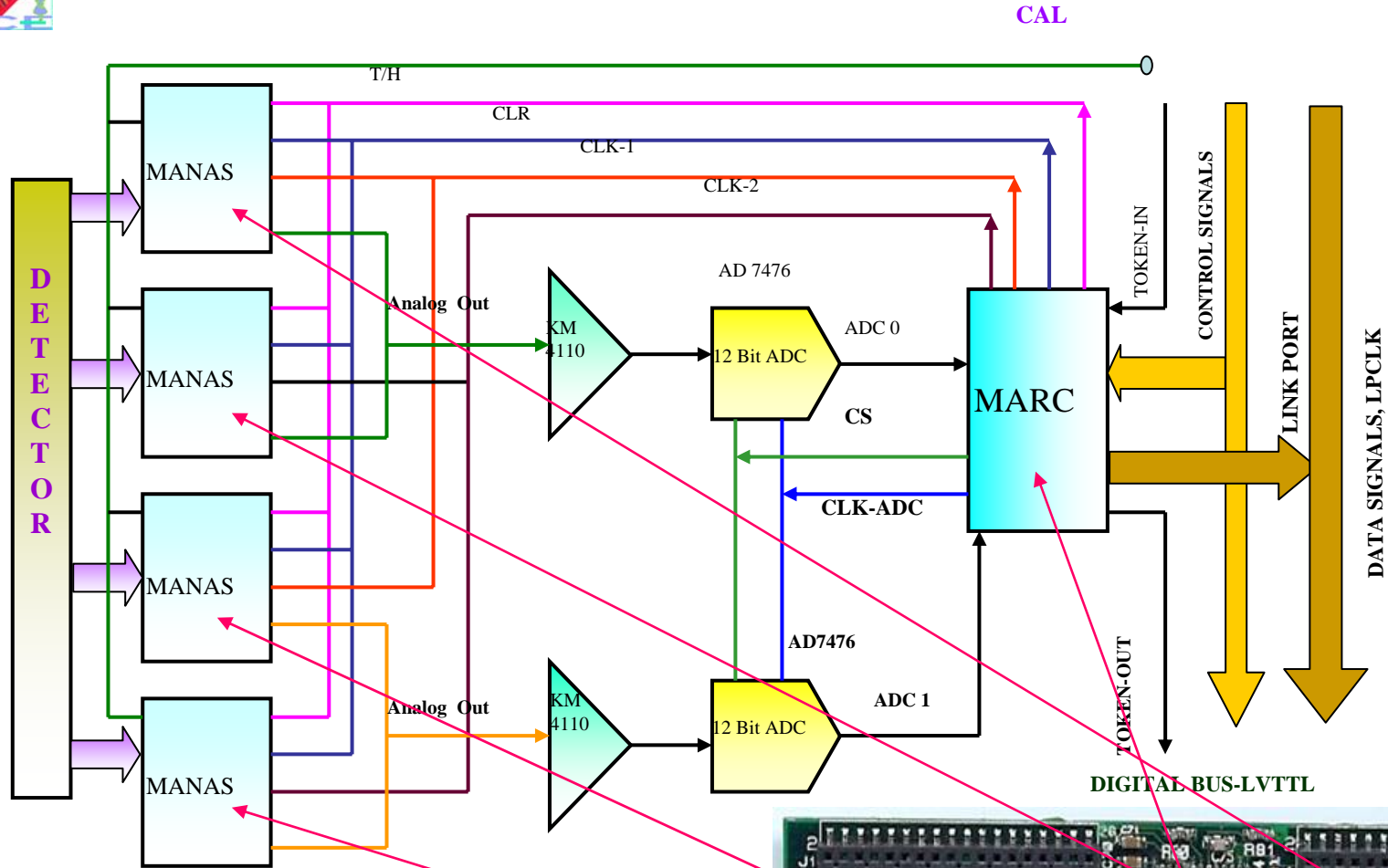
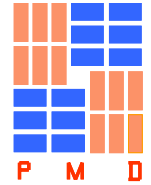
Raw2(s)Digits : by 31<sup>st</sup> October, 2006

## DDL / Equipment ID scheme

Detector ID	Detector Name	DDL Offset	#Of DDL	DDL Index	Equipment – ID	
<b>8</b>	<b>CPV</b>	<b>2048</b>	<b>2</b>	<b>4</b>	<b>2052</b>	Connected to CROCUS#4
				<b>5</b>	<b>2053</b>	Connected to CROCUS#5
<b>9</b>	<b>PRE– SHOWER</b>	<b>2304</b>	<b>4</b>	<b>0</b>	<b>2304</b>	Connected to CROCUS#0
				<b>1</b>	<b>2305</b>	Connected to CROCUS#1
				<b>2</b>	<b>2306</b>	Connected to CROCUS#2
				<b>3</b>	<b>2307</b>	Connected to CROCUS#3

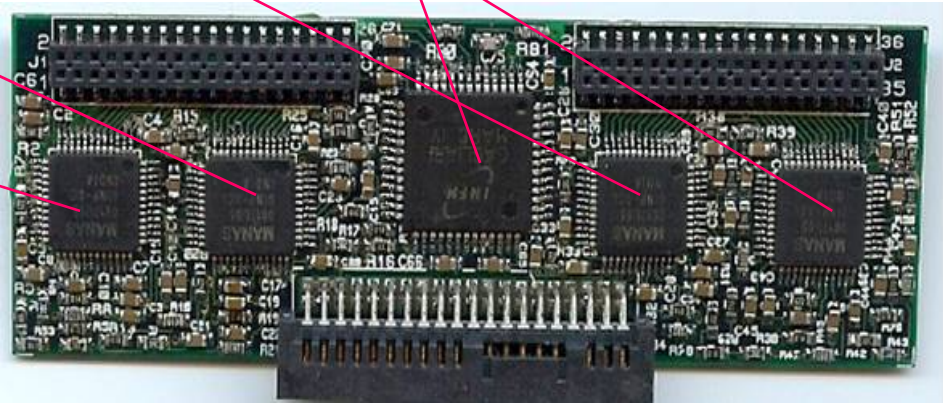


# FEE BOARD CONFIGURATION



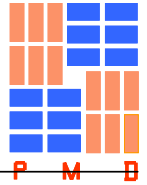
**FEE board**

- Main Components:**
1. MANAS ( Multiplexed-Analog-Signal-processor )
  2. MARC ( Muon-Arm-Readout-Chip )
  3. ADC ( Analog to Digital Converter )

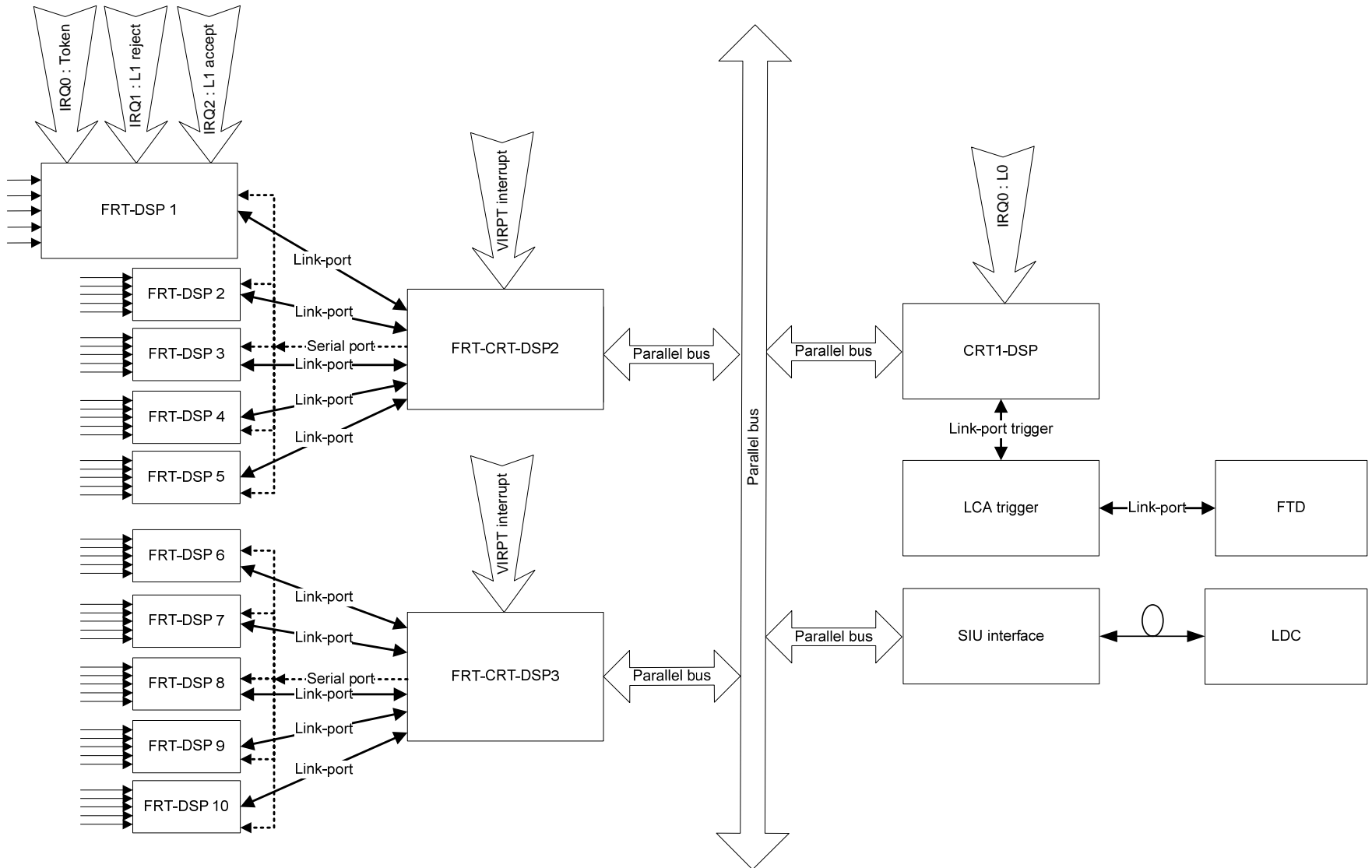


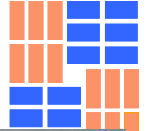


# CROCUS SYSTEM MAIN SIGNALS & I/O PORTS

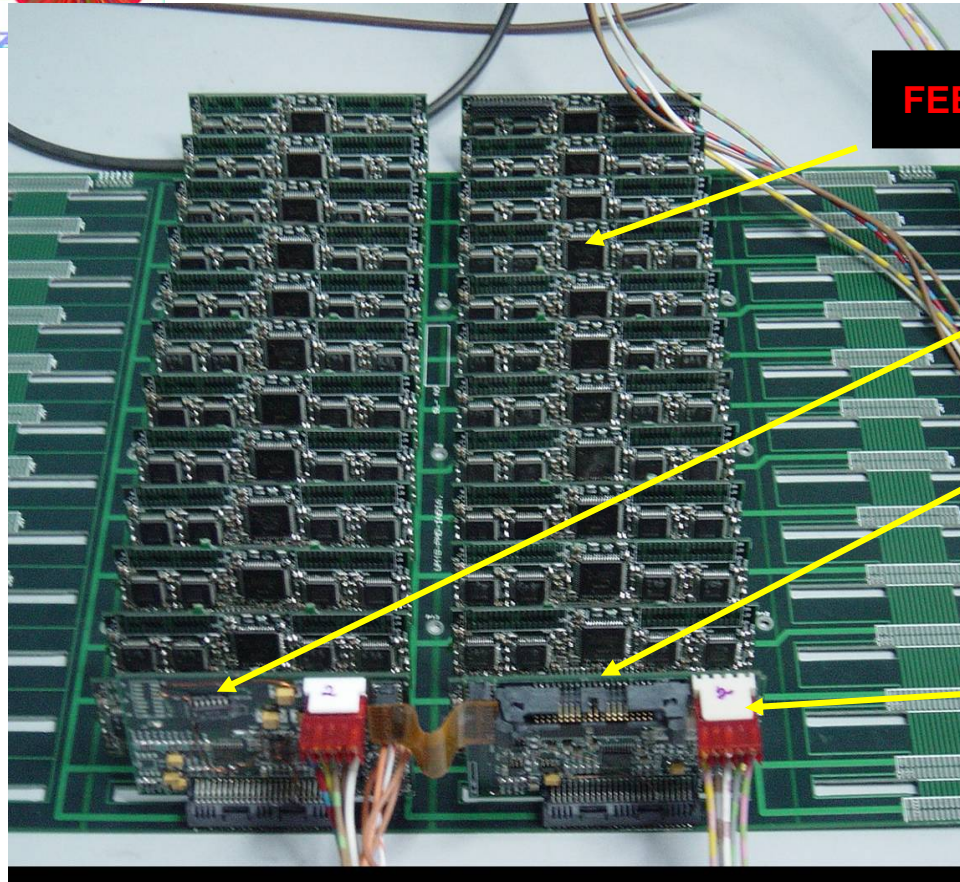


PATCH bus  
PATCH bus  
PATCH bus  
PATCH bus  
PATCH bus

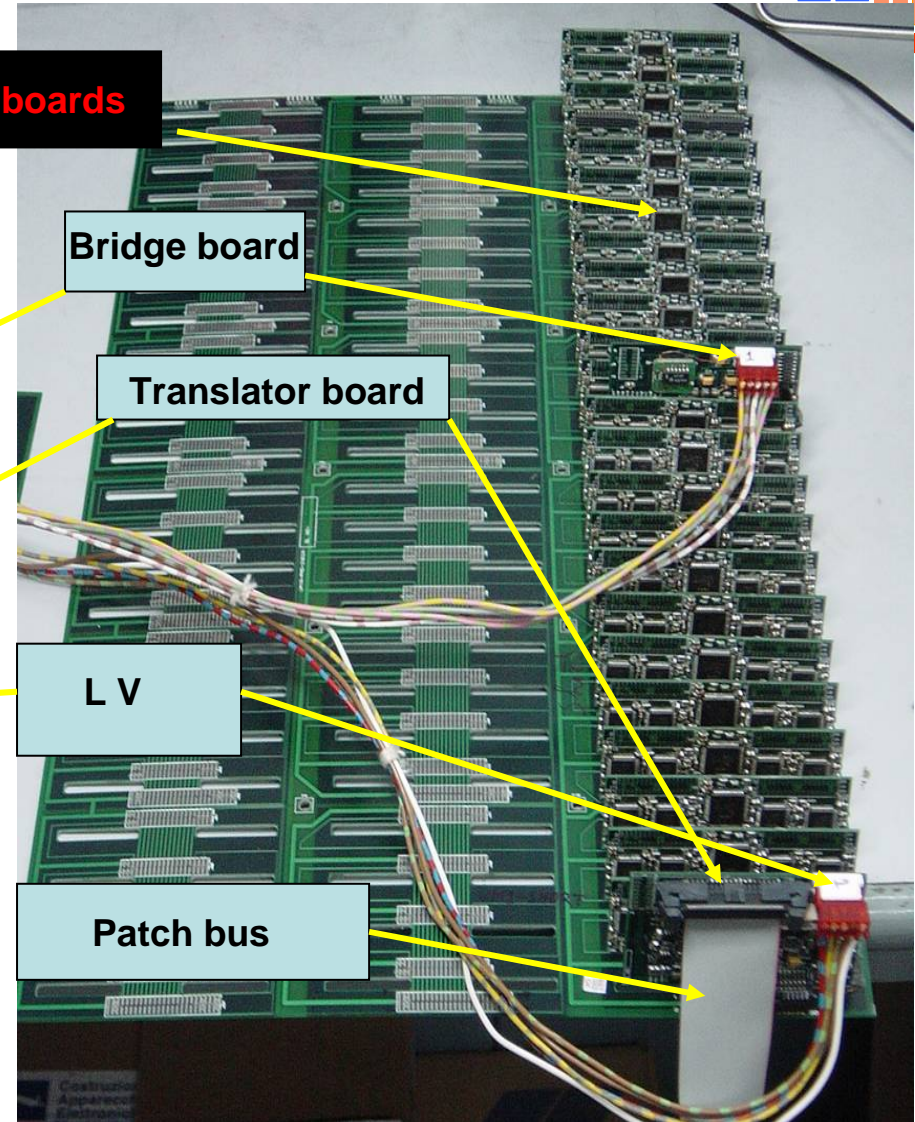




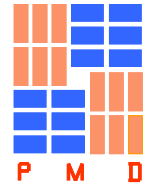
# Chain to FEE board connection



**FEE board arrangement in short type module**



**FEE board arrangement in long type module**



# DATA WORD

MANAS Adr. 0	0	0
MANAS Adr. 1	0	1
MANAS Adr. 2	1	0
MANAS Adr. 3	1	1

**P** = Parity bit / **M** = MANU Address ( 11 Bit )

**G** = MANAS Address

**C** = Channel number / **D** = Data ( 12 Bit )

32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	
<b>P</b>	<b>0</b>	<b>0</b>	<b>M</b>	<b>M</b>	<b>M</b>	<b>M</b>	<b>M</b>	<b>M</b>	<b>M</b>	<b>M</b>	<b>M</b>	<b>M</b>	<b>M</b>	<b>G</b>	<b>G</b>	<b>C</b>	<b>C</b>	<b>C</b>	<b>D</b>	<b>D</b>	<b>D</b>	<b>D</b>	<b>D</b>	<b>D</b>	<b>D</b>	<b>D</b>	<b>D</b>	<b>D</b>	<b>D</b>	<b>D</b>	<b>D</b>	<b>D</b>

Output Word