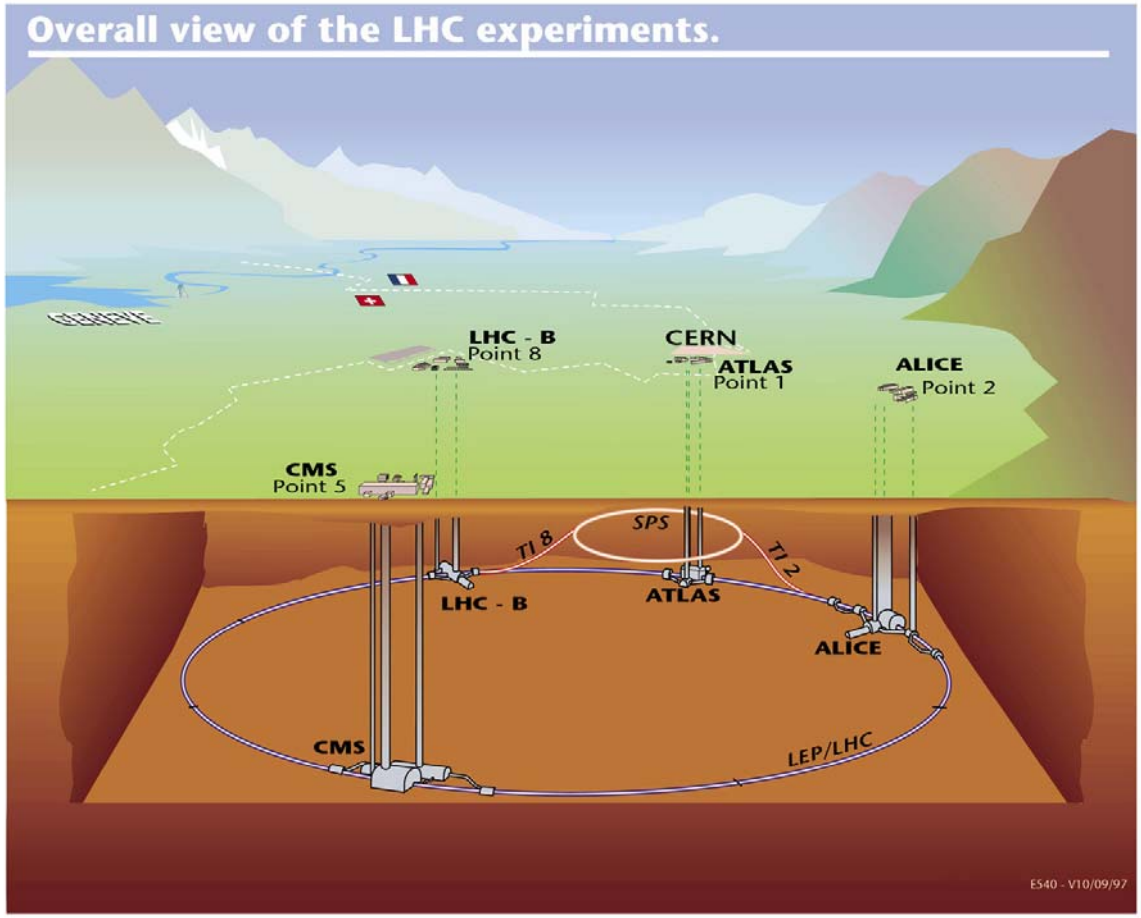
The ALICE DAQ and DDL

LHC experiments

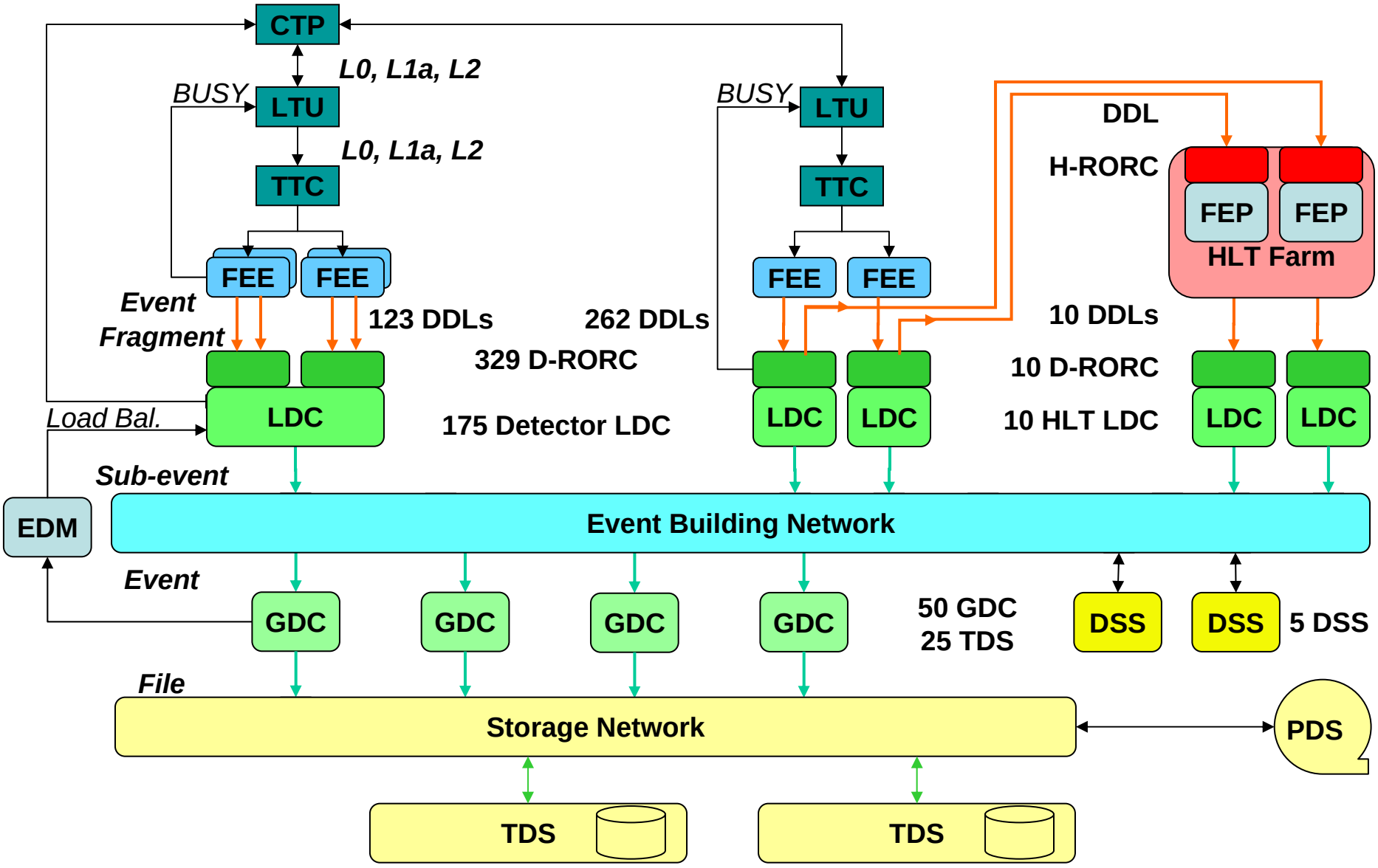


ALICE experiment

http://aliceinfo.cern.ch

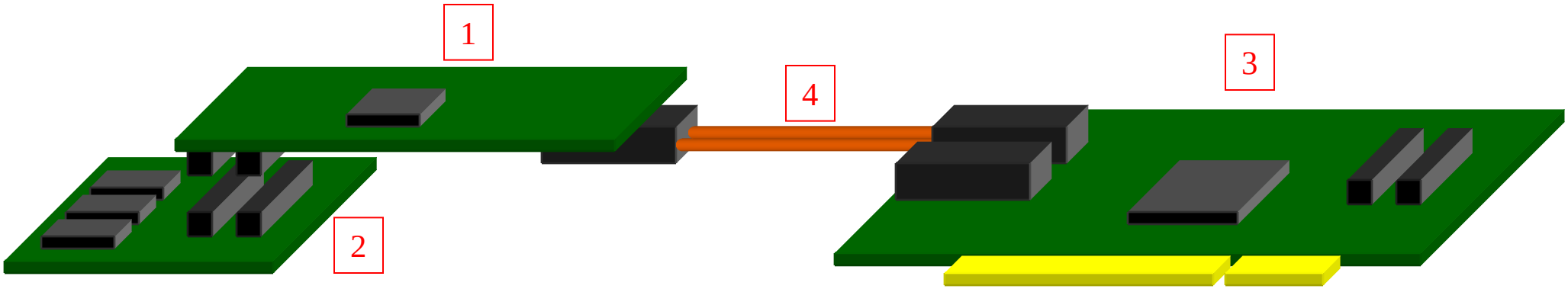
- ALICE = A Large Ion Collider Experiment @ CERN LHC
  - 17 sub-detectors: SPD, SSD, SDD, TPC, TDR, TOF, MUON TRK, MUON TRG, HMPID, PHOS, FMD, T0, V0, ZDC, PMD, ACORDE, EMCAL
  - Designed for Pb-Pb collisions (1 month/year)
  - Study as well p-p collisions

ALICE data-acquisition system



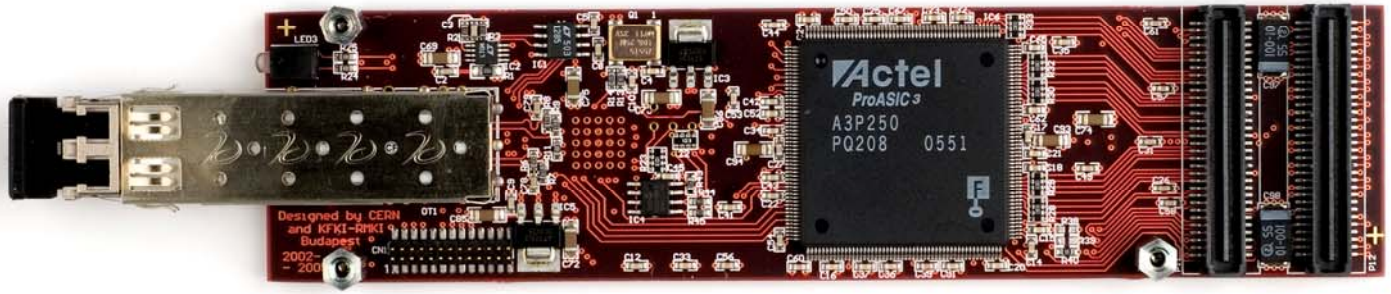
DDL architecture

- Source Interface Unit (SIU) (1)
  - Interface to the Front-end Electronics (2)
- Read-out Receiver Card (D-RORC) (3)
  - With integrated Destination Interface Unit (DIU)
- Full duplex optical link (4)
  - Multimode optical cable of up to 200 m

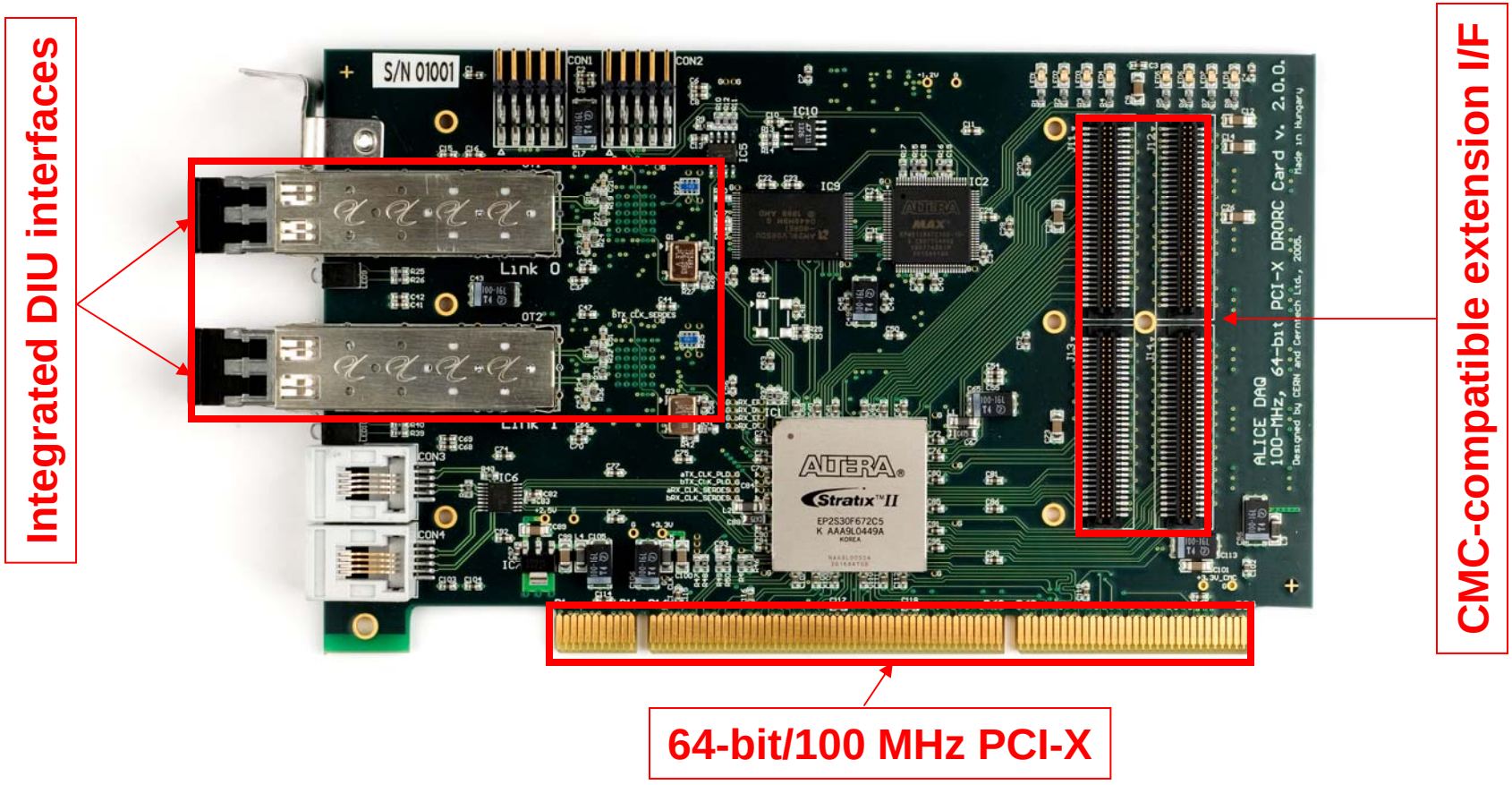


Source Interface Unit (SIU)

- 2.125 Gbit/s serial speed, ~200 MB/s bandwidth
- 3.3V (LVTTL) interface
- 32-bit half-duplex data bus (bi-directional bus)
- Bi-directional flow control
- User defined clock (synchronous interface)
- Radiation tolerant



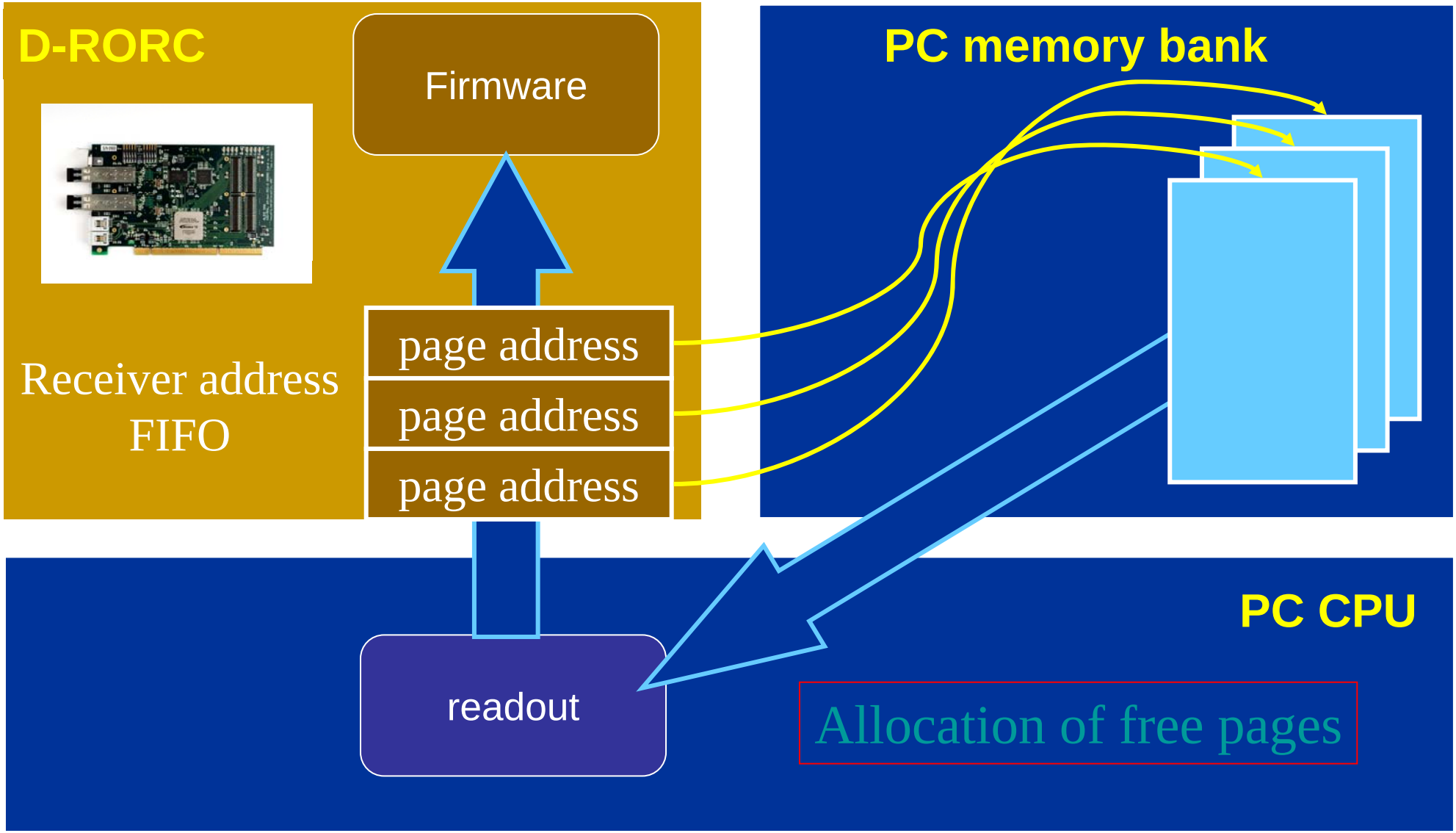
DAQ Read-out Receiver Card (D-RORC)



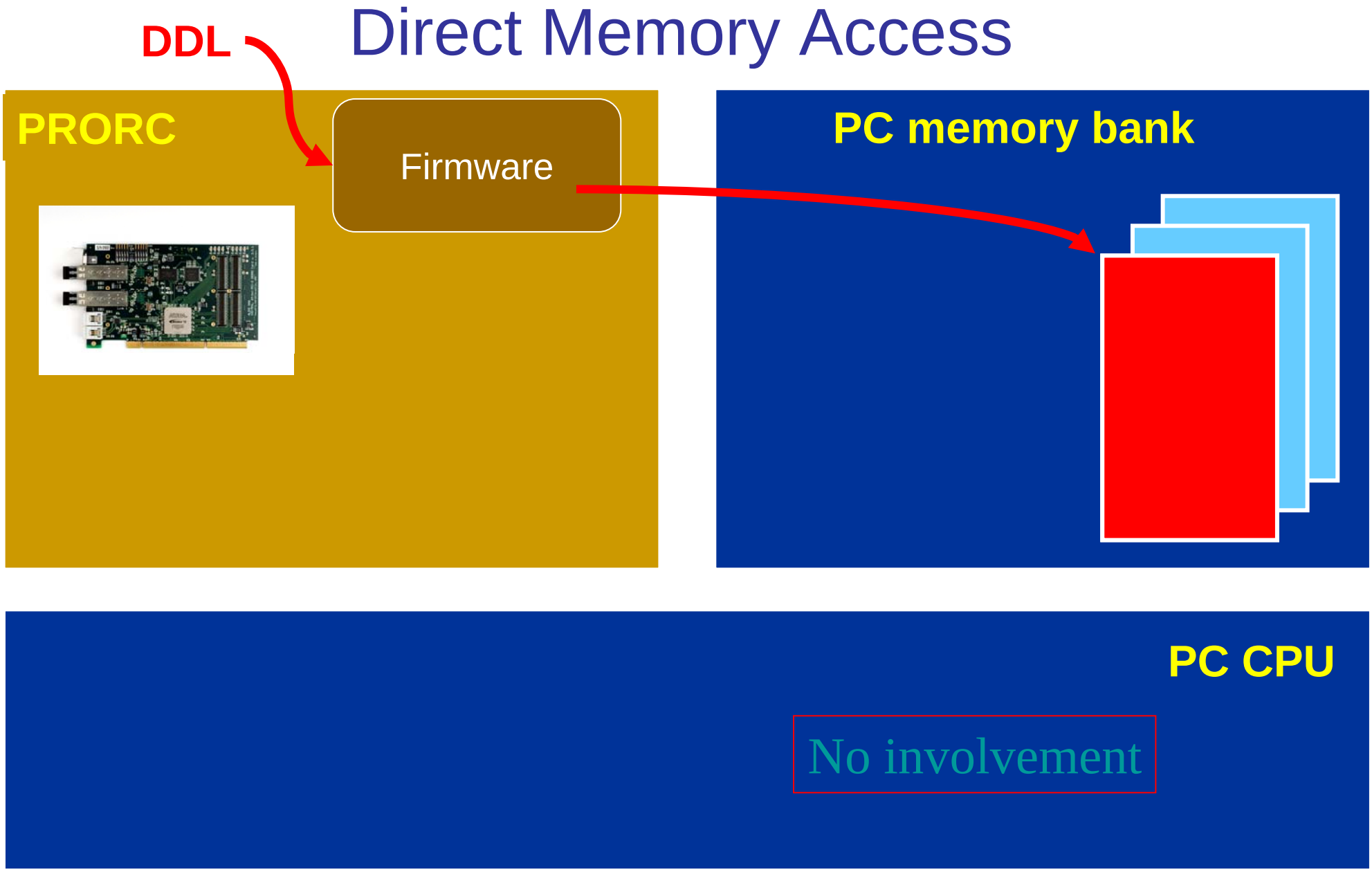
RORC features

- Interface between the DDL and PCI local bus
  - D-RORC: 64 bit/100 MHz PCI-X version, max. throughput 800 MB/s
- PCI master capability, data push architecture
  - Autonomous operation with little software assistance
  - Supports multi-paged memory management
- Direct data transfer to the PC memory
  - No local memory on the board
  - Small elasticity buffers between different clock domains
- Built-in test capability
  - Internal pattern generator can produce formatted data

Memory allocation



Direct Memory Access



Transfer report