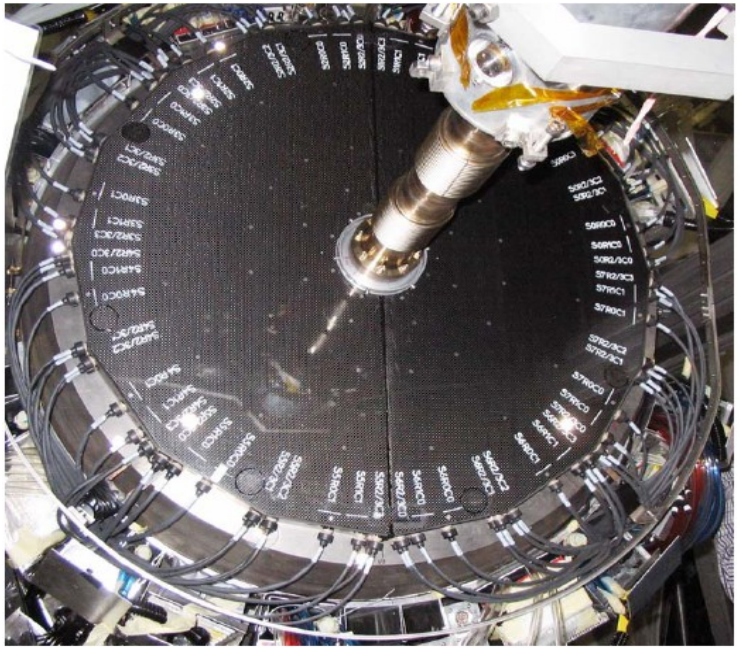
V0 Status



Work has been done on

- Raw Data
- Calibration
- DCS (see Raphaël's talk)

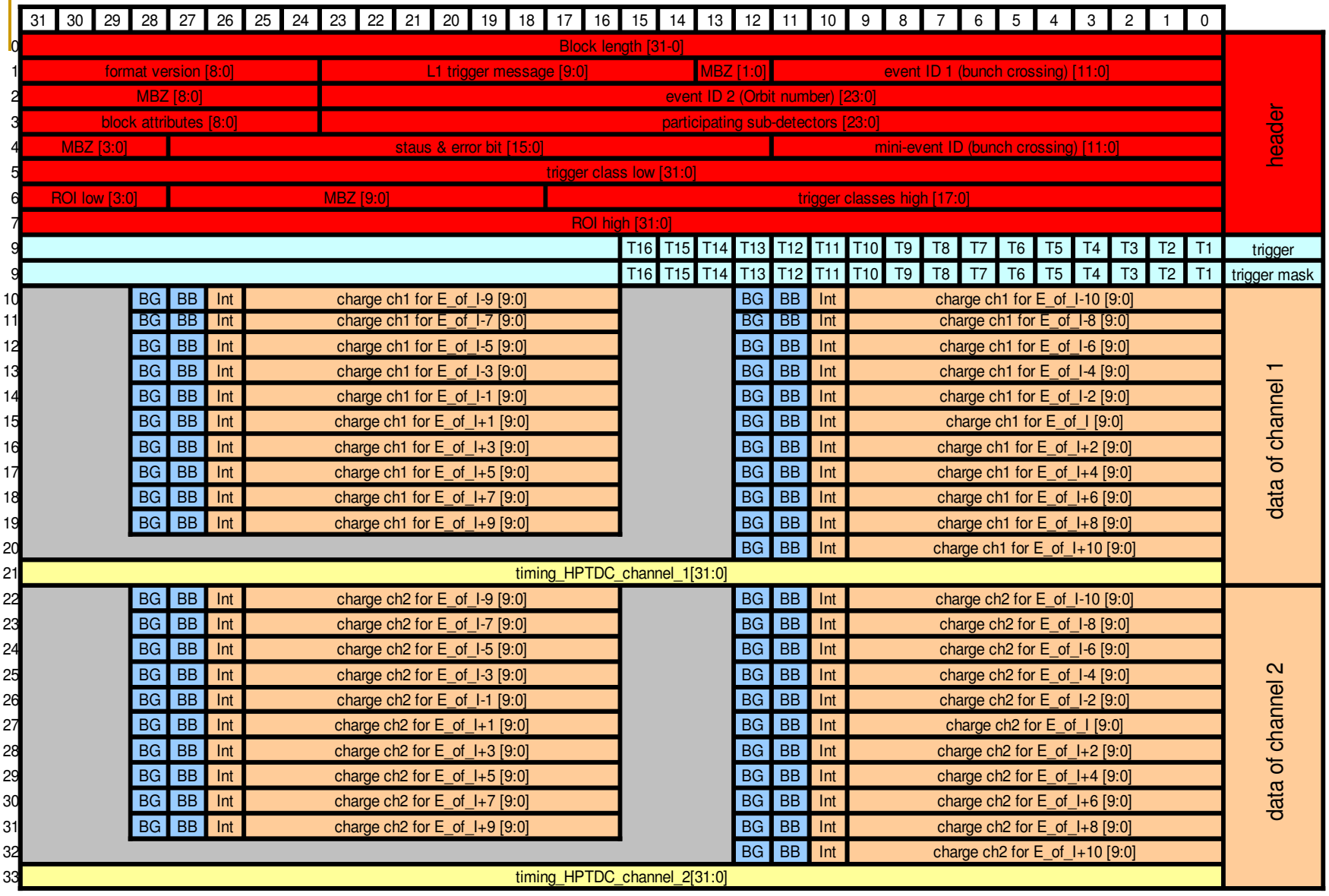
Format of Recorded Event

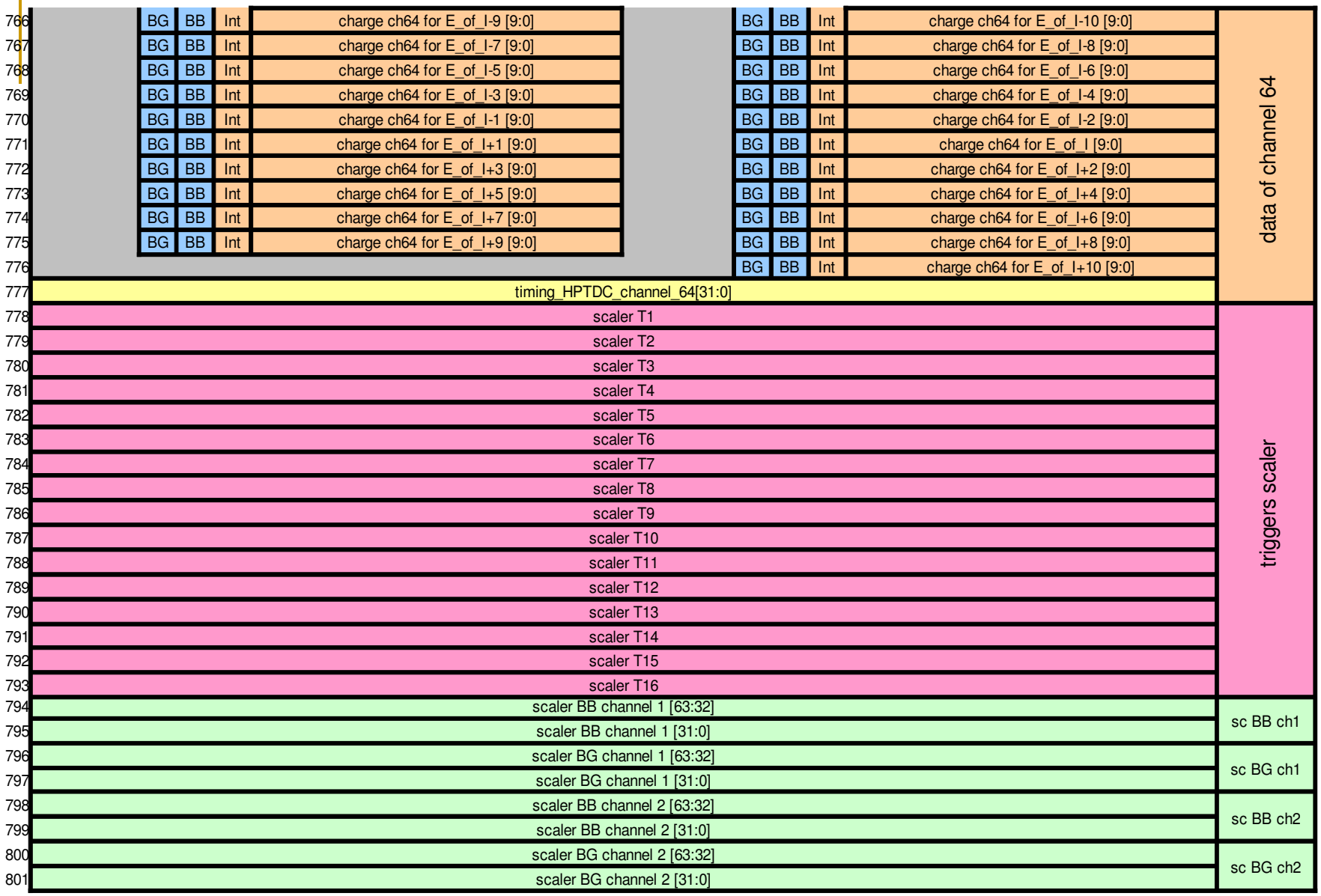
An event as seen by the V0 Front End Electronics will be:

- Charges (64),
- Arrival times (64) and time response widths (64),
- Beam-Beam (BB) and Beam-Gas (BG) flags (64),
- States of the 5 triggers sent to the CTP (MinBias (MB), Beam-Beam (BB), Beam-Gas (BG), Central, and SemiCentral).

For each event triggered by a L2 signal coming from the CTP (called Event of Interest or EoI), the following information will be sent to the DAQ to be recorded:

1. The event of interest itself with **all** the parameters listed above, for physics analysis
2. The events between EoI-10 to EoI+10 (charges and BB/BG flags), for monitoring pedestals and for calibration purposes
3. The 10 last Minimum Bias events (charges and BB/BG flags), for monitoring gains and for calibration purposes.


31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
0 Block length [31-0]
1 format version [8:0] | L1 trigger message [9:0] | MBZ [1:0] | event ID 1 (bunch crossing) [11:0]
2 MBZ [8:0] | event ID 2 (Orbit number) [23:0]
3 block attributes [8:0] | participating sub-detectors [23:0]
4 MBZ [3:0] | staus & error bit [15:0] | mini-event ID (bunch crossing) [11:0]
5 trigger class low [31:0]
6 ROI low [3:0] | MBZ [9:0] | trigger classes high [17:0]
7 ROI high [31:0]
header
9 T16 T15 T14 T13 T12 T11 T10 T9 T8 T7 T6 T5 T4 T3 T2 T1
trigger
9 T16 T15 T14 T13 T12 T11 T10 T9 T8 T7 T6 T5 T4 T3 T2 T1
trigger mask
10 BG BB Int charge ch1 for E_of_I-9 [9:0] | BG BB Int charge ch1 for E_of_I-10 [9:0]
11 BG BB Int charge ch1 for E_of_I-7 [9:0] | BG BB Int charge ch1 for E_of_I-8 [9:0]
12 BG BB Int charge ch1 for E_of_I-5 [9:0] | BG BB Int charge ch1 for E_of_I-6 [9:0]
13 BG BB Int charge ch1 for E_of_I-3 [9:0] | BG BB Int charge ch1 for E_of_I-4 [9:0]
14 BG BB Int charge ch1 for E_of_I-1 [9:0] | BG BB Int charge ch1 for E_of_I-2 [9:0]
15 BG BB Int charge ch1 for E_of_I+1 [9:0] | BG BB Int charge ch1 for E_of_I [9:0]
16 BG BB Int charge ch1 for E_of_I+3 [9:0] | BG BB Int charge ch1 for E_of_I+2 [9:0]
17 BG BB Int charge ch1 for E_of_I+5 [9:0] | BG BB Int charge ch1 for E_of_I+4 [9:0]
18 BG BB Int charge ch1 for E_of_I+7 [9:0] | BG BB Int charge ch1 for E_of_I+6 [9:0]
19 BG BB Int charge ch1 for E_of_I+9 [9:0] | BG BB Int charge ch1 for E_of_I+8 [9:0]
20 BG BB Int charge ch1 for E_of_I+10 [9:0]
21 timing_HPTDC_channel_1[31:0]
data of channel 1
22 BG BB Int charge ch2 for E_of_I-9 [9:0] | BG BB Int charge ch2 for E_of_I-10 [9:0]
23 BG BB Int charge ch2 for E_of_I-7 [9:0] | BG BB Int charge ch2 for E_of_I-8 [9:0]
24 BG BB Int charge ch2 for E_of_I-5 [9:0] | BG BB Int charge ch2 for E_of_I-6 [9:0]
25 BG BB Int charge ch2 for E_of_I-3 [9:0] | BG BB Int charge ch2 for E_of_I-4 [9:0]
26 BG BB Int charge ch2 for E_of_I-1 [9:0] | BG BB Int charge ch2 for E_of_I-2 [9:0]
27 BG BB Int charge ch2 for E_of_I+1 [9:0] | BG BB Int charge ch2 for E_of_I [9:0]
28 BG BB Int charge ch2 for E_of_I+3 [9:0] | BG BB Int charge ch2 for E_of_I+2 [9:0]
29 BG BB Int charge ch2 for E_of_I+5 [9:0] | BG BB Int charge ch2 for E_of_I+4 [9:0]
30 BG BB Int charge ch2 for E_of_I+7 [9:0] | BG BB Int charge ch2 for E_of_I+6 [9:0]
31 BG BB Int charge ch2 for E_of_I+9 [9:0] | BG BB Int charge ch2 for E_of_I+8 [9:0]
32 BG BB Int charge ch2 for E_of_I+10 [9:0]
33 timing_HPTDC_channel_2[31:0]
data of channel 2


766 BG BB Int charge ch64 for E_of_I-9 [9:0] BG BB Int charge ch64 for E_of_I-10 [9:0]
767 BG BB Int charge ch64 for E_of_I-7 [9:0] BG BB Int charge ch64 for E_of_I-8 [9:0]
768 BG BB Int charge ch64 for E_of_I-5 [9:0] BG BB Int charge ch64 for E_of_I-6 [9:0]
769 BG BB Int charge ch64 for E_of_I-3 [9:0] BG BB Int charge ch64 for E_of_I-4 [9:0]
770 BG BB Int charge ch64 for E_of_I-1 [9:0] BG BB Int charge ch64 for E_of_I-2 [9:0]
771 BG BB Int charge ch64 for E_of_I+1 [9:0] BG BB Int charge ch64 for E_of_I [9:0]
772 BG BB Int charge ch64 for E_of_I+3 [9:0] BG BB Int charge ch64 for E_of_I+2 [9:0]
773 BG BB Int charge ch64 for E_of_I+5 [9:0] BG BB Int charge ch64 for E_of_I+4 [9:0]
774 BG BB Int charge ch64 for E_of_I+7 [9:0] BG BB Int charge ch64 for E_of_I+6 [9:0]
775 BG BB Int charge ch64 for E_of_I+9 [9:0] BG BB Int charge ch64 for E_of_I+8 [9:0]
776 BG BB Int charge ch64 for E_of_I+10 [9:0]
data of channel 64
777 timing_HPTDC_channel_64[31:0]
778 scaler T1
779 scaler T2
780 scaler T3
781 scaler T4
782 scaler T5
783 scaler T6
784 scaler T7
785 scaler T8
786 scaler T9
787 scaler T10
788 scaler T11
789 scaler T12
790 scaler T13
791 scaler T14
792 scaler T15
793 scaler T16
triggers scaler
794 scaler BB channel 1 [63:32]
795 scaler BB channel 1 [31:0]
sc BB ch1
796 scaler BG channel 1 [63:32]
797 scaler BG channel 1 [31:0]
sc BG ch1
798 scaler BB channel 2 [63:32]
799 scaler BB channel 2 [31:0]
sc BB ch2
800 scaler BG channel 2 [63:32]
801 scaler BG channel 2 [31:0]
sc BG ch2

scaler BB channel 64 [63:32]										sc BB ch64
scaler BB channel 64 [31:0]										
scaler BG channel 64 [63:32]										sc BG ch64
scaler BG channel 64 [31:0]										
bunch number for minimum bias -10										bunch n° for MB
bunch number for minimum bias -9										
bunch number for minimum bias -8										
bunch number for minimum bias -7										
bunch number for minimum bias -6										
bunch number for minimum bias -5										
bunch number for minimum bias -4										
bunch number for minimum bias -3										
bunch number for minimum bias -2										
bunch number for minimum bias -1										
	BG	BB	Int	charge on ch1 for minimum-bias -9 [9:0]		BG	BB	Int	charge on ch1 for minimum-bias -10 [9:0]	MB ch1
	BG	BB	Int	charge on ch1 for minimum-bias -7 [9:0]		BG	BB	Int	charge on ch1 for minimum-bias -8 [9:0]	
	BG	BB	Int	charge on ch1 for minimum-bias -5 [9:0]		BG	BB	Int	charge on ch1 for minimum-bias -6 [9:0]	
	BG	BB	Int	charge on ch1 for minimum-bias -3 [9:0]		BG	BB	Int	charge on ch1 for minimum-bias -4 [9:0]	
	BG	BB	Int	charge on ch1 for minimum-bias -1 [9:0]		BG	BB	Int	charge on ch1 for minimum-bias -2 [9:0]	
	BG	BB	Int	charge on ch2 for minimum-bias -9 [9:0]		BG	BB	Int	charge on ch2 for minimum-bias -10 [9:0]	MB ch2
	BG	BB	Int	charge on ch2 for minimum-bias -7 [9:0]		BG	BB	Int	charge on ch2 for minimum-bias -8 [9:0]	
	BG	BB	Int	charge on ch2 for minimum-bias -5 [9:0]		BG	BB	Int	charge on ch2 for minimum-bias -6 [9:0]	
	BG	BB	Int	charge on ch2 for minimum-bias -3 [9:0]		BG	BB	Int	charge on ch2 for minimum-bias -4 [9:0]	
	BG	BB	Int	charge on ch2 for minimum-bias -1 [9:0]		BG	BB	Int	charge on ch2 for minimum-bias -2 [9:0]	
	BG	BB	Int	charge on ch3 for minimum-bias -9 [9:0]		BG	BB	Int	charge on ch3 for minimum-bias -10 [9:0]	MB ch3
	BG	BB	Int	charge on ch3 for minimum-bias -7 [9:0]		BG	BB	Int	charge on ch3 for minimum-bias -8 [9:0]	
	BG	BB	Int	charge on ch3 for minimum-bias -5 [9:0]		BG	BB	Int	charge on ch3 for minimum-bias -6 [9:0]	
	BG	BB	Int	charge on ch3 for minimum-bias -3 [9:0]		BG	BB	Int	charge on ch3 for minimum-bias -4 [9:0]	
	BG	BB	Int	charge on ch3 for minimum-bias -1 [9:0]		BG	BB	Int	charge on ch3 for minimum-bias -2 [9:0]	
	BG	BB	Int	charge on ch4 for minimum-bias -9 [9:0]		BG	BB	Int	charge on ch4 for minimum-bias -10 [9:0]	MB ch4
	BG	BB	Int	charge on ch4 for minimum-bias -7 [9:0]		BG	BB	Int	charge on ch4 for minimum-bias -8 [9:0]	
	BG	BB	Int	charge on ch4 for minimum-bias -5 [9:0]		BG	BB	Int	charge on ch4 for minimum-bias -6 [9:0]	
	BG	BB	Int	charge on ch4 for minimum-bias -3 [9:0]		BG	BB	Int	charge on ch4 for minimum-bias -4 [9:0]	
	BG	BB	Int	charge on ch4 for minimum-bias -1 [9:0]		BG	BB	Int	charge on ch4 for minimum-bias -2 [9:0]	

Raw Data Format

This format of Raw Data (common header as defined by the DAQ group and data blocks transferred over one DDL) has been implemented in AliRoot by Cvetan in classes **AliVZEROBuffer** and **AliVZERORawStream**

Conversion from DDL Raw Data to Digits can be achieved using macro **VZERORaw2Digits**

Calibration information

VZERO calibration object is defined in **AliVZEROCalibData** as arrays of

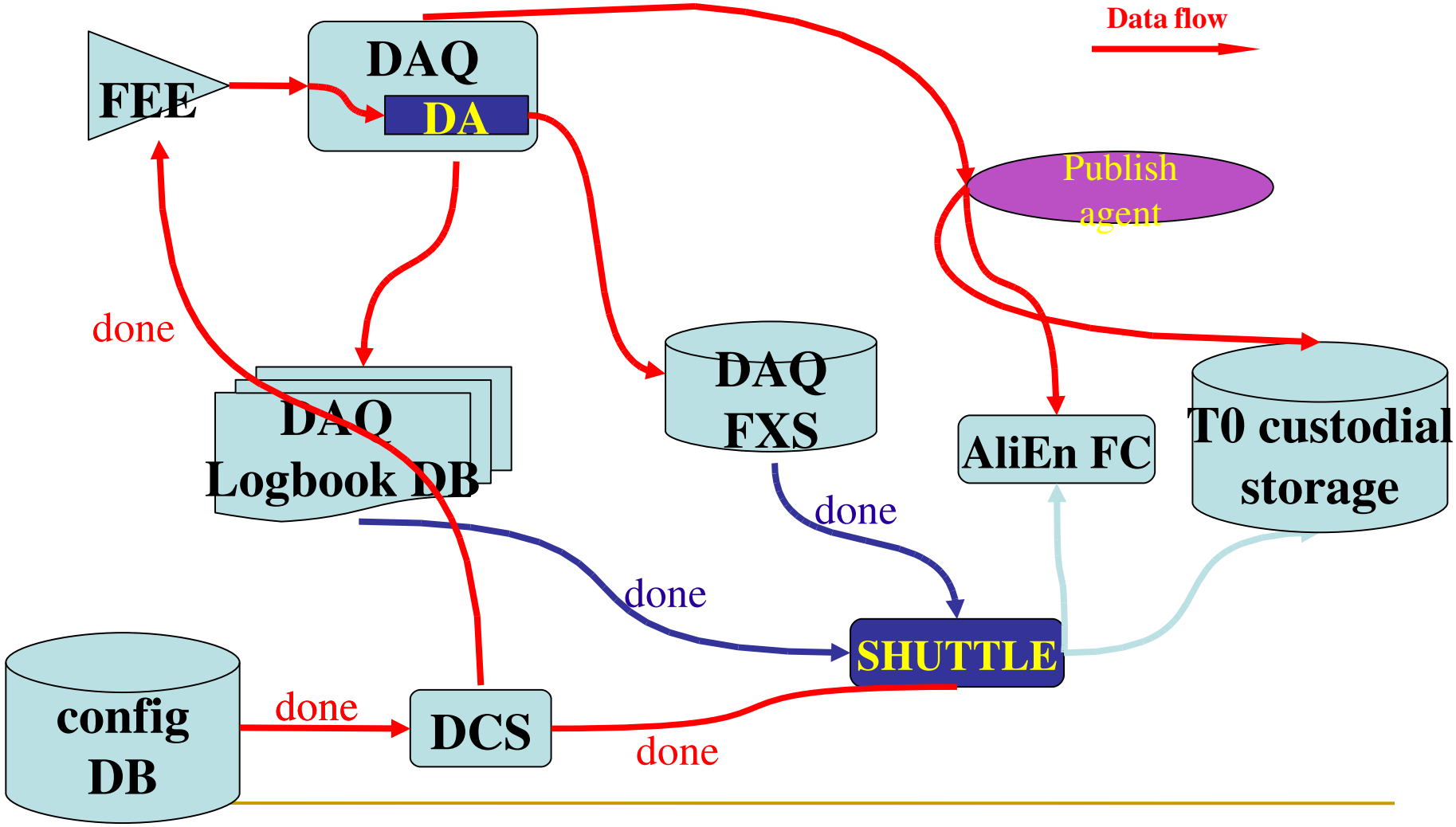
- ADC pedestals (128 Float_t)
- ADC sigmas of pedestal distributions (128 Float_t)
- ADC gains (128 Float_t)

- time offsets (64 Float_t)
- time gains (64 Float_t)

- High Voltages (64 Float_t)
- widths of HV (64 Float_t)

(128 values for ADC information because two sets of ADCs will be used)

Calibration strategy



SHUTTLE Preprocessor

AliVZEROPreprocessor has been implemented in Aliroot and committed to CVS. It has been checked using dummy files.

It retrieves:

- High Voltages mean values from **DCS** through object **AliVZERODataDCS**

- ADC pedestals, sigmas, and gains from **DAQ** through the FXS

and stores them into CDB as a VZEROCalibData object

DA for calibration

All the information needed for calibration is recorded within PHYSICS runs.

Therefore the DA will

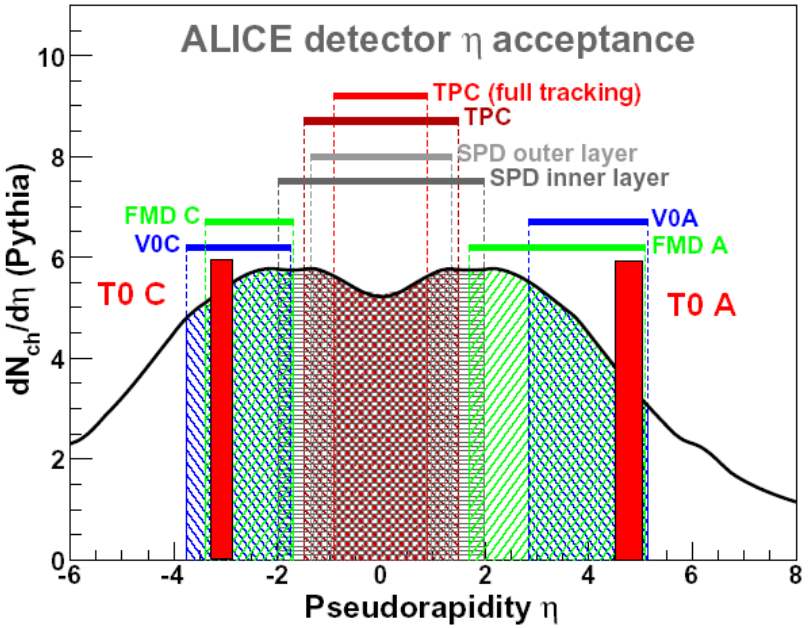
- read data of PHYSICS runs from DAQ LDC and select calibration-dedicated information
- create ADC and TDC histograms for each channel
- fit histograms
- give to FXS values of pedestals, sigmas and gains (stored in DAQ FXS file V0_Ped_Width_gain.dat to be fetched by the SHUTTLE VZEROPreprocessor)

Work in progress

Backup slides follow

The V0 detector (II)

V0C



Δη	V0A	V0C
Ring 1	5.1/4.5	-3.7/-3.2
Ring 2	4.5/3.9	-3.2/-2.7
Ring 3	3.9/3.4	-2.7/-2.2
Ring 4	3.4/2.8	-2.2/-1.7

Cell numbering

As seen from IP: